SSD revue June 2012

SSD Electronics Upgrade
The ladder card

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Mines-Nantes; Université de Nantes; France

Ladder card
overview (1/2)

The ladder card is the upgrade for the CONNEXION card (sometimes called C2D2 card) and for the ADC card. There is one ladder card at each end of a ladder.

There are four versions of the ladder card:

✓ Version 0 "mechanical prototype": non-functional card. Only to verify mechanical integration

✓ Version 1 "prototype": test and validation of technical choices

➢ Version 2 "preproduction": validation of the card

➢ Version 3 "production": should be the same as v2. To be installed in STAR

Ladder card
overview (2/2)
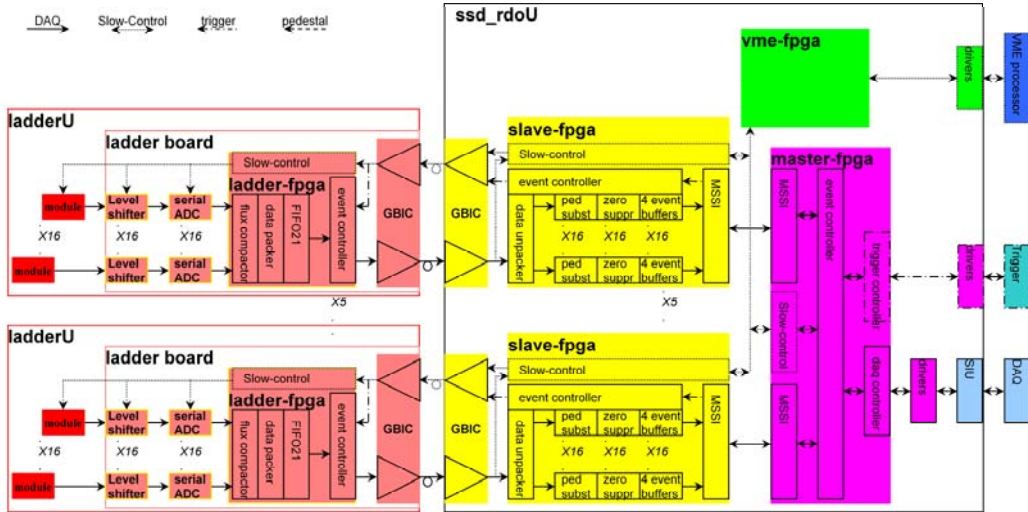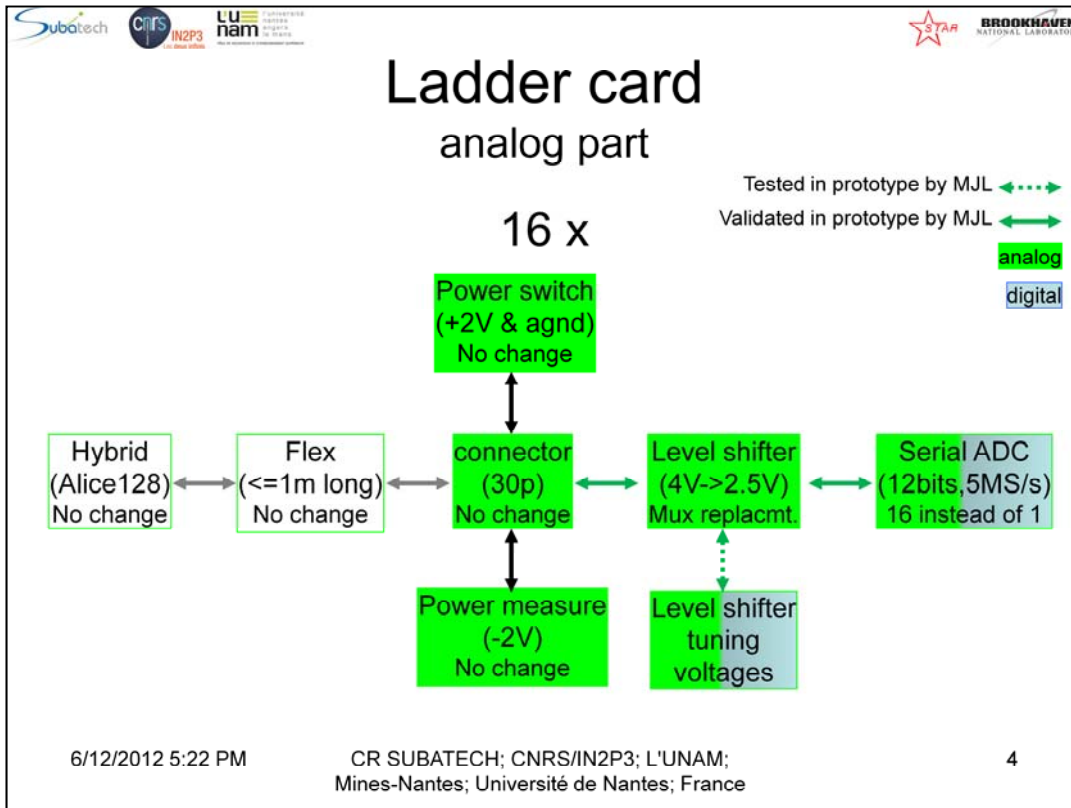
The only change (compared to old SSD) in the analog part is the ADC.

The 16 analog lines were multiplexed to 1 ADC.

Now, each analog line has a dedicated ADC.

The new ADC works at lower voltage, implying level shifting for the analog lines.

MJL tested Analog to Digital conversion of static voltages applied to the input connectors.

Level shifter showed bad rejection of analog power supplies due to Digital to Analog converter used as tunable voltage reference.
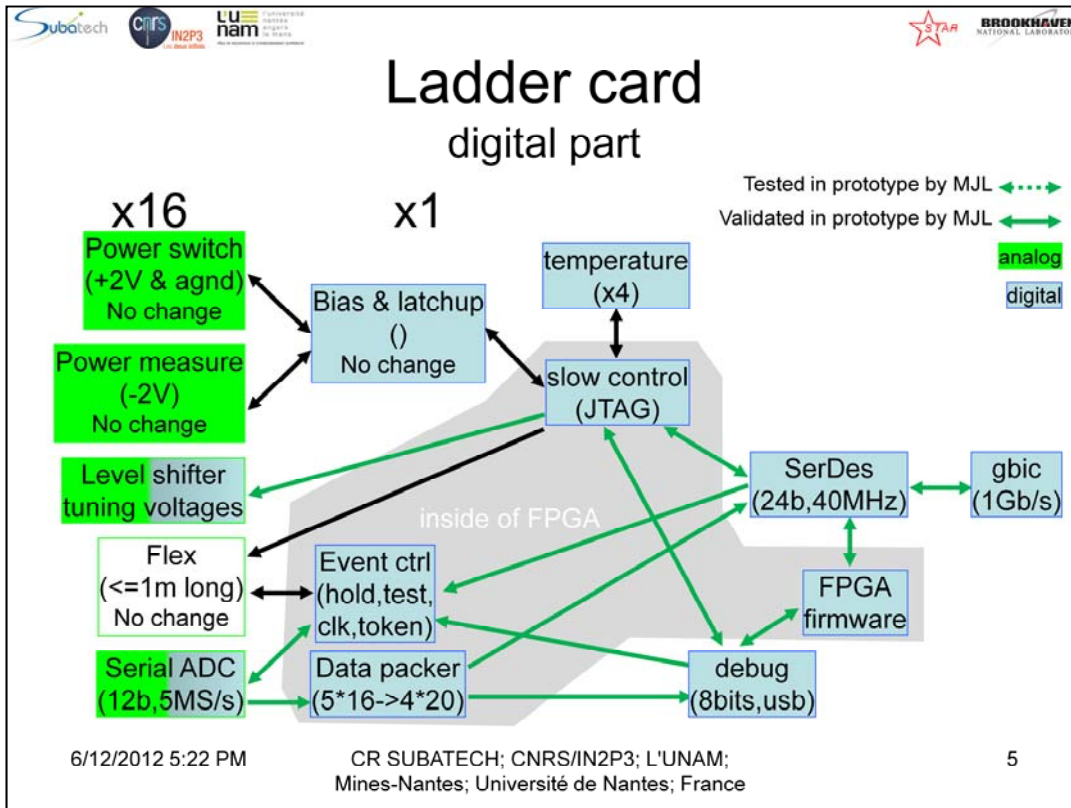
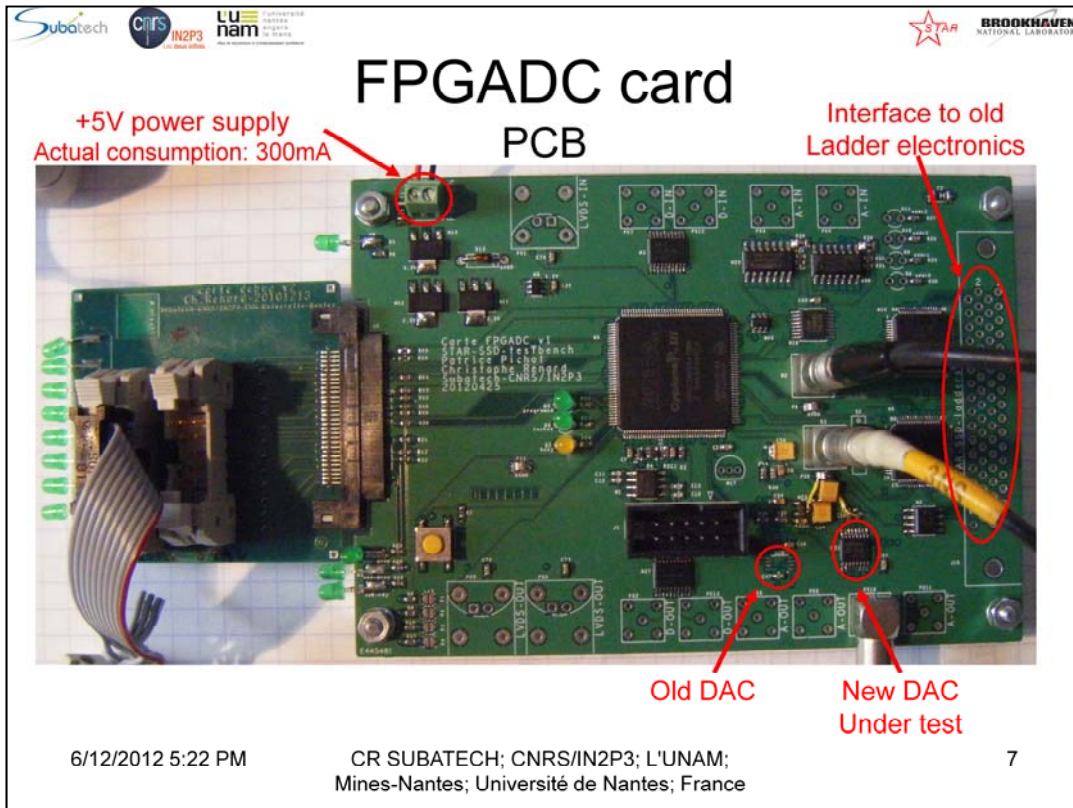The digital part of the ladder board is mostly new, due to the changes

• from 1 to 16 ADC (now, we convert data from the 16 sensors at the same time),

• from parallel ADC to serial ADC

• from daisy chain copper bus to high speed serial optical line

MJL validated programming of FPGA firmware, slow-control and acquisition using both GBIC interface and debug interface.

Ladder card
to do list for preproduction (at SUBATECH)

- Verify ADC (acquisition) with dynamic voltages
- Verify ADC (acquisition) with real module(s)
- Verify slow-control with real module(s)
- Validate a design for level-shifter tuning (DAC)
- Insert DAC modifications in schematics and PCB
- Generate GERBER files for fab
- Update documentation on the web

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Ladder card
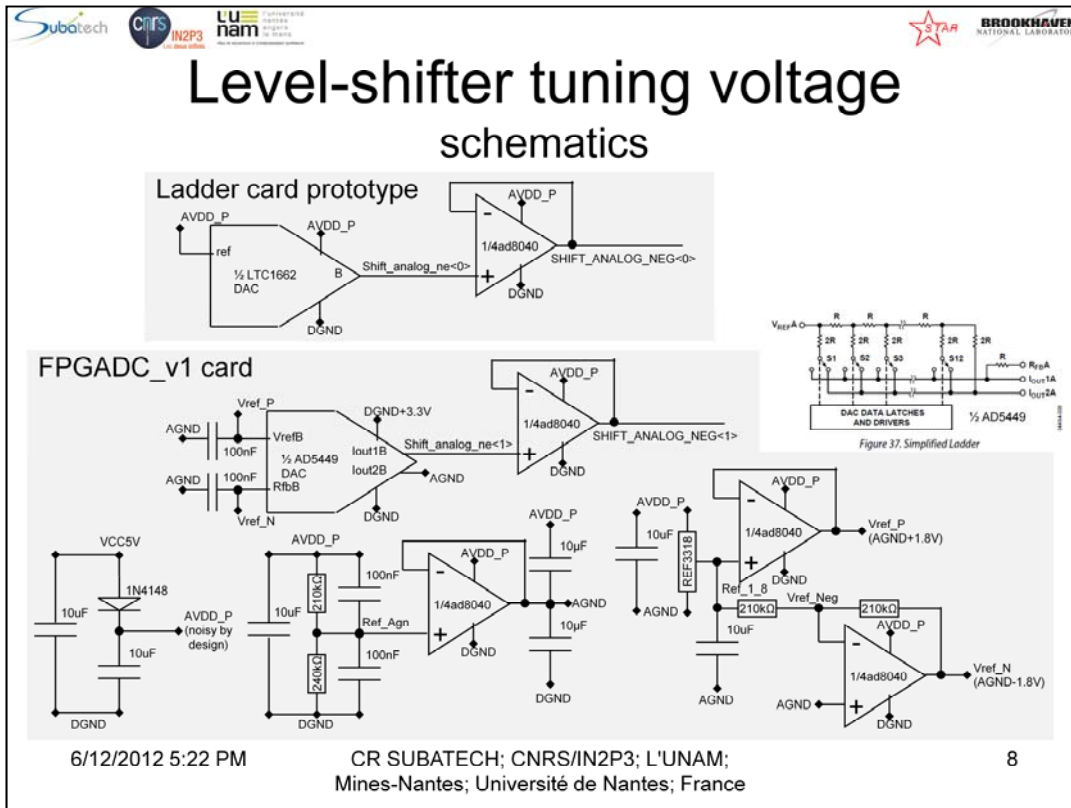## to do list for preproduction (at SUBATECH)

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FPGADC_v1 card will replace the old test bench that we used to test ladders equipped with the old electronics.

I added some components to test a new design for the DAC.

New firmware in FPGA to setup values in new DAC is working.

Level-shifter tuning voltage
schematics

Ladder card prototype / FPGADC_v1 card

Figure 37. Simplified Ladder

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<u>Ladder card prototype:</u>

• Shift_analog_ne<0> referenced to DGND => copies -2V power supply variations

• Reference input of LTC1662 connected to +2V power supply => Shift_analog_ne<0> copies +2V power supply variations

<u>FPGADC_v1 card:</u>

• Shift_analog_ne<1> referenced to AGND => independent from -2V power supply variations

• Reference inputs of AD5449 connected to Vref_P and Vref_N voltages => Shift_analog_ne<1> independent from +2V power supply variations

• AVDD_P intentionally made noisy to see how Shift_analog_ne<1> rejects this noise
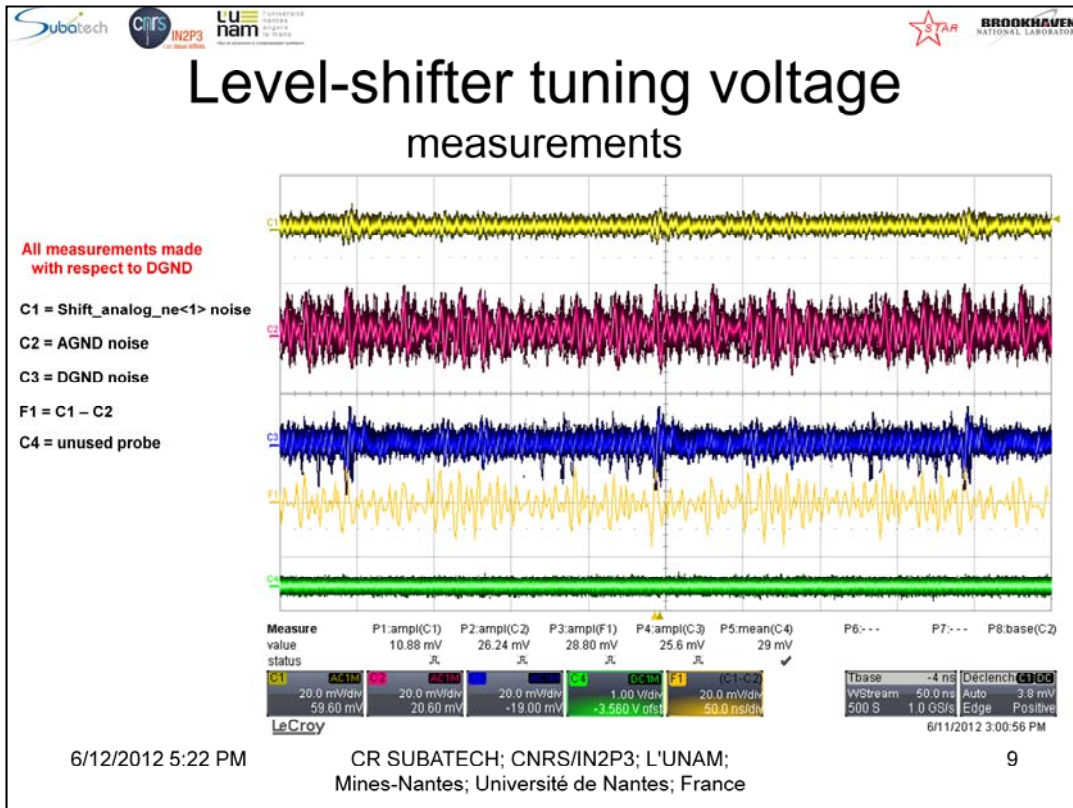
Abnormal noise on AGND comes mainly from bad decoupling on FPGADC card.
More tests needed to validate (or reject) new design.

Ladder card
options (1/2)

Fabrication options:

1. Fabricate few pre-prod now. Populate them for tests. Then fabricate prod, taking test results into account.

2. Fabricate full prod now but populate only few for tests. Eventually fabricate new prod, taking test results into account.

DAC options:

a) Keep actual DAC (LT1662) as-is

b) Keep actual DAC (LT1662) but use a +1.8V voltage reference instead of +2V supply at the reference input.

c) Use new DAC (AD5449)

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1. is preferred by Jim.
    → safe
    → slow (?): each fab takes ~2 months (including paperwork)

2. Is proposed (preferred?) by Micheal
→ gamble on test results
→ (could be) fast: saves one fab (~2 months)

a)
    → ready now
    → will physics accept resulting resolution ?

b)
    → almost ready now
    → easy to reverse to a)
    → will physics accept resulting resolution ?

c)
    → needs time to validate, then implement in design

Ladder card
options (2/2)

1.b+a|b|c: fab & test now option b). Then prod with option a) or b) or c),
   depending on tests
   → do we have time ?

1.c+a|b|c : fab & test now option c). Then prod with option a) or b) or c),
   depending on tests
   → do we have time ?

2.a: fab & test now option a). Then populate prod with option a)
   → will physics accept resulting resolution ?

2.b: fab & test now option b). Then populate prod with option a) or b) ,
   depending on tests
   → will physics accept resulting resolution ?

2.c(+?): fab & test now option c). Then populate prod with option c) or fab new
   prod with option a) or b), depending on tests
   → do we have time ?

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Many thanks for your attention

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