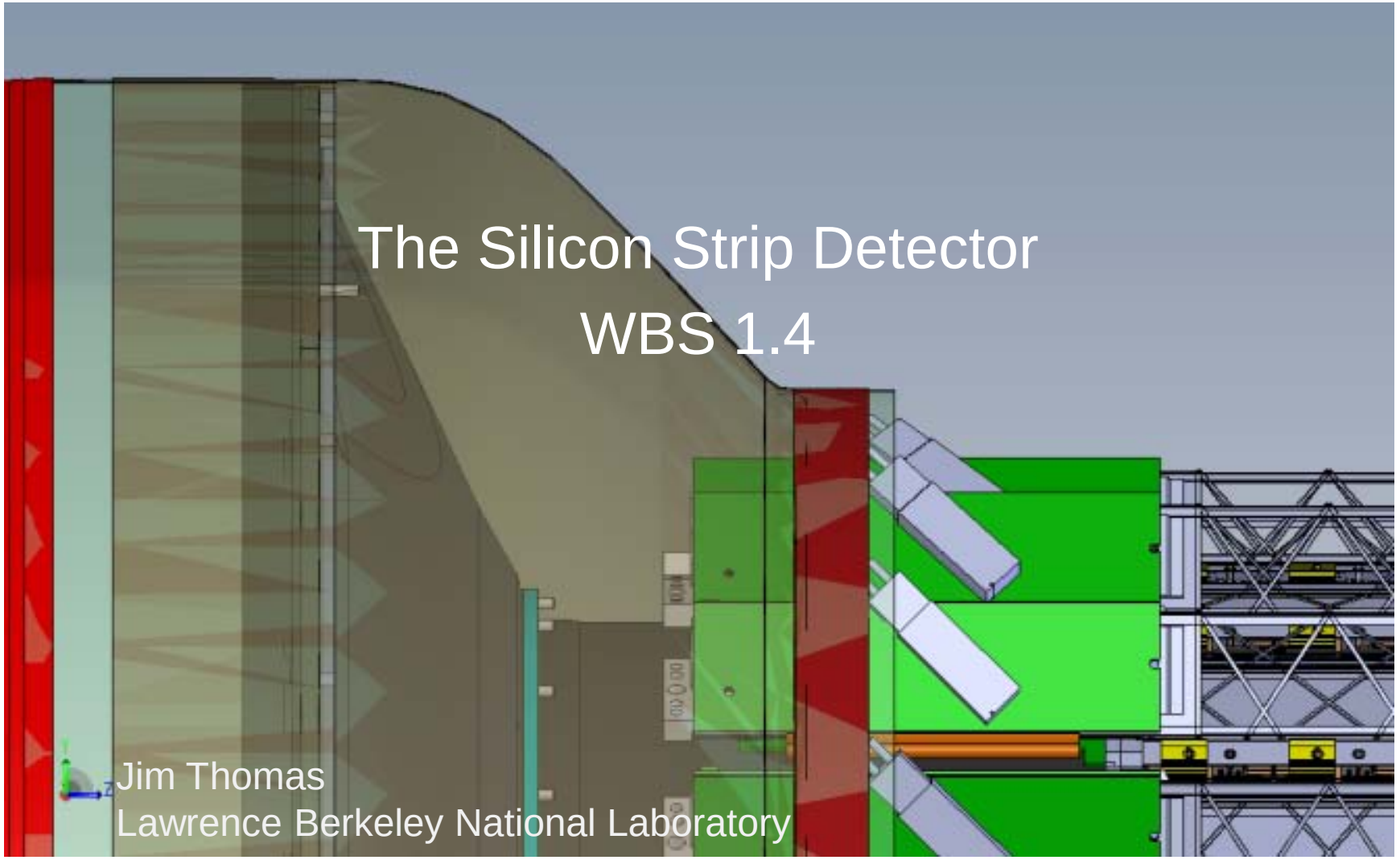
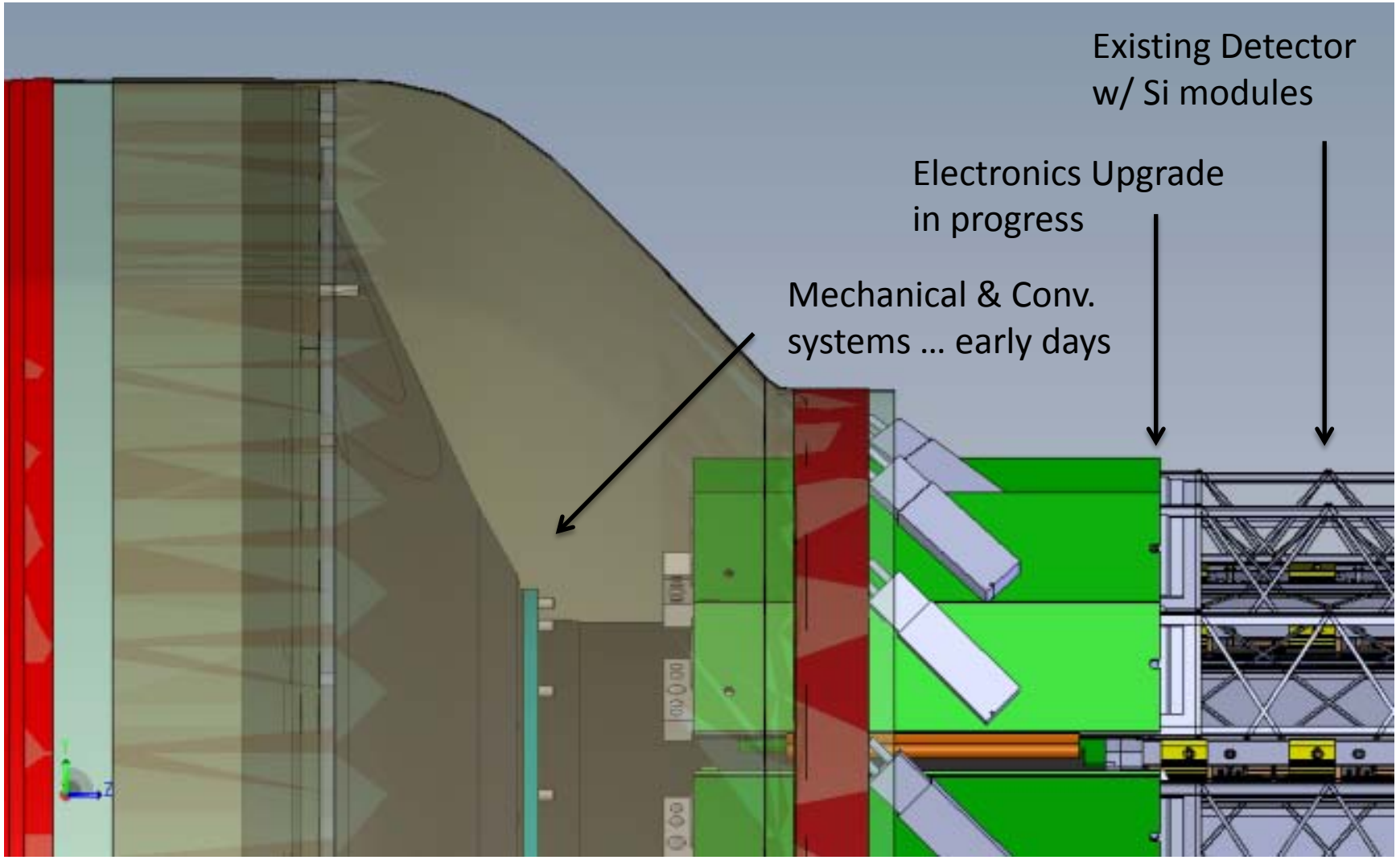
STAR HFT



The Silicon Strip Detector
WBS 1.4

Jim Thomas
Lawrence Berkeley National Laboratory

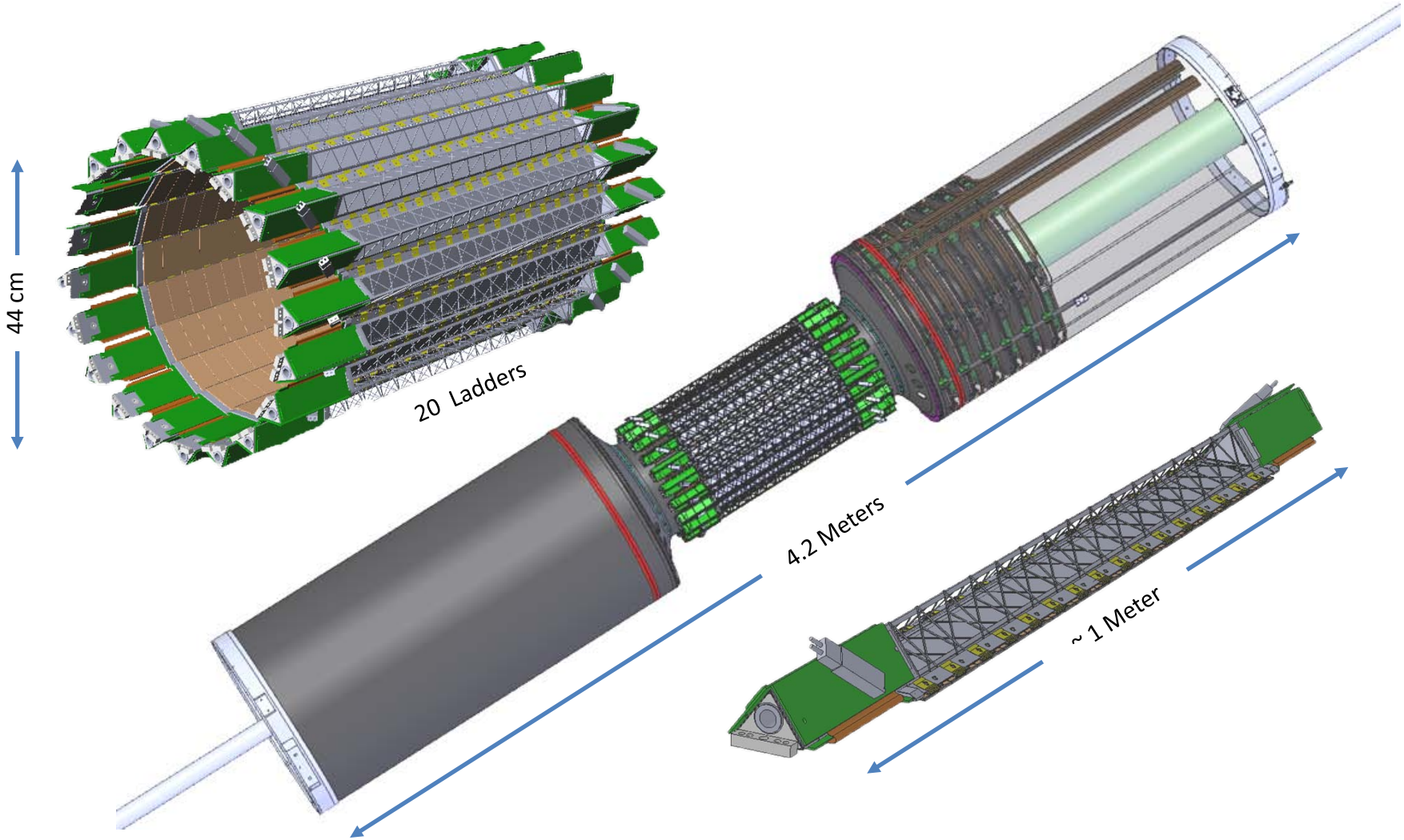
The SSD is an existing detector ⇒ upgrade



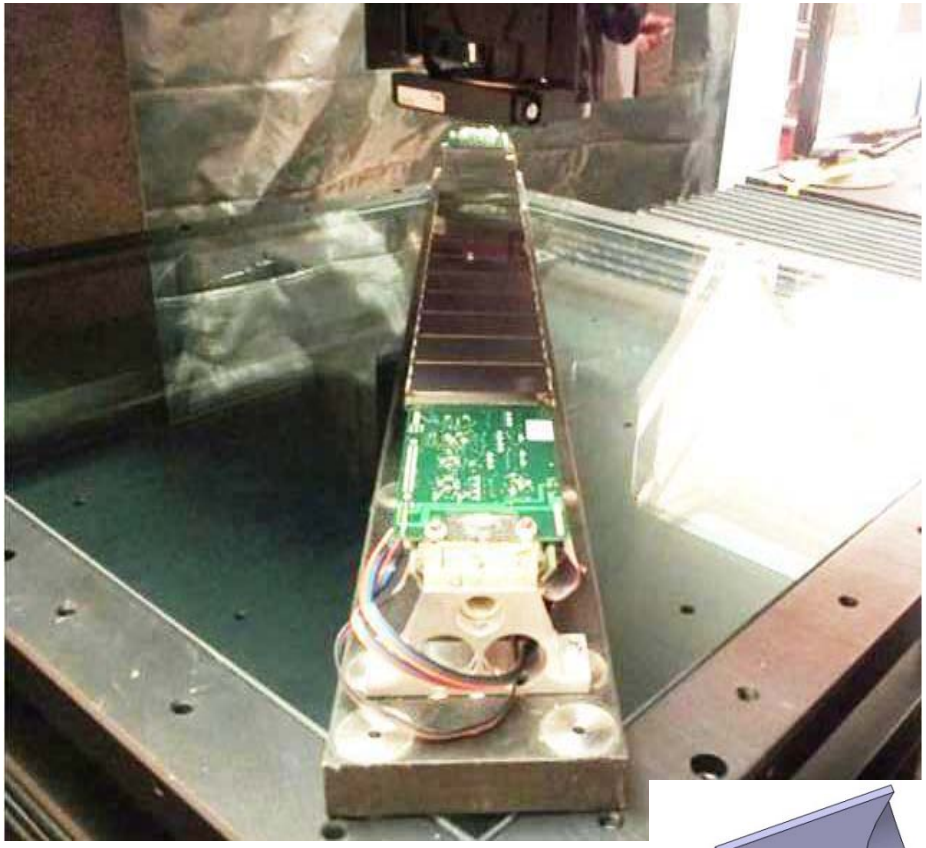
Outline

- Brief overview of the subsystem
- Technical Progress since the last review
  - Construction and Procurement Activity
- Resources
  - People and institutions
- Reviews and Milestones
- Risk assessment
- Cost & Schedule
- Summary

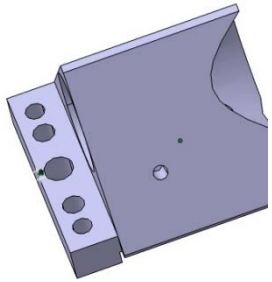
SSD Overview – the SSD sits on the OSC

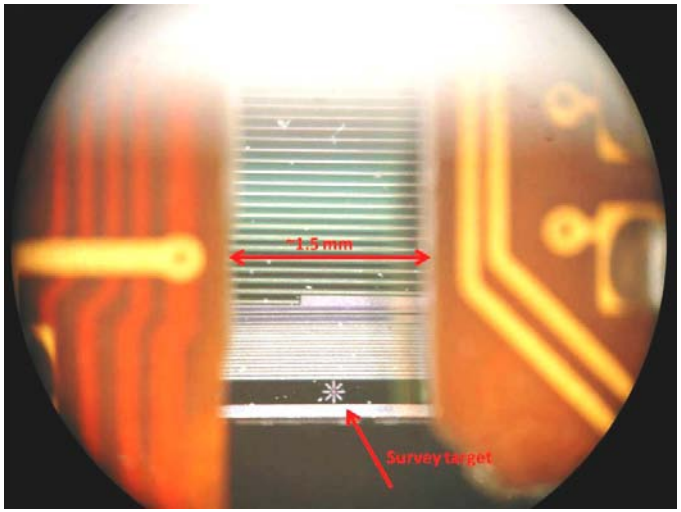


Progress: Ladder 0 is ready to be surveyed

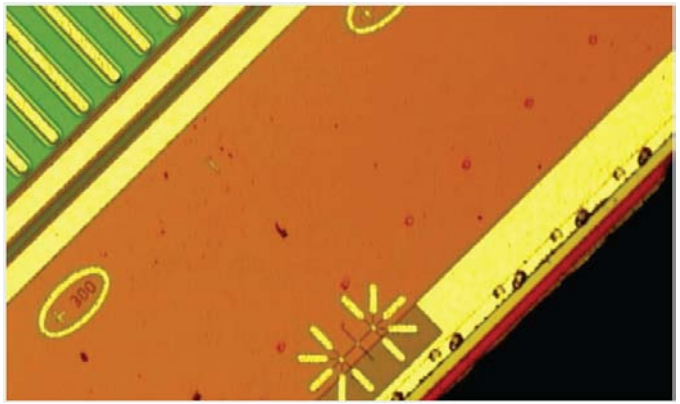


Reference point for survey and mounting on OSC



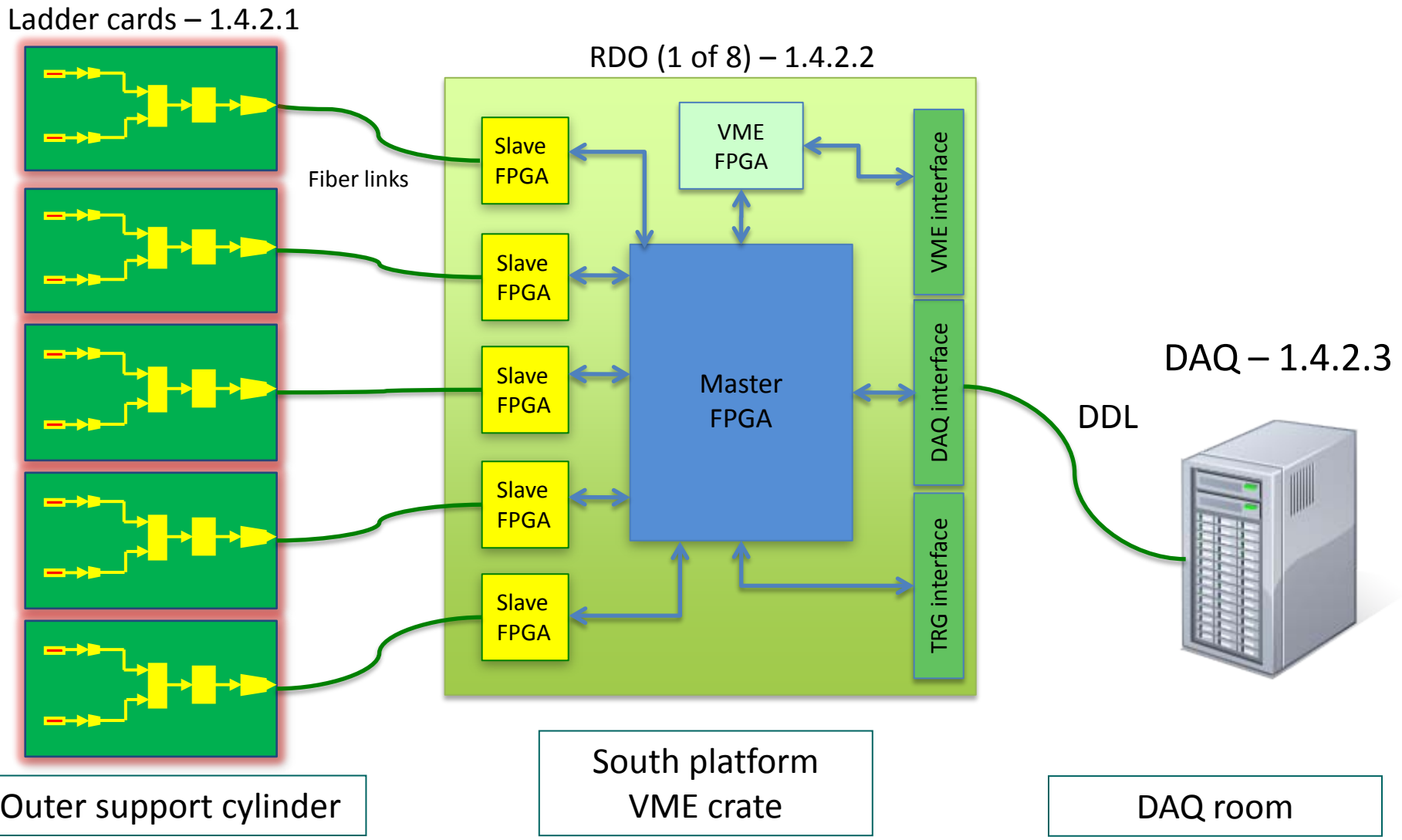


Target on end of wafer (backside)

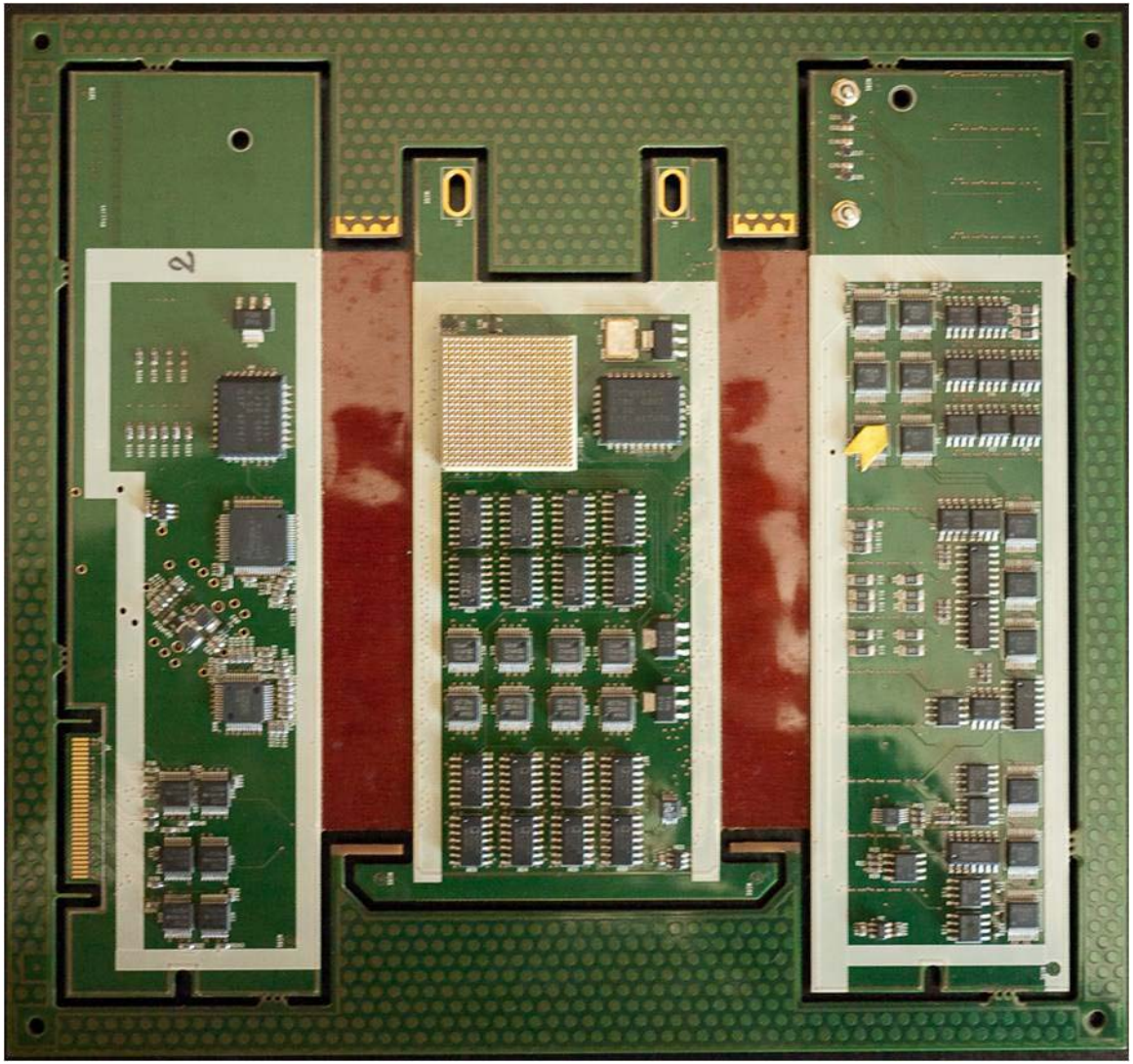


Targets on edges of wafer (front)

Readout Electronics – the heart of the upgrade



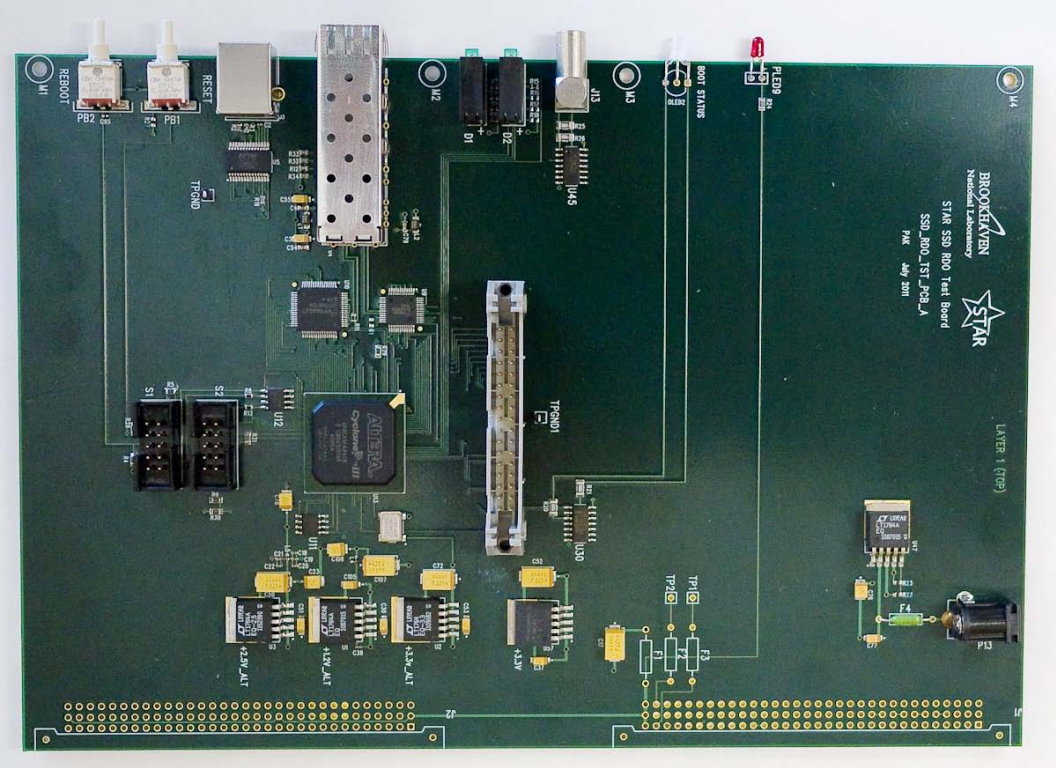
Progress: Ladder Card built and tested



- Prototype with interposer card working since about the time of our previous OPA review
- A new layout with the improved FGPA traces has been completed.
- Next Step:

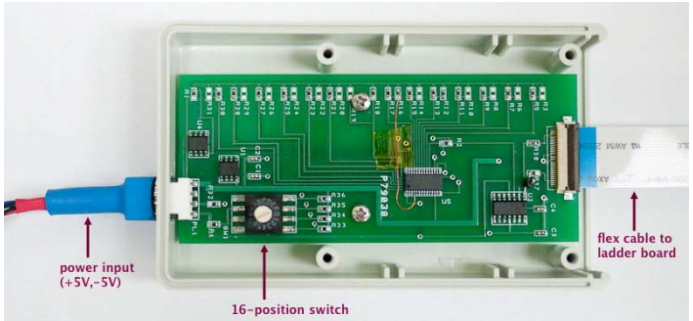
  Preparing to pass from prototype to pre-production version

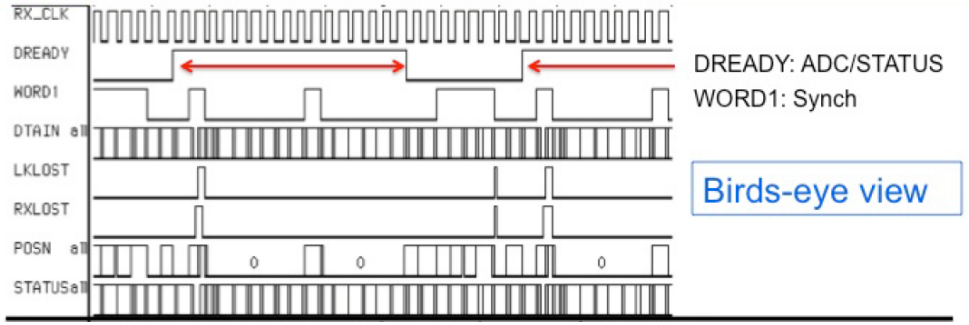
Progress: ‘Quick’ RDO built and tested



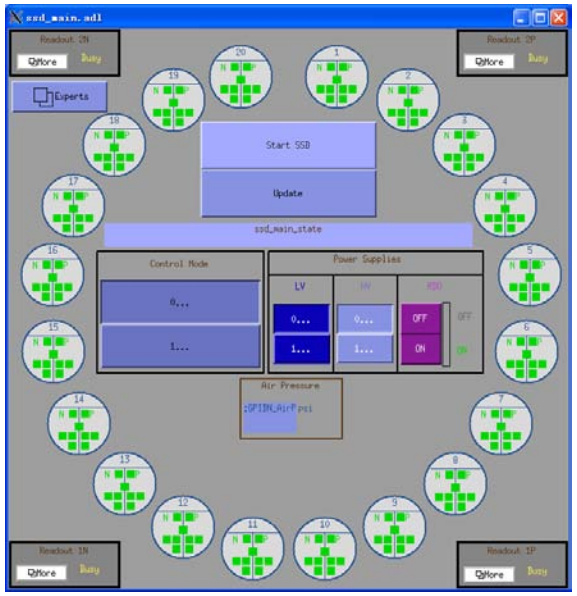
- Prototype RDO board w/services for 1 ladder
- A complete RDO board has recently been completed and sent off for fabrication
- Milestone:

  Passed from prototype to pre-production version

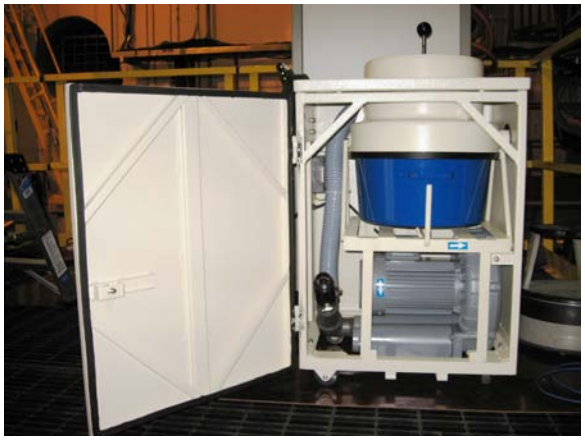




Progress: Slow Controls and Conventional Systems



- Weihua Yan has developed a slow controls interface to the new Power supplies
- Working on the more complex problem of JTAG communication to the ladders
- Prototype quantities of PS and Power modules are in-house



Cooling system – vacuum

Instrumentation for cooling

Progress: Mechanical Engineering

Done:

WSC, OSC & ESC

To Do:

Split the shroud so it is easier to install the SSD ladders

Route air in & vacuum out via East end only

Ladder mounts

Cable and hose routing under the shroud is in progress

Resources and Institutions

BNL	Micheal LeVine	Design & test, VHDL, ++
	Bob Sheetz	EE on RDO board, ++
	John Hammond	EE layout RDO board
	Tim Camarada	EE technical work
	Bob Soja	ME technical work
CEEM / IUCF	Gerard Visser	Cables
Subatech	Christophe Renard	EE layout LB, VHDL, ++
	Stéphane Bouvier	Silicon Modules
	Gerard Guilloux	Ladder Mechanics
LBL	Jim Thomas	Conv. Sys. Design & test, ++
	Eric Anderssen	HFT Mechanical Engineering
	Joseph Silber	HFT Mechanical Engineering
Tsinghua	Weihua Yan - student	Slow Controls

SSD Internal Review – 6/20/2012

- SSD Electronics (and other systems) Review
  - Chair: H.G. Ritter
  - Committee: Anderssen, Greiner, Schambach, Stezelberger and Visser
- Charge
  - Design of Ladder Board
  - Design of the RDO board
  - Interface documentation
  - Test results with prototypes
- Recommendations (major items)
  - The LB may proceed from prototype to pre-production step
    - but also recommended new voltage reference and additional tests
  - The RDO may proceed from the prototype to pre-production step
  - Create a testing plan specifying which functionality will be tested and how

SSD Milestone List

Level	Milestone	BCP #3 Date	Actual /Forecast
1	CD-4 Approve Project Completion	Jul-15	Jul-15
1.4	**SSD**		
2	SSD Preproduction Design Review of RDO		Jun-12 (A)
2	SSD Production of Ladder Boards ready to begin	Nov-12	Dec-12
2	SSD Assembled onto OSC ready for installation	Aug-13	Sep-13
3	L3 - SSD RDO Design Finished	3/30/12	Jun-12 (A)
3	L3 - Preproduction Ladder Board PCB Received	8/10/12	TBD
3	L3 - Production RDO Board Received	3/22/13	3/22/13
3	L3 - Installation of cooling on STAR platform and Magnet Endcap complete	8/16/13	8/16/13

Risk assessment – selected highlights

STAR HFT

WBS #	Description of Risk	Mitigation	Level
1.4.2.1.1	Ladderboard PCB design & layout	Schedule and budget include 3rd iteration of prototype boards	Moderate impact High severity
1.4.2.2.1	RDO PCB design and layout	Schedule and budget include 3rd iteration of prototype boards	Low impact Low severity ✓
1.4.2.1.2 1.4.2.1.3 1.4.2.2.2 1.4.2.2.3	Components (chips, DDL) unavailable	Procure components as soon as possible	Low impact Low severity ✓
1.4.4.4	Slow Controls Software Development Manpower	Obtain commitments as soon as possible	Low impact Low severity
1.4.2.3.3	DAQ Production components unavailable	Procure components as soon as possible	Low impact Low Severity ✓
1.4.3	Assembly –if STAR does not roll out in FY13 then IDS not available	Complete as many tests as possible – mock up remaining system tests	Low impact Low severity

✓ = **significant progress or reduced risk**

Cost and Schedule Summary

- SSD Costs have not changed much
  - the estimate has actually been revised downwards slightly since last review

- Two major procurement (> 50K) still to go.
  - Power Supply Modules and the associated Crates. Estimate $77K (1/27/2012) but we have reserved $84K for this procurement.
  - Production Ladder board fabrication originally estimated at $65K. This will almost certainly be < 50 K when final bids are in.

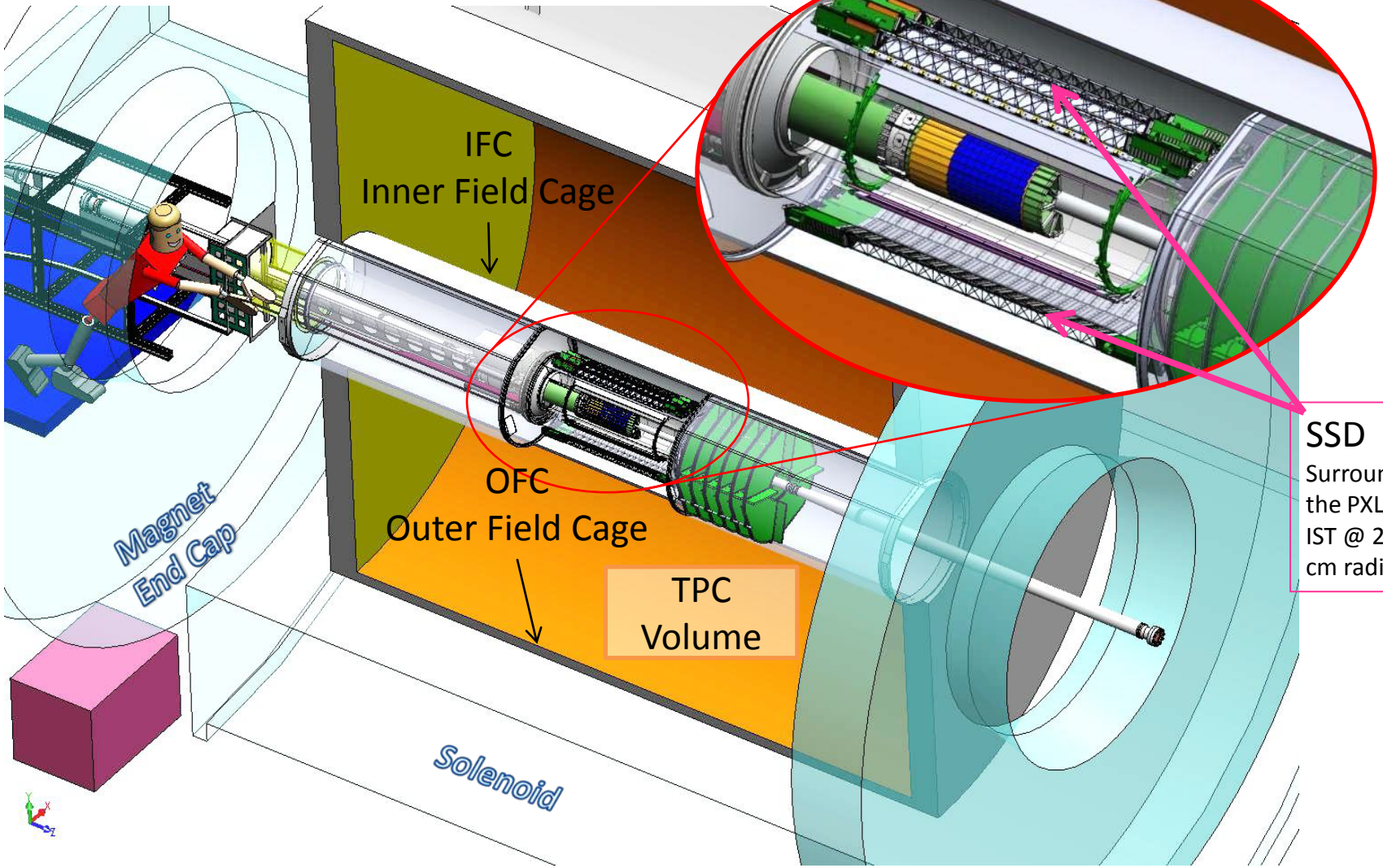
- We are behind schedule
  - Testing of the prototype Ladder Board is late and the completion of the design for the pre-production Ladder Board is late
  - ~ 2 month delay which we are still working to resolve
  - Our schedule can be scrubbed … but clearly the schedule is fragile

Summary

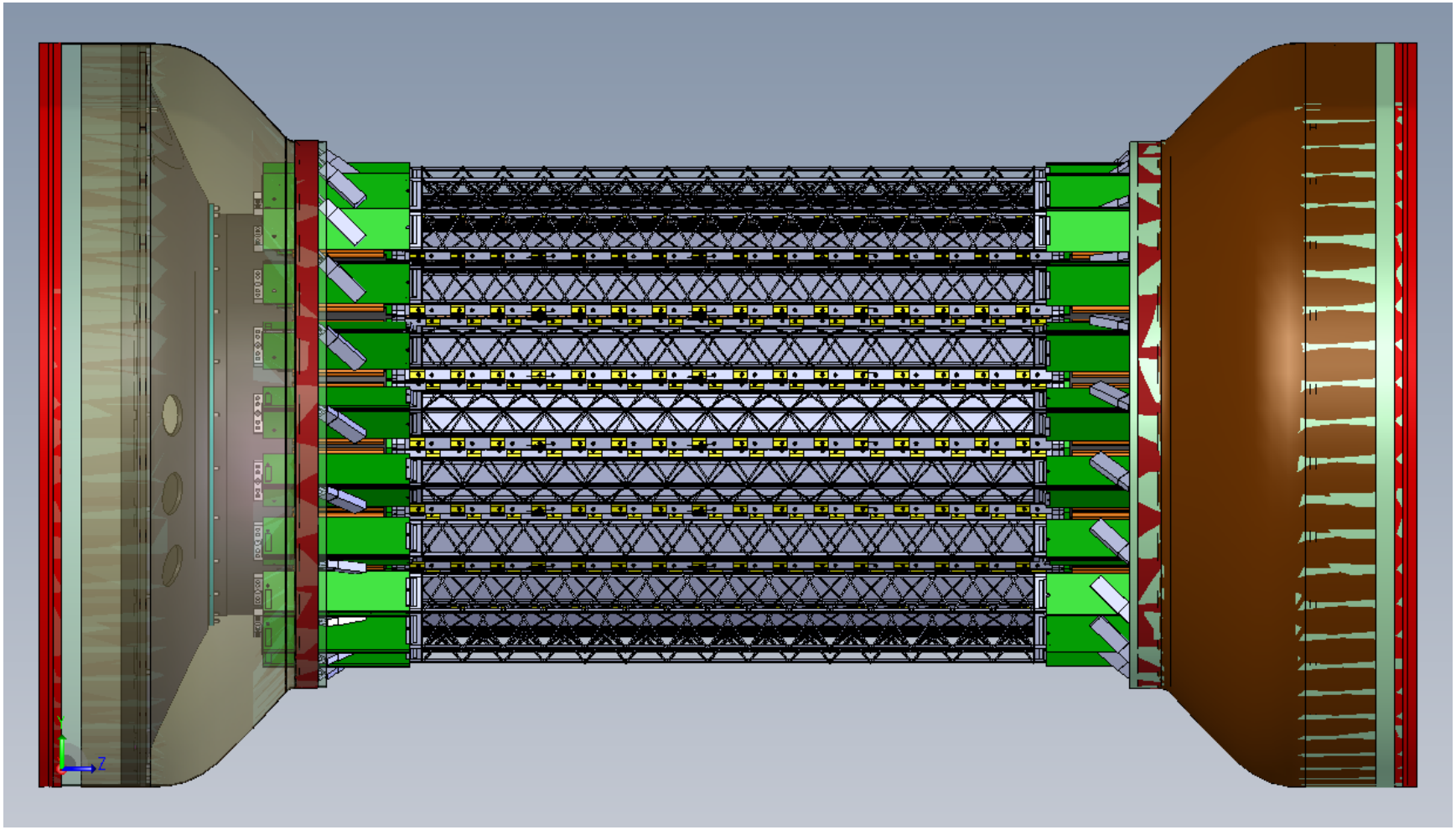
- The SSD upgrade project is clearly defined and the design requirements are understood
- We have a well developed 3 stage prototype, test and fabrication plan
- A great deal of progress has been made since last July
- The coming year will be dominated by fabrication of production electronics, mechanical engineering tasks, integrated testing and software development.
- Resources necessary for the completion of the project are in hand and, for the most part, readily available
- The costs are under control; keeping to schedule will be a challenge

Backup Slides

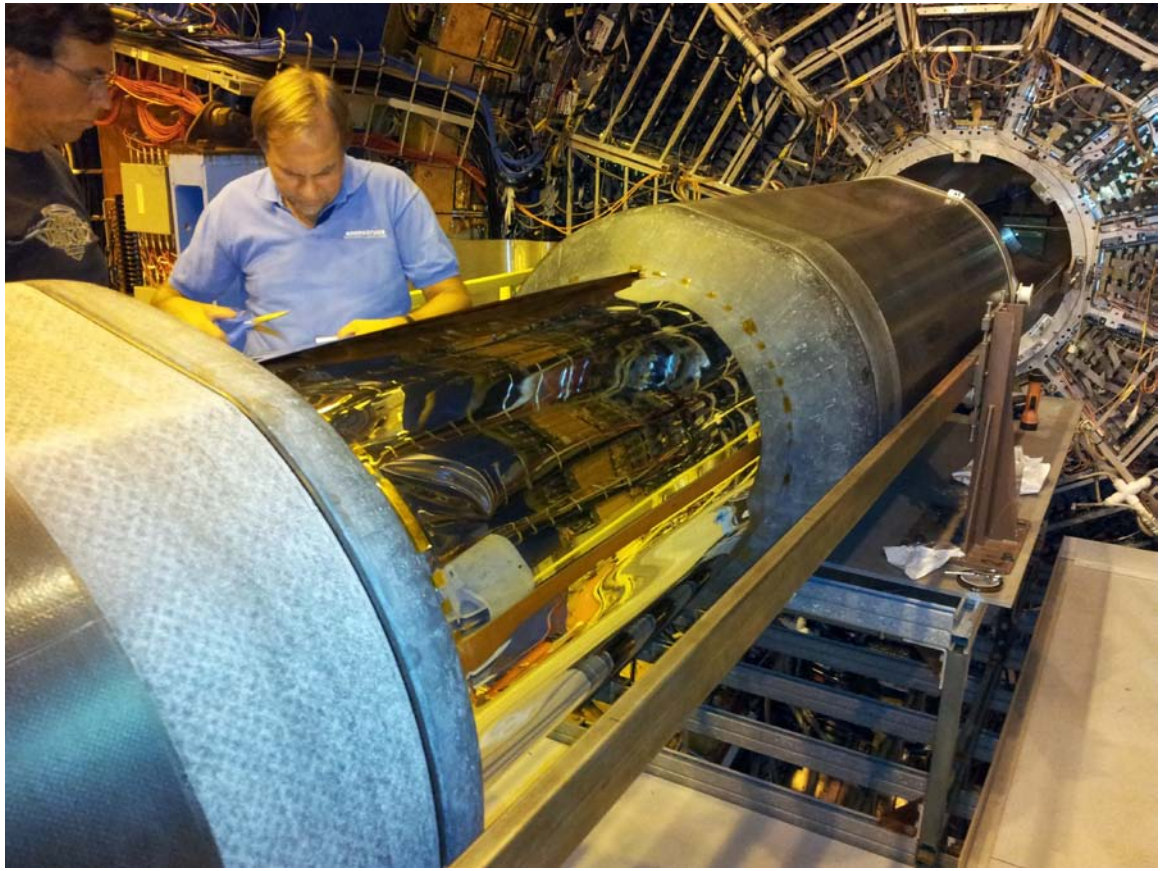
SSD Location in STAR



Schematic View of the SSD

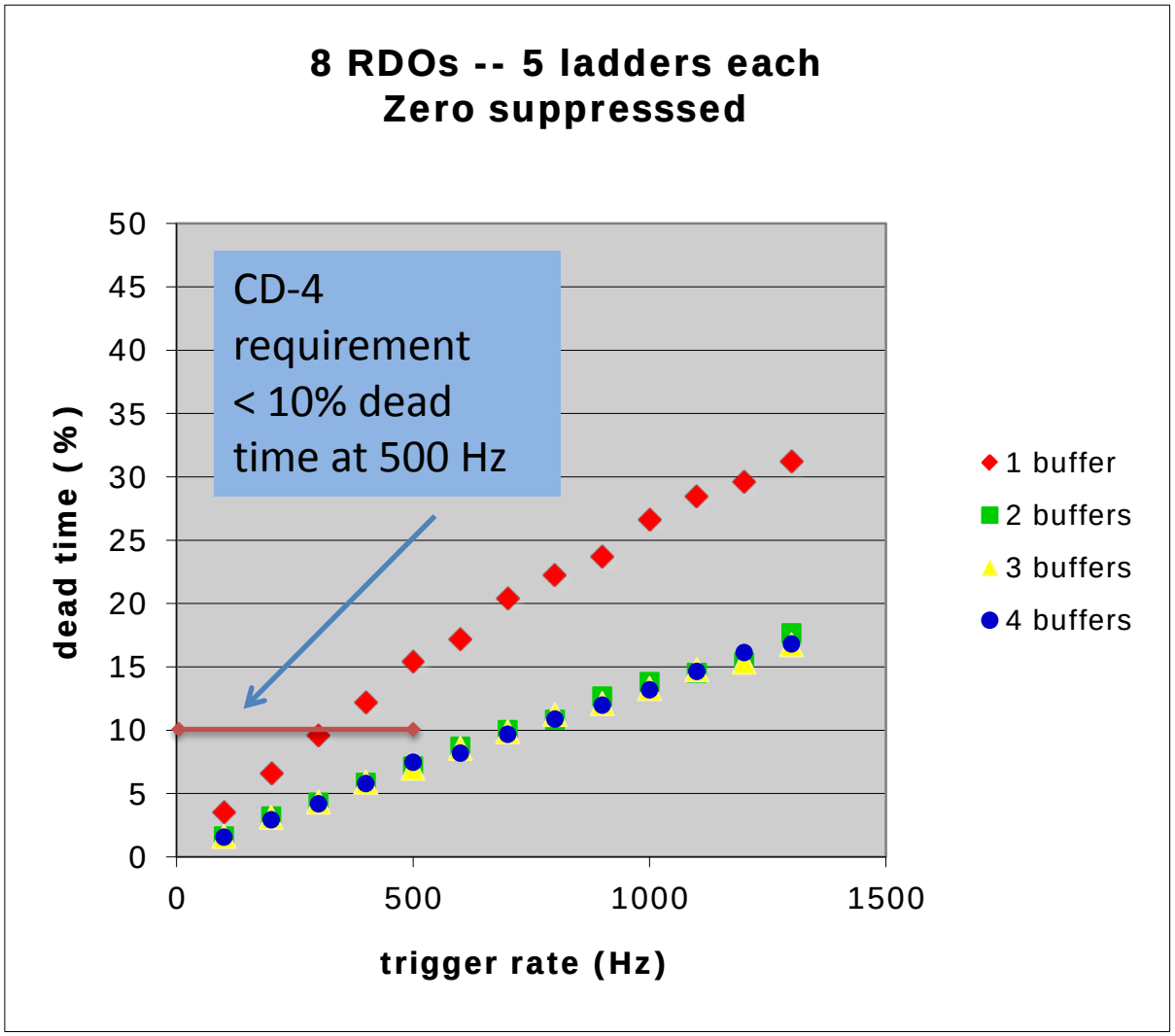


Progress: Mechanical Engineering



- Cable trays will be installed around FGT planes
- OSC with shroud and E&M shield installed
- SSD Specific work not yet complete

SSD CD4 Requirements on Dead time



- Dead-time as a function of random trigger rate
  - Simulated performance with 3% occupancy
- The SSD will have 4 buffers as part of the firmware
- Multiple buffers hide the downstream DAQ from the dead-time of the system for randomly arriving triggers

Charge for the Review

1. Technical: Is the design of the STAR HFT MIE technically sound? Are there plans in place for resolving any remaining technical issues to meet the CD-4, *Approve Start of Operations*, performance requirements?

2. Cost, Schedule, Risk, and Contingency: Are there adequate resources to complete the project within the cost and schedule of the approved performance baseline? Is there adequate cost and schedule contingency to address the remaining risks?

3. Management: Is the project being properly organized, staffed, and managed for its successful execution? Are plans being developed for the transition to operations and for achieving optimal performance following project completion?

4. ES&H: Are ES&H aspects being properly addressed? Are Integrated Safety Management Principles being followed?

5. Prior Reviews: Has the project responded appropriately to the recommendations from previous reviews?