The Silicon Strip Detector
an overview and introduction

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SSD Location in STAR

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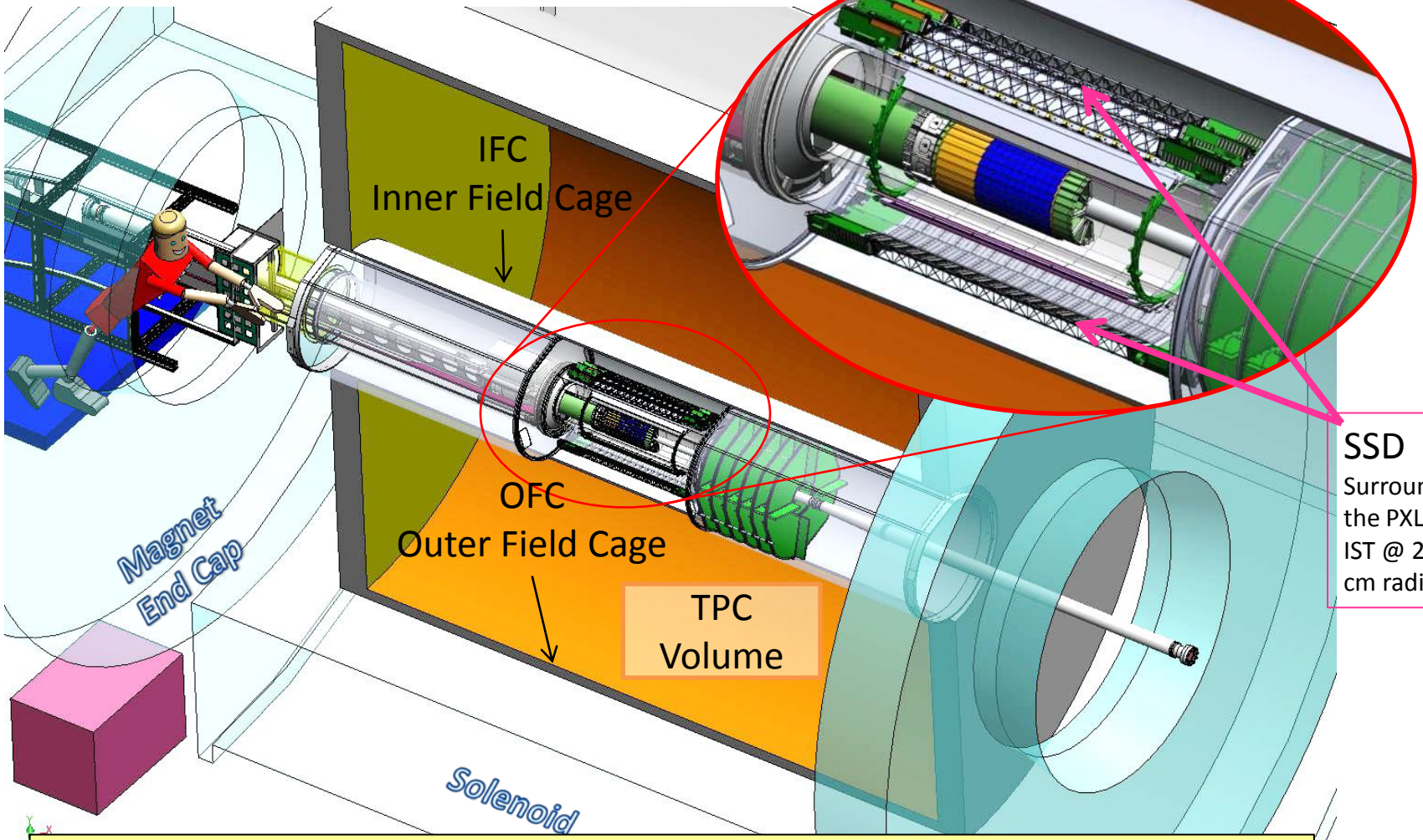

The SSD is an existing detector that needs an upgrade to meet HFT specs

Si Detectors Inside the TPC

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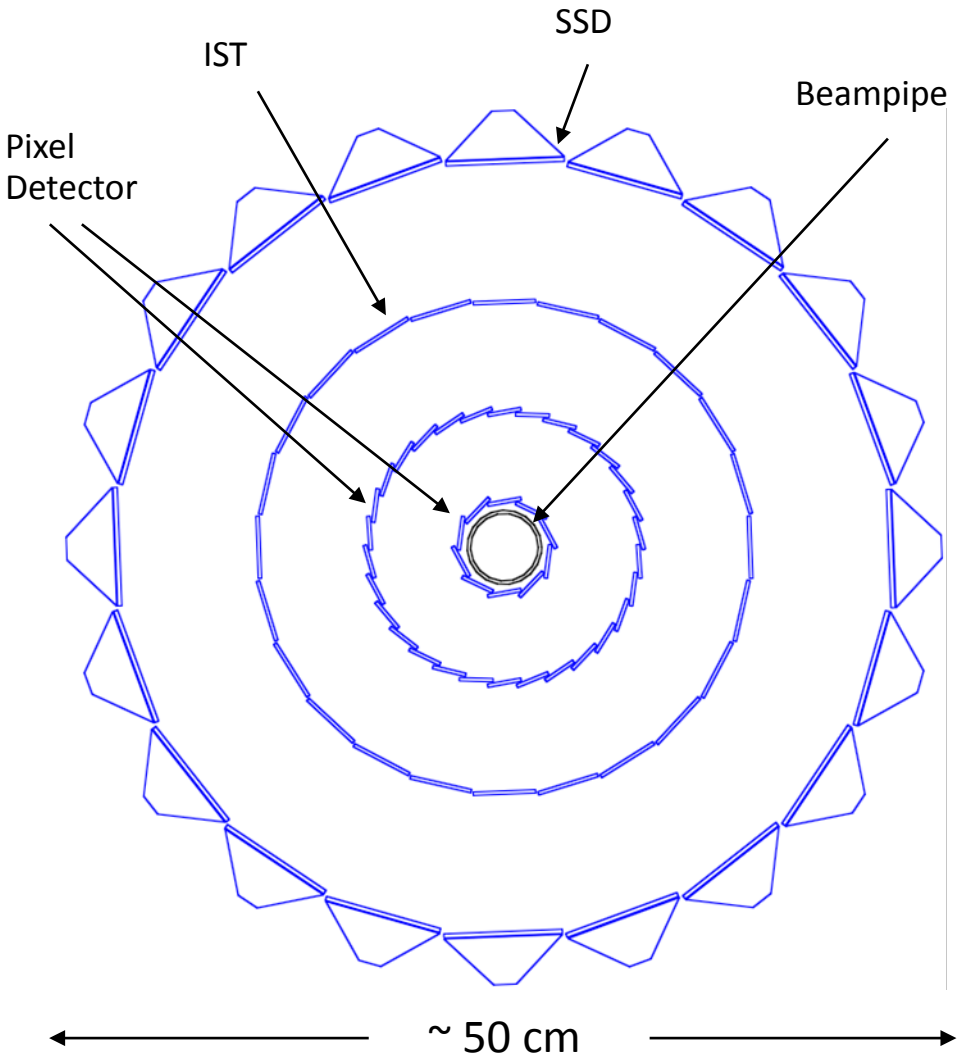
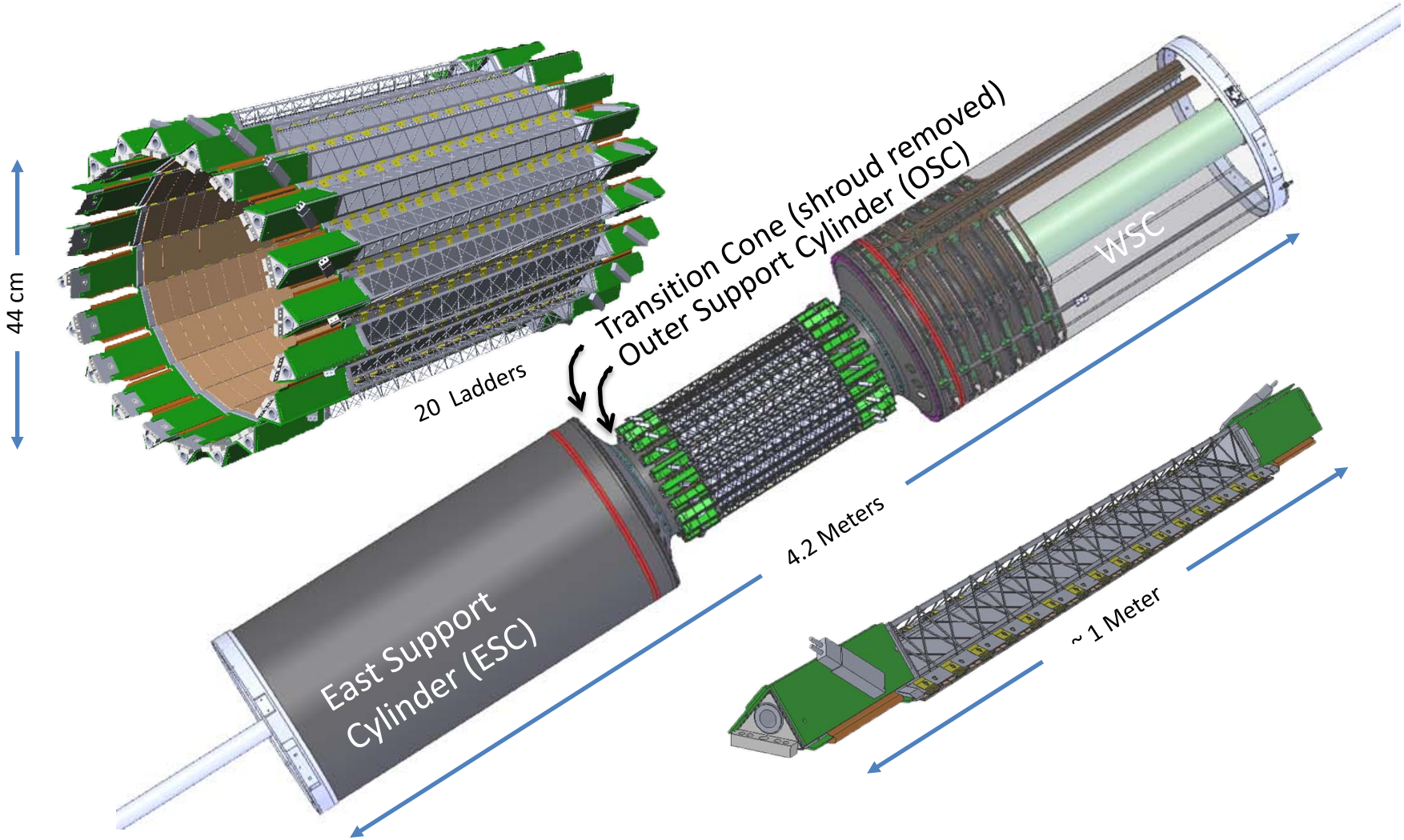
- **Goal: graded resolution and high efficiency from the outside → in**
- **TPC – SSD – IST – PXL**
- **TPC pointing resolution at the SSD is ~ 1 mm**
- **SSD pointing at the IST is ~ 400 μm ε = 0.98**
- **IST pointing at PXL 2 is ~ 400 μm ε = 0.98**
- **PXL 2 pointing at PXL1 is ~ 125 μm ε = 0.93**
- **PXL1 pointing at the VTX is ~ 40 μm ε = 0.94**

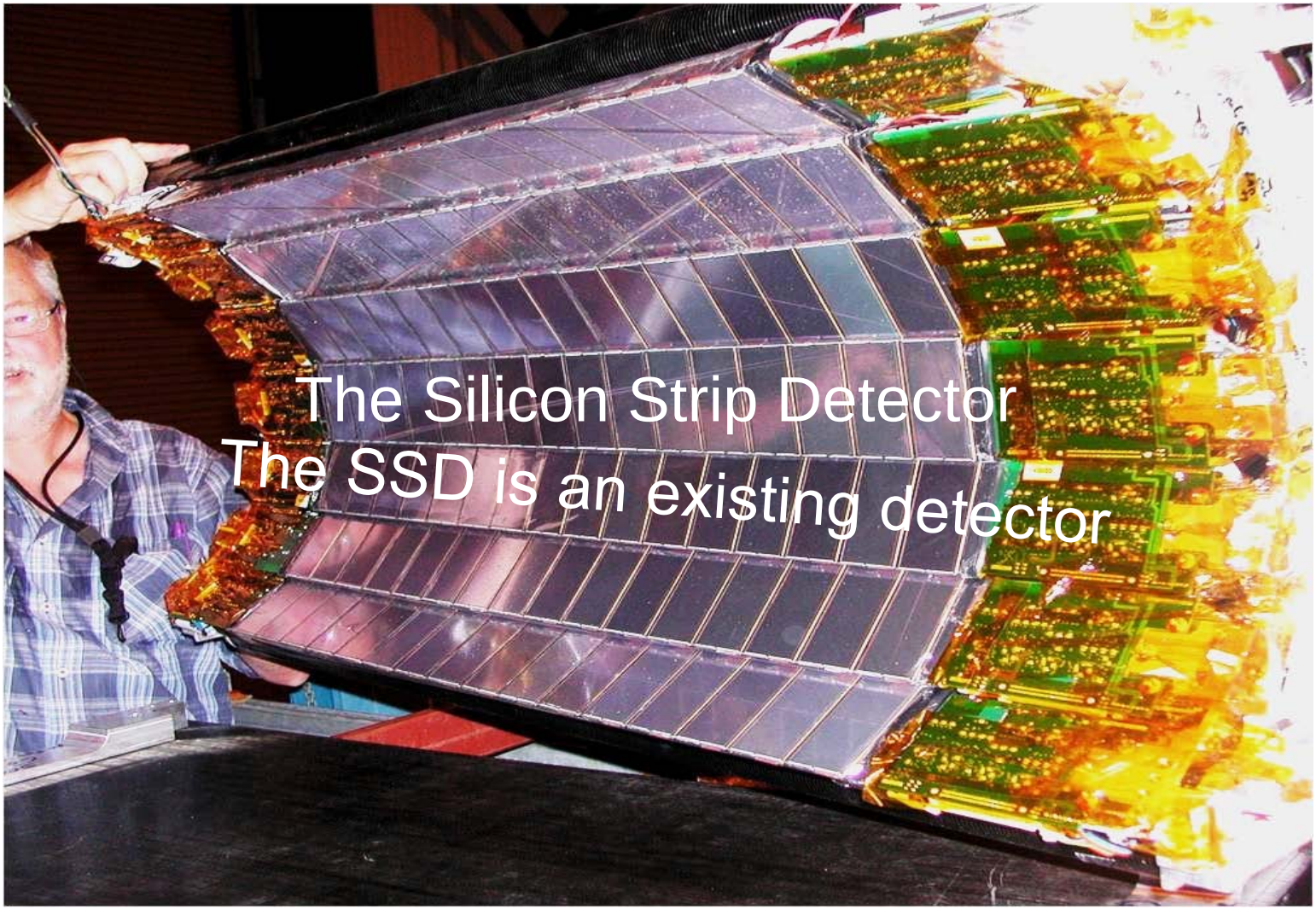


The challenge is to find tracks in a high density environment with high efficiency because a D^0 needs single track ε^2

SSD Overview and a few acronyms

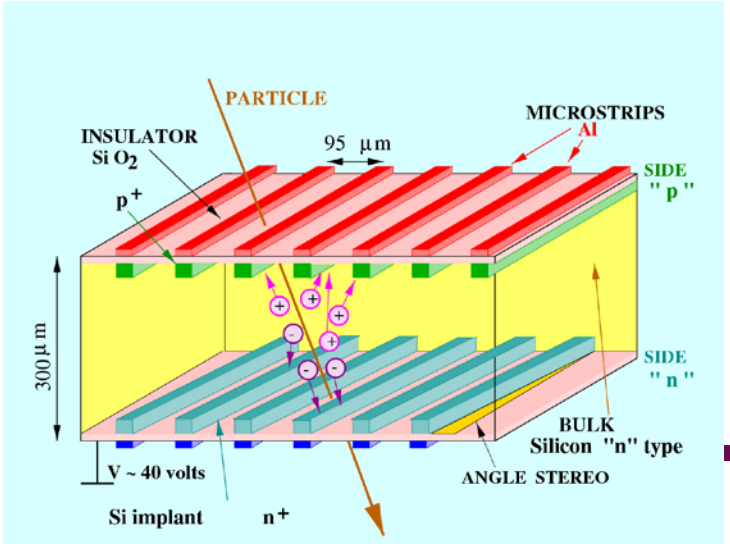


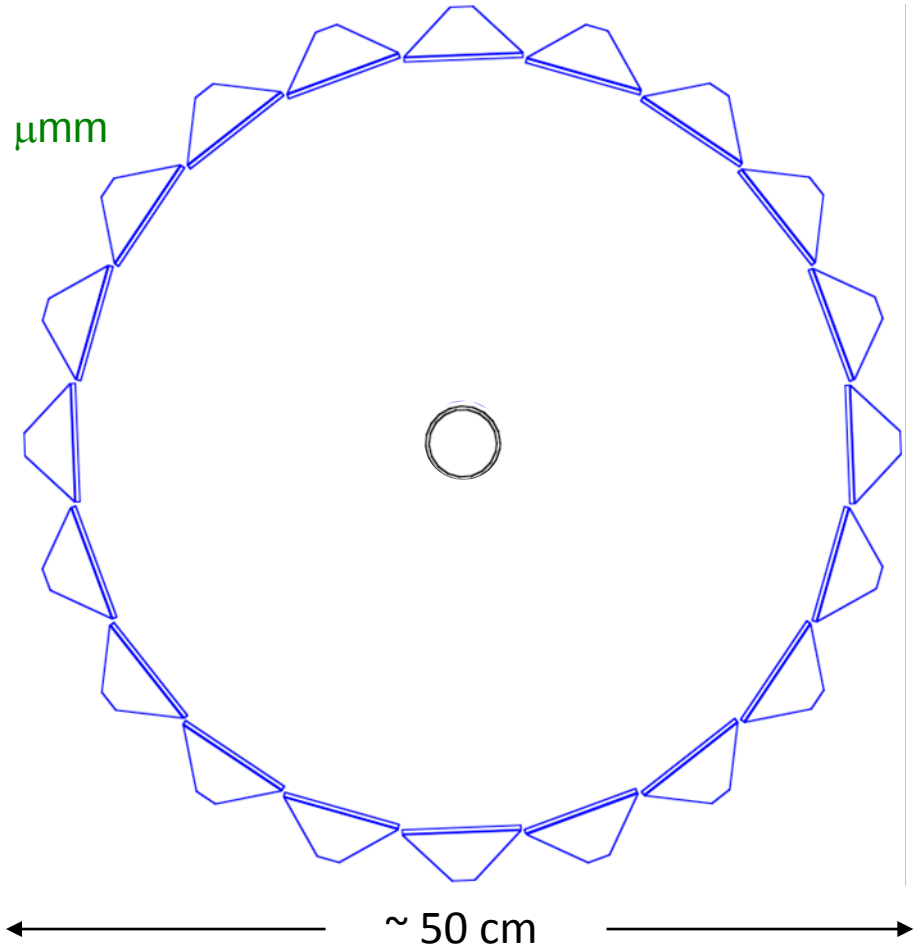
SSD



SSD Parameters

- Double sided Si wafers modules: 300 μm thick with 95 μm strips that are 4.2 cm long
  - 768 strips per side
  - Strips crossed at 35 mrad
    effective resolution 30 μm x 900 μmm
- One layer at 22 cm radius
  - 20 ladders, 67 cm long
  - 16 modules per ladder
- air cooled
- $|\eta| < 1.2$
- 1 % radiation length @ $\eta = 0$

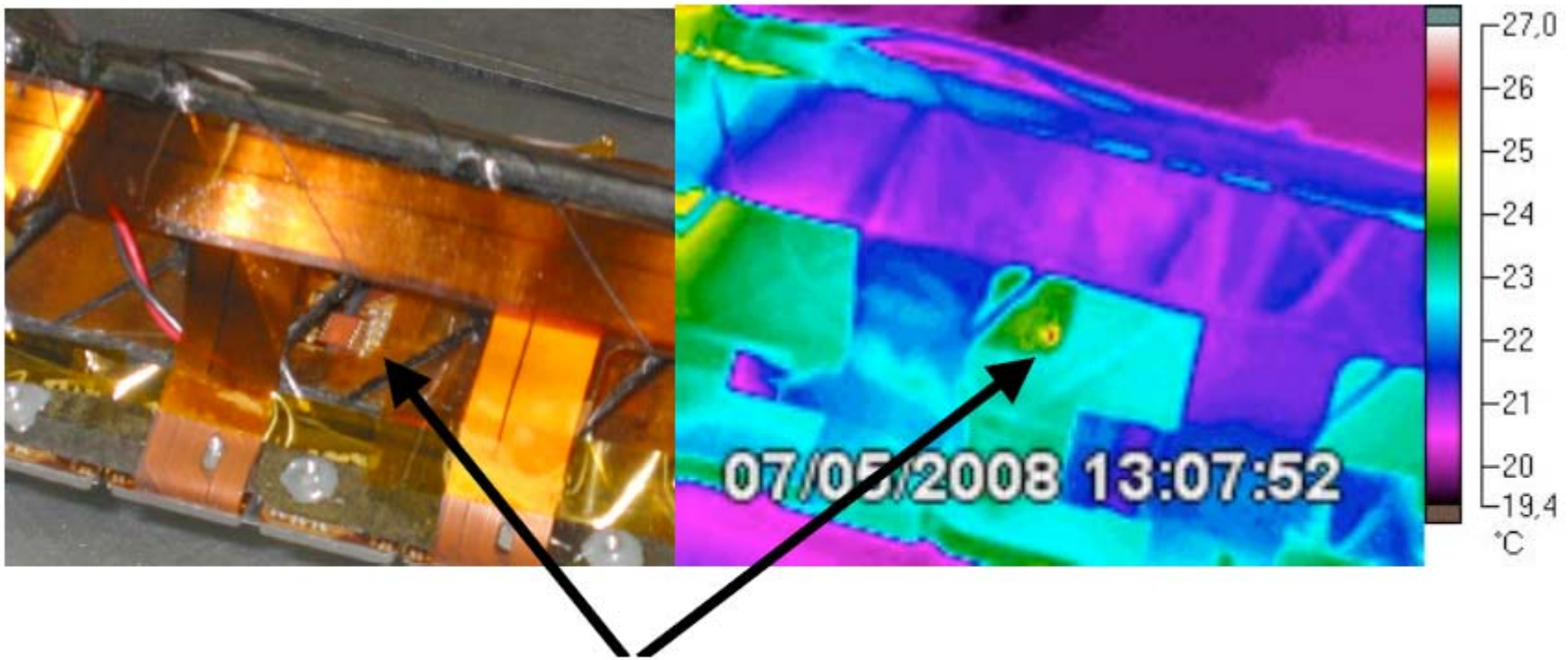




Status of the ladders

- The last run with the SSD was in 2007 … it wasn't a good run
  - cooling failures led to overheating and poor performance
  - perhaps related to this, there were several bias capacitors that failed on the modules. This caused 3 ladders to 'trip' frequently.
  - some ladder boards were damaged (ADC aging or other issues)
- Status in May of 2008
  - Six good ladders
  - Seven ladders with one bad hybrid (half module)
  - Nine ladders with several bad modules
  - bad ladder boards do not matter because we are going to replace them
- The ladders were refurbished in 2008 (see next page)
  - Now 94% of modules (on 20 ladders) are good
  - The modules & ladders have not be used since these repairs
- The ladders have not been operated since 2008

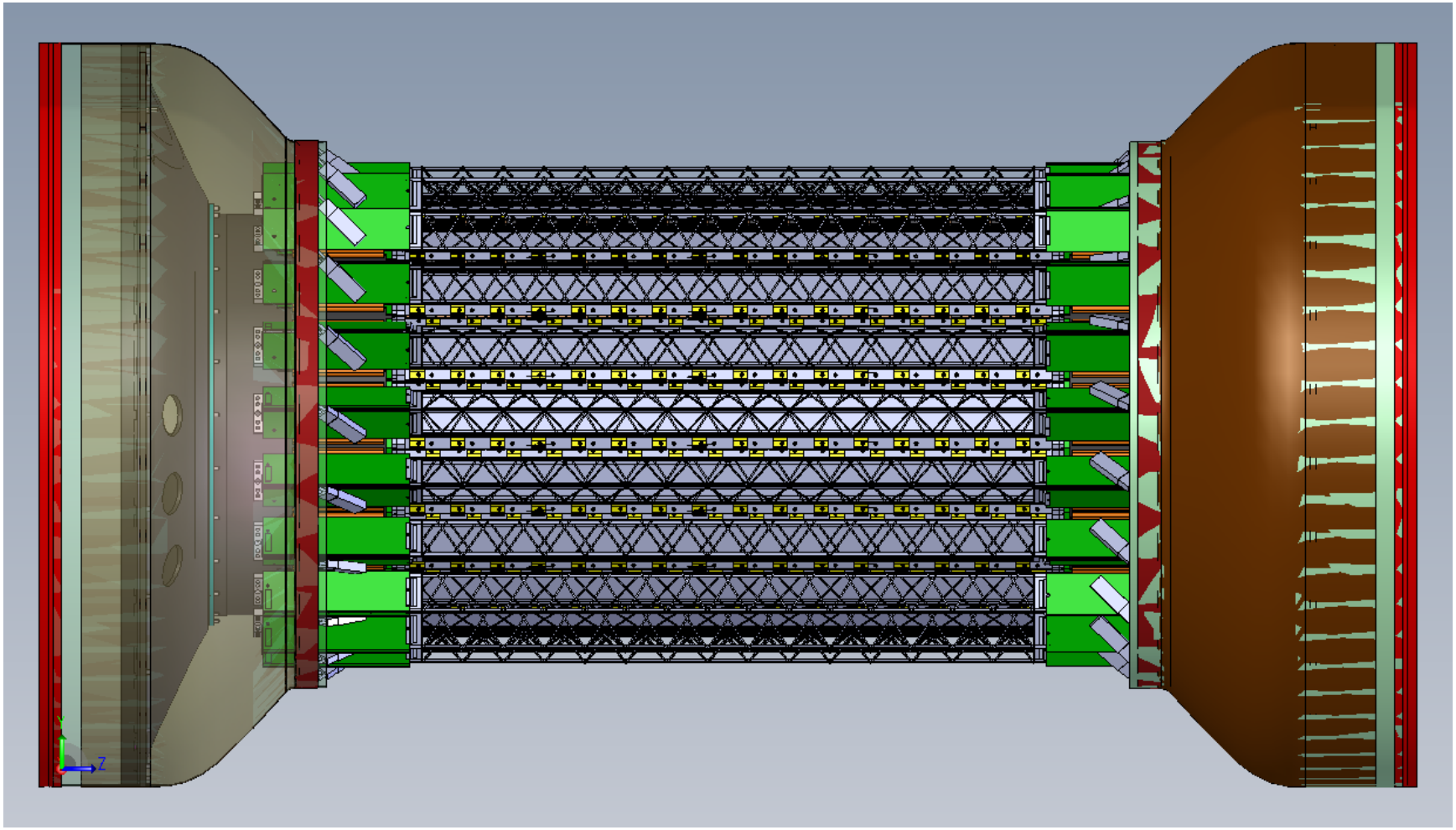
HV coupling capacitors were replaced



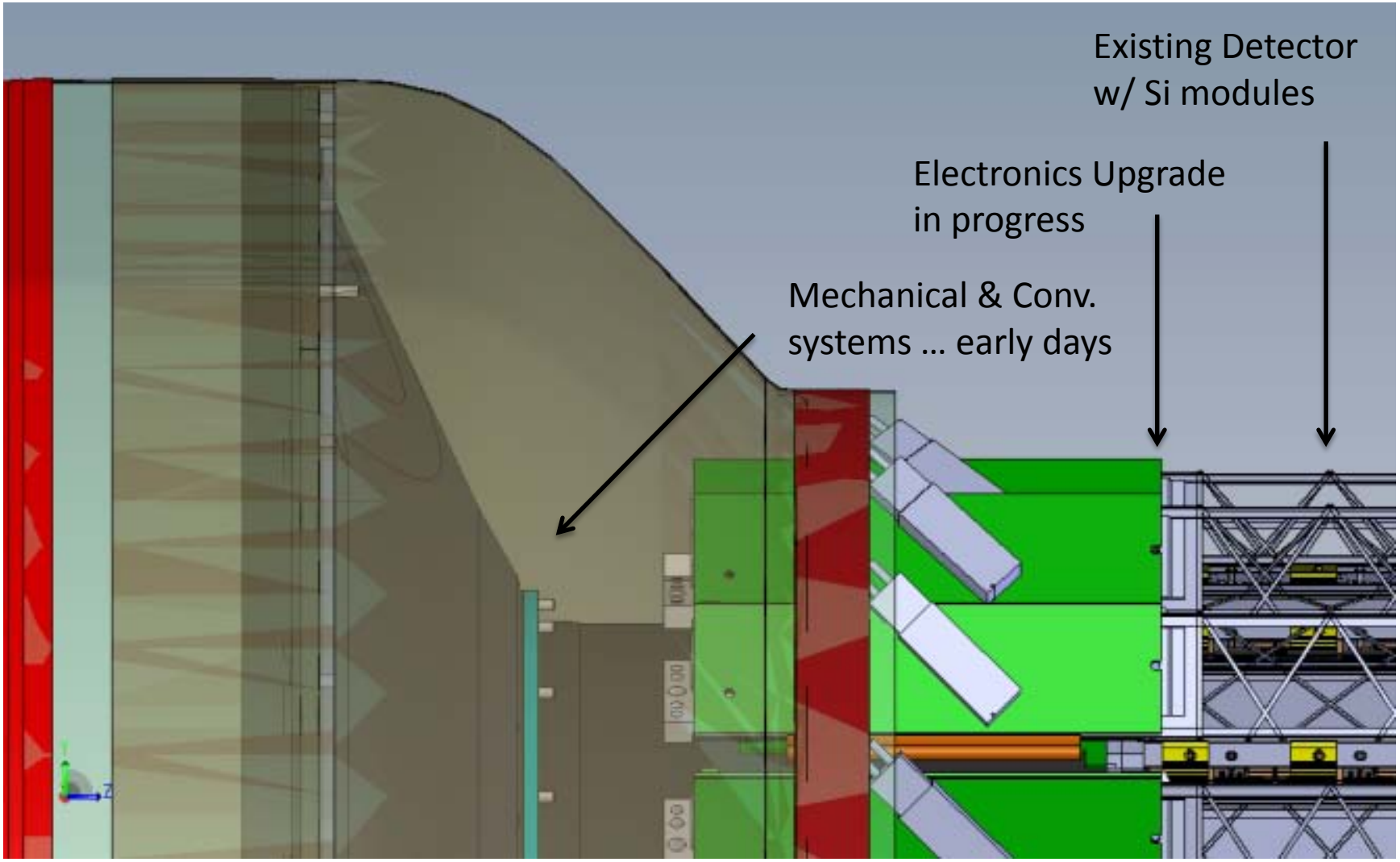
Leaking capacitor

A window has been opened in the kapton layer (dedicated to air flow) and after biasing the ladder (only the high voltage) one can see the leaking capacitor hotter than the other components on the hybrid circuit. The ladder was biased at 45V and the high voltage current was around 800μA.

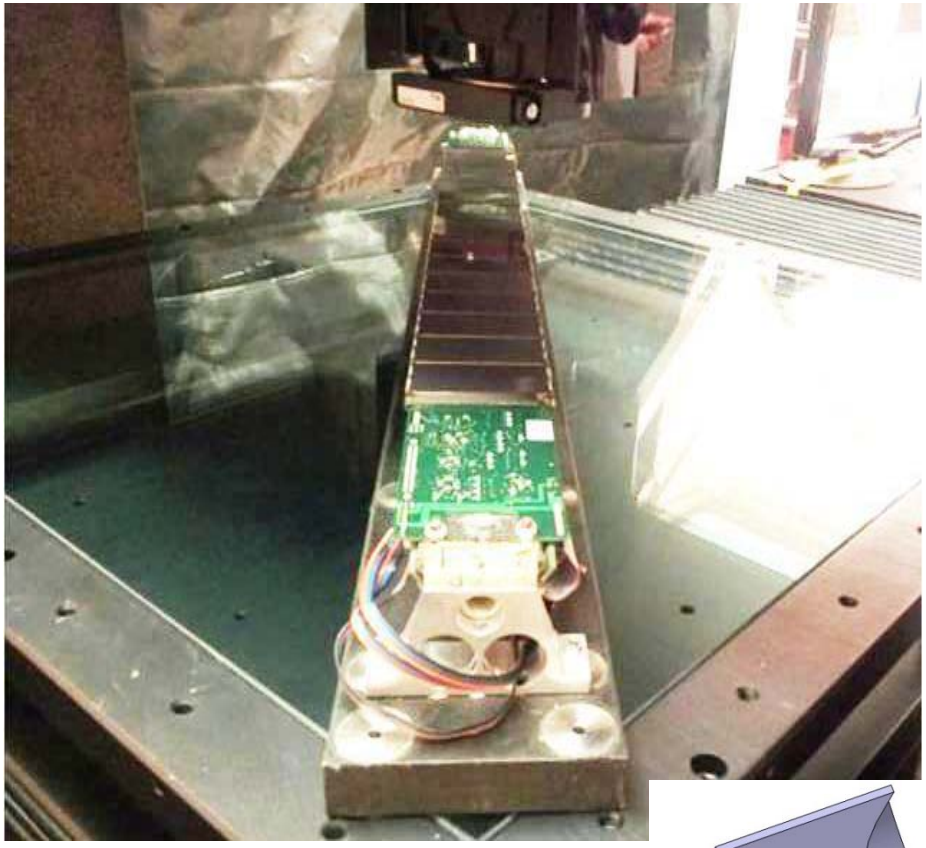
Schematic View of the new SSD



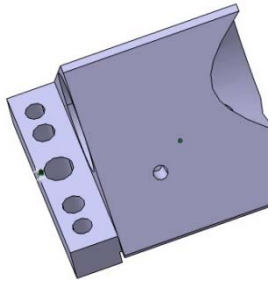
The SSD is an existing detector ⇒ upgrade

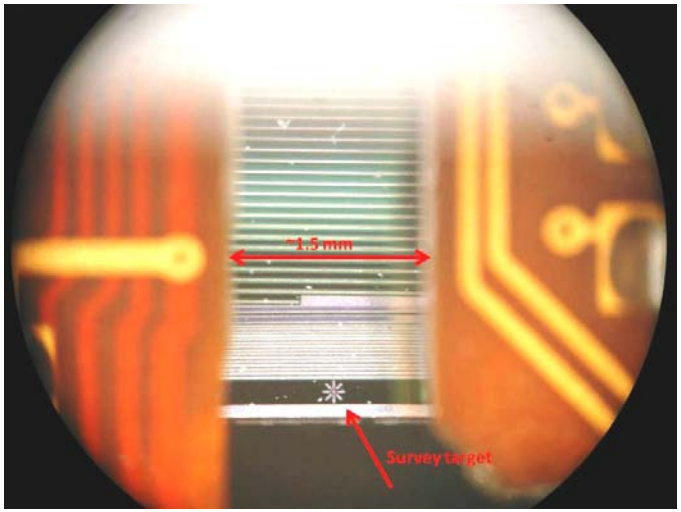


Progress: Ladder 0 is ready to be surveyed

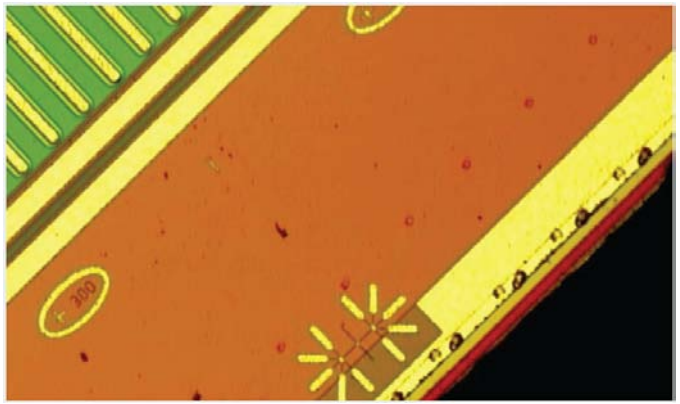


Reference point for survey and mounting on OSC



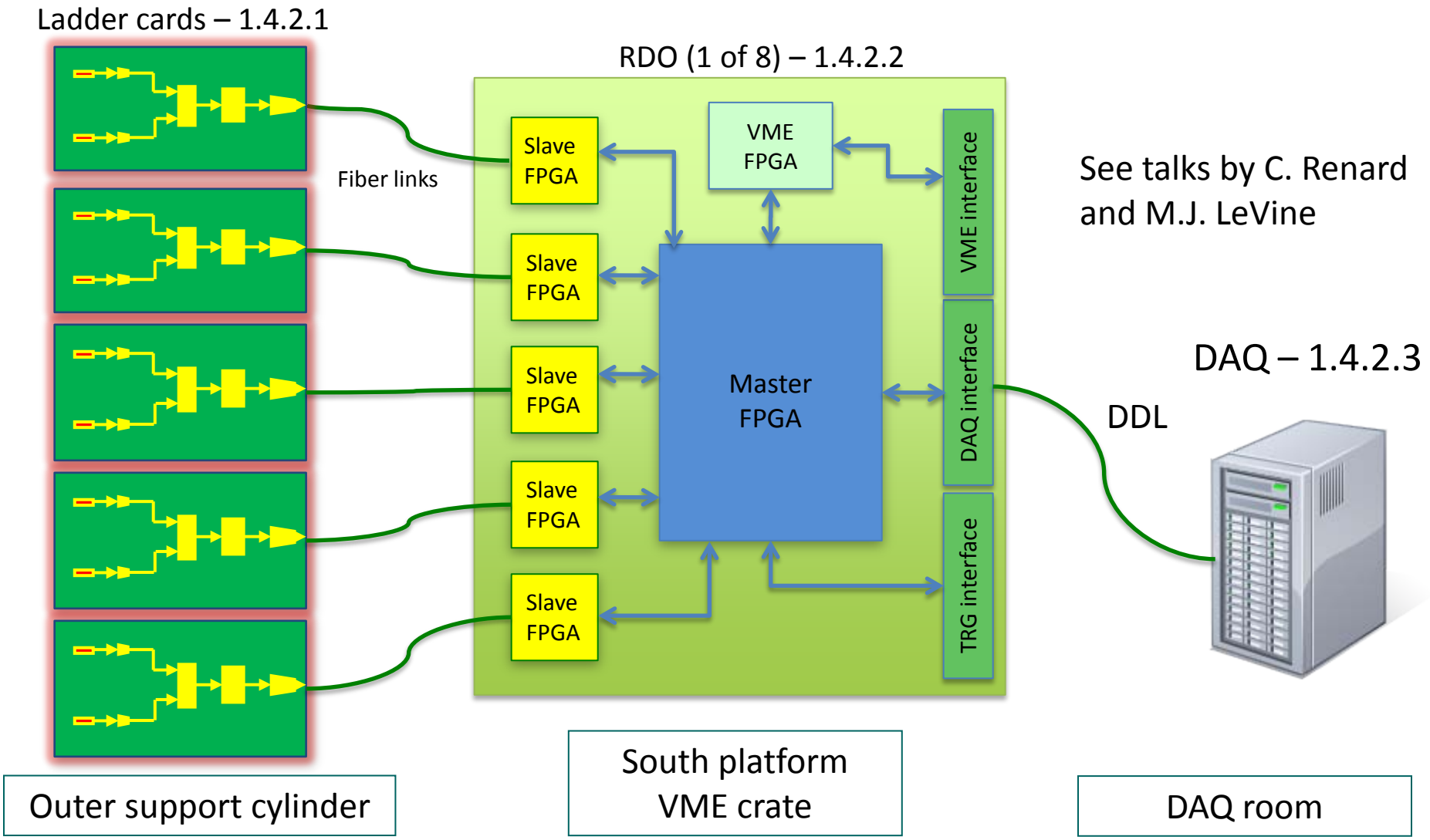


Target on end of wafer (backside)

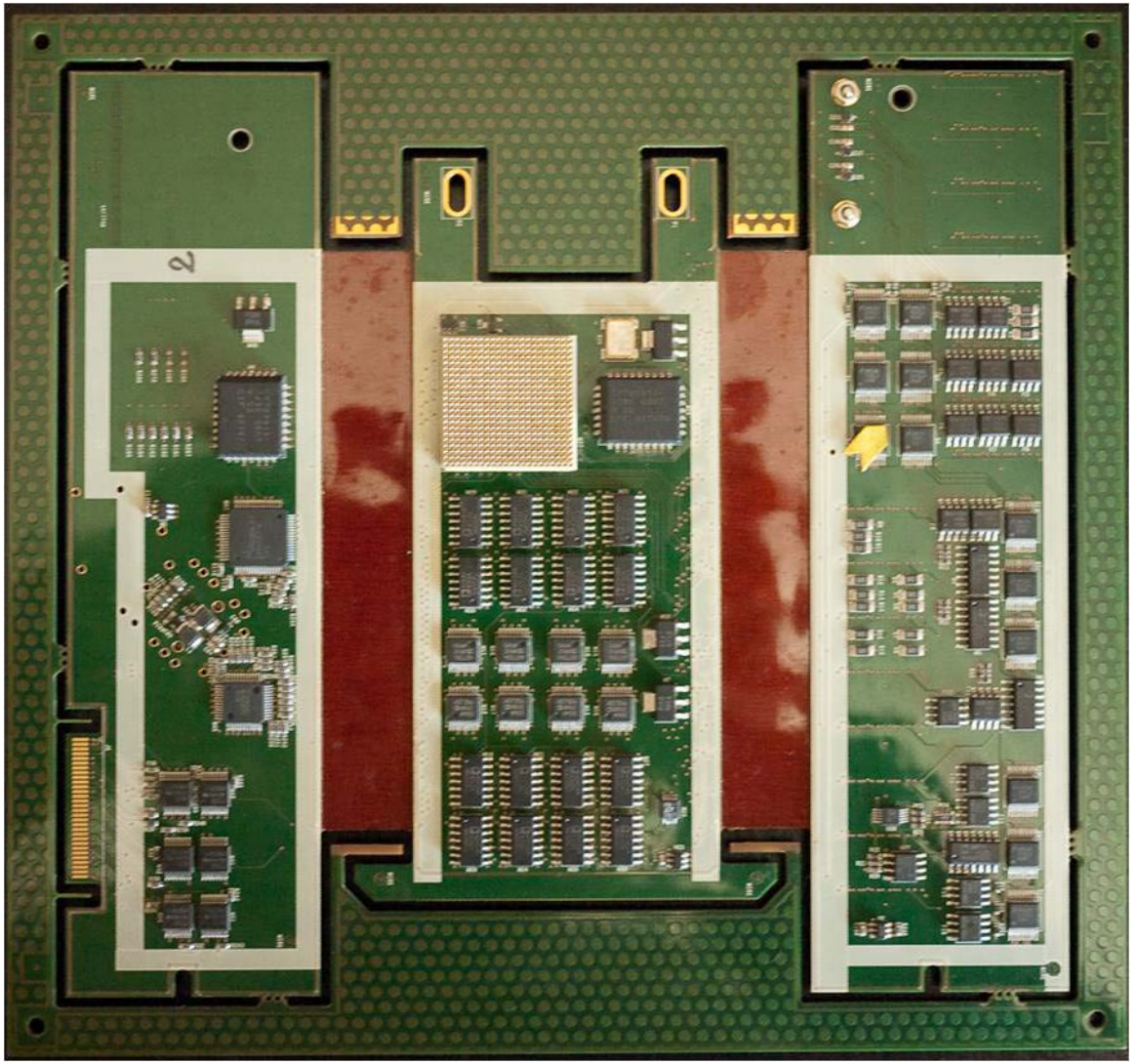


Targets on edges of wafer (front)

Readout Electronics – the heart of the upgrade



Progress: Ladder Card built and tested

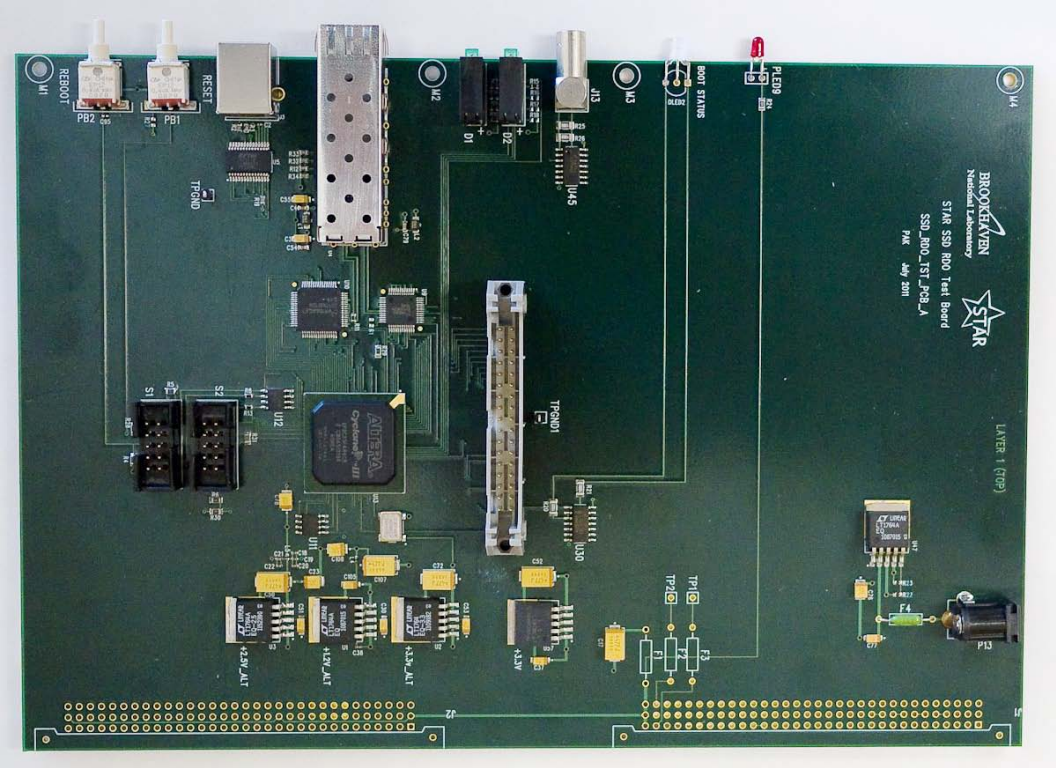


- Prototype with interposer card working since last summer
- FPGAADC – DAC test as voltage ref. for ADC
- A new layout has recently been completed and will be sent off for fabrication

  (see talk by C. Renard)
- Milestone:

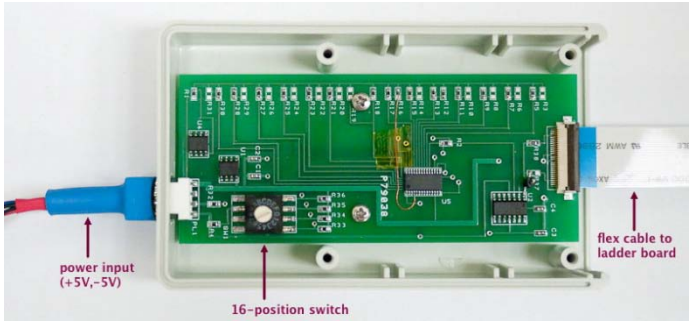
  Passing from prototype to pre-production version

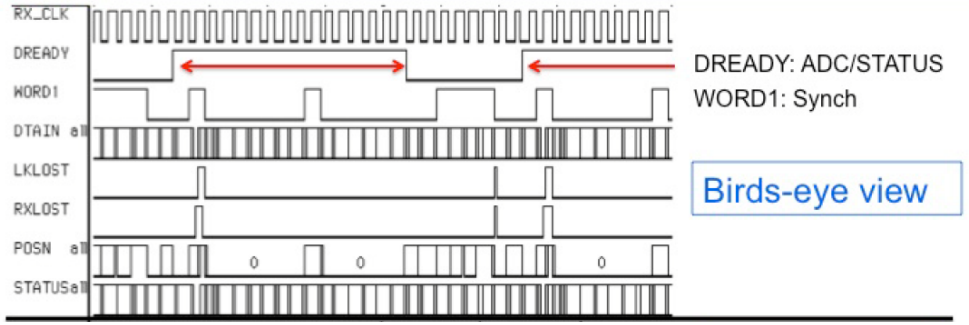
Progress: ‘Quick’ RDO built and tested



- Prototype RDO board w/services for 1 ladder
- A complete RDO board has recently been completed and sent off for fabrication
- Milestone:

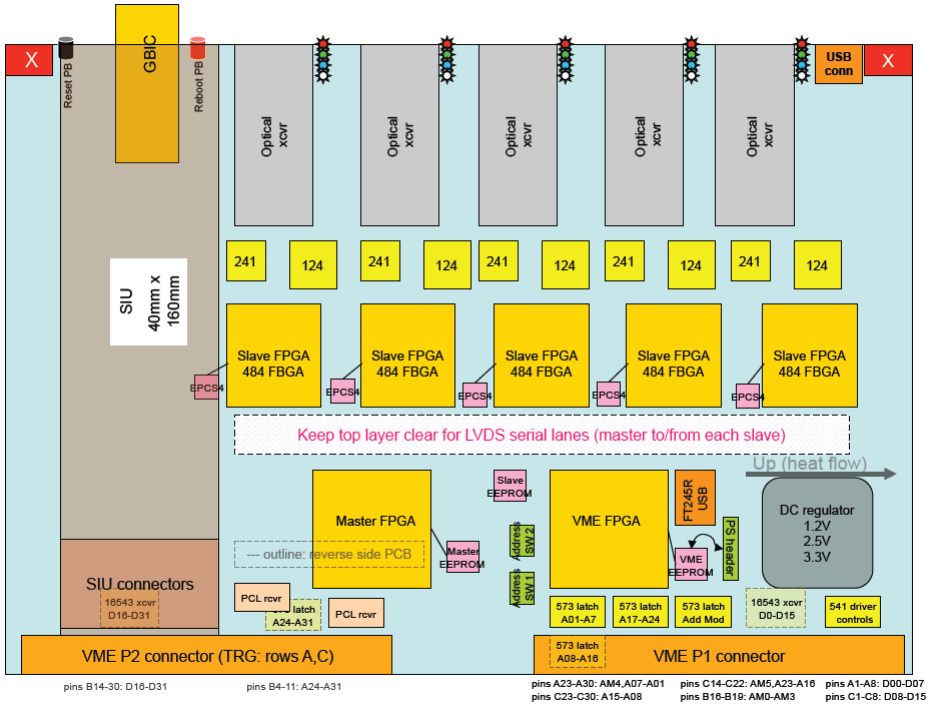
  Passing from prototype to pre-production version





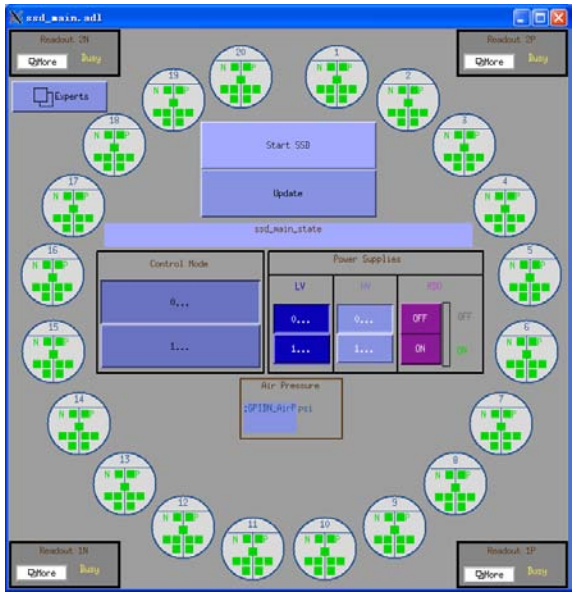
Progress: Readout Board Status (RDO)

- ✓Design of Slave FPGA complete
- ✓Pin outs for Master and VME FPGAs done
- ✓Full RDO board has been designed and laid out
- ✓ Components ordered
- Fab will begin in July

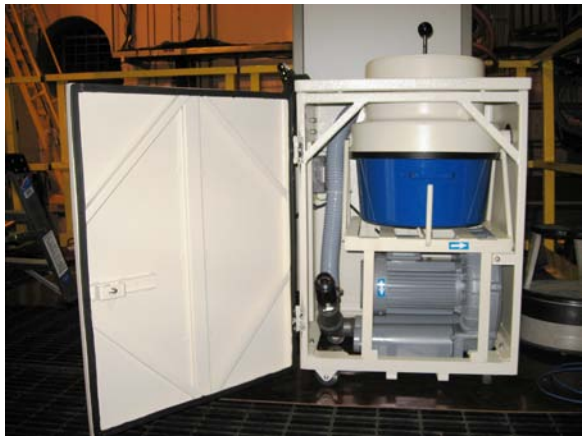


See talk by M.J. LeVine

Progress: Slow Controls and Conventional Systems



- We have developed a slow controls interface to the new Power supplies (See talk by Weihua Yan)
- Working on the more complex problem of JTAG communication to the ladders
- Prototype quantities of PS and Power modules are in-house
- Cooling system is in-house and has been tested.



Cooling system – vacuum

Instrumentation for cooling

Mechanical Engineering: the OSC & Shroud

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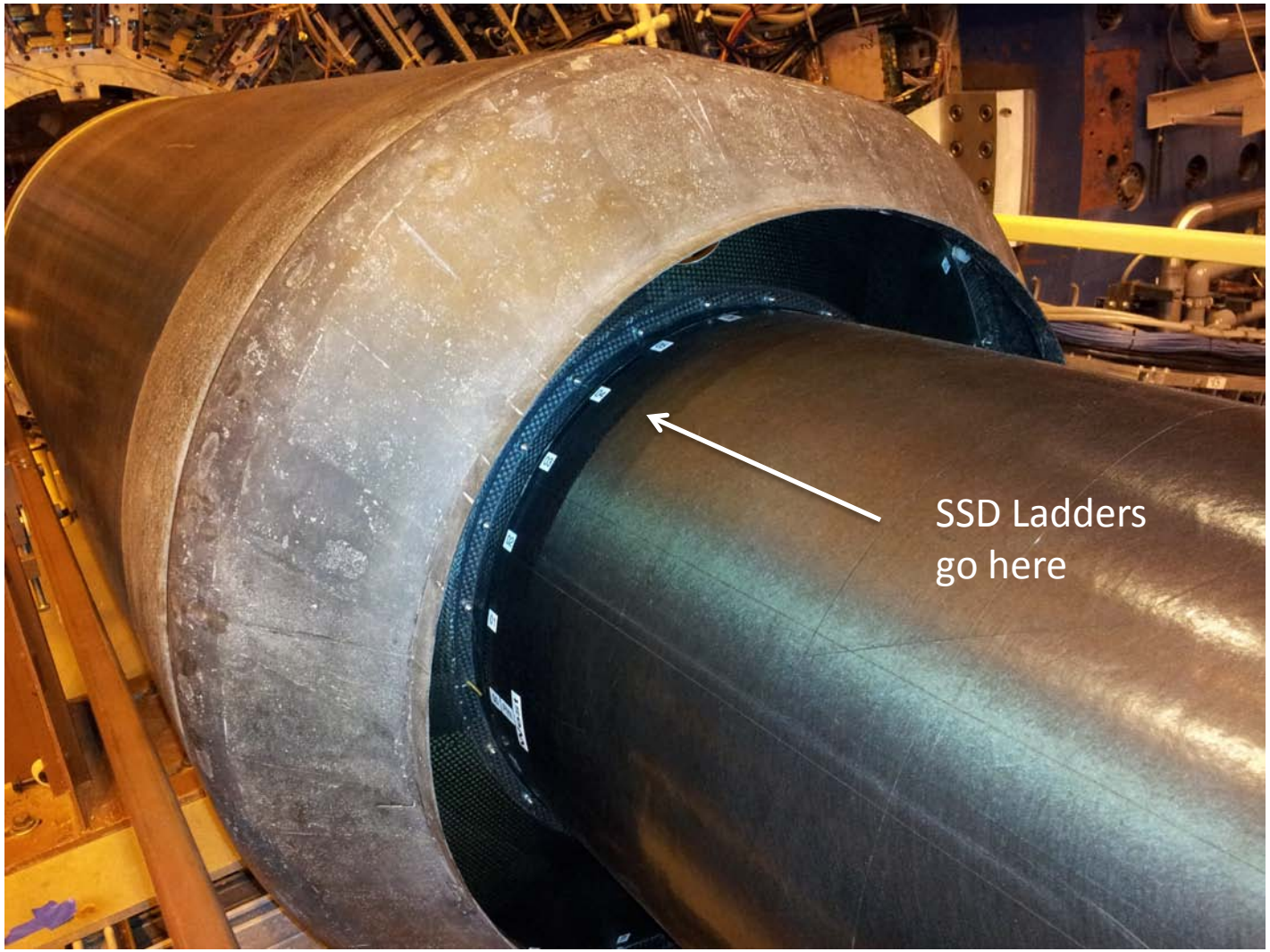
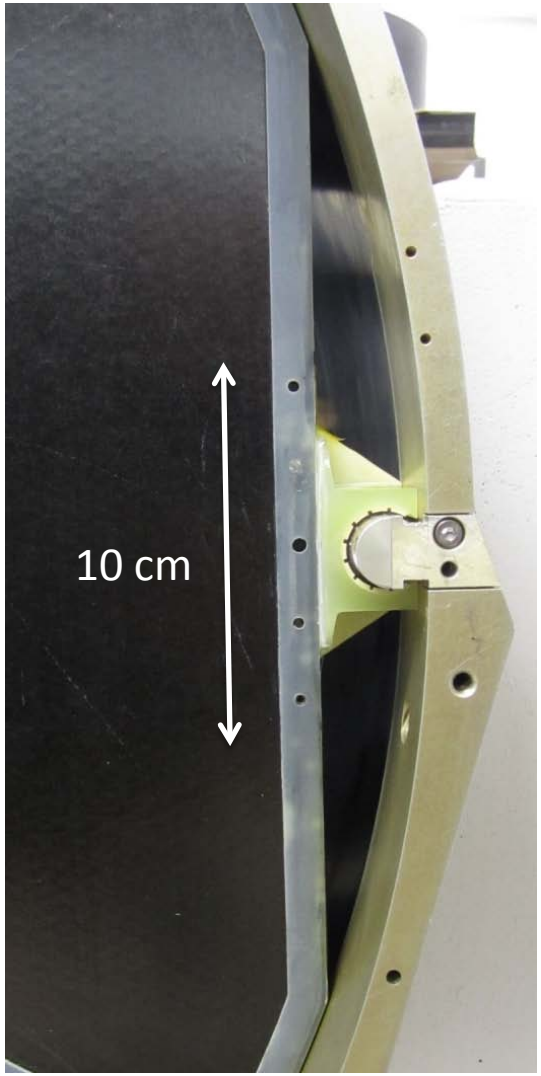
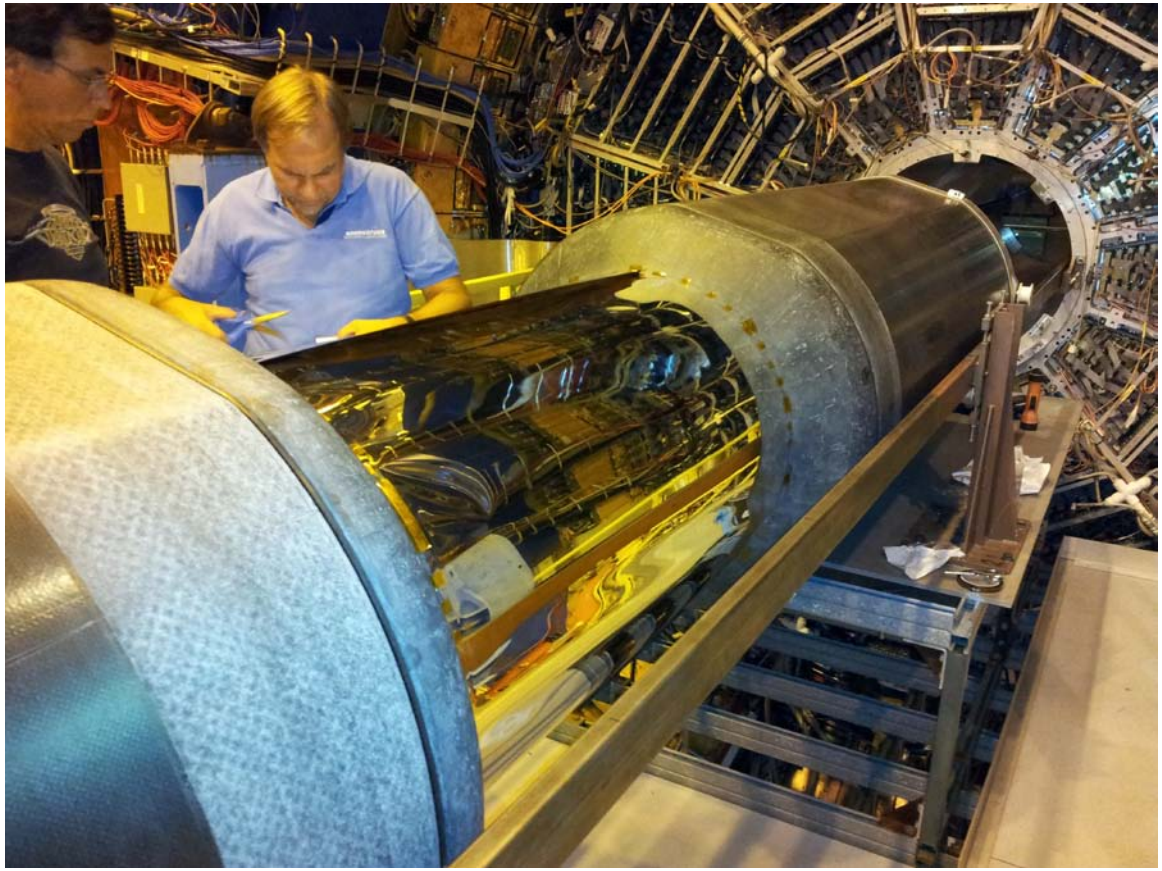


Progress: Mechanical Engineering





- Cable trays will be installed around FGT planes
- OSC with shroud and E&M shield installed
- SSD Specific work not yet complete

Milestones

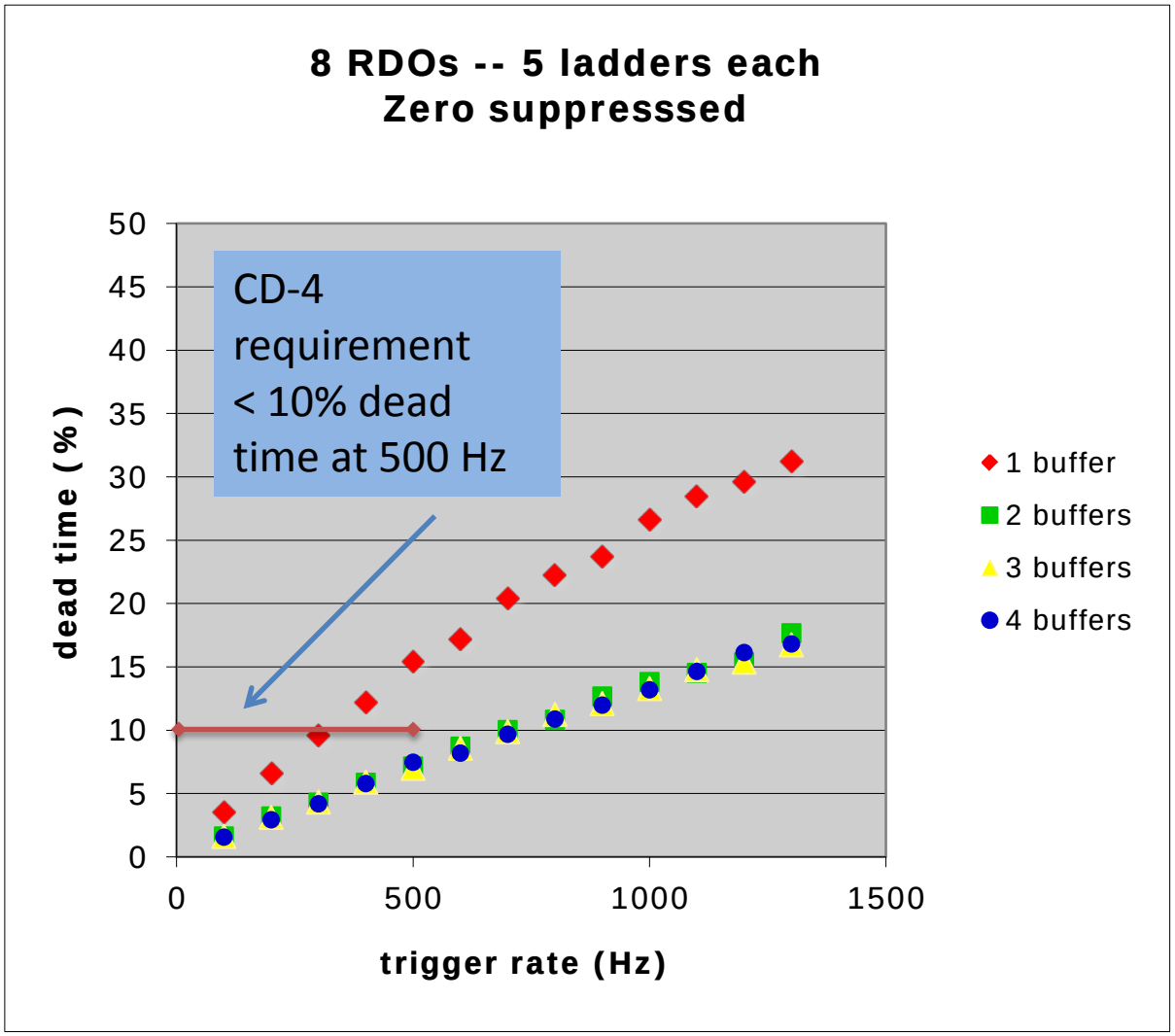
WBS	New Task Name	New Date	Old Date
1.4.2.1.1.2	L2 CP - SSD Prototype Ladder Board Design Finished	10/15/2010	10/15/2010
1.4.2.2.1.3	L2 CP - SSD QRDO Board design finished	7/19/2011	7/25/2011
1.4.2.2.1.7	L3 CP - QRDO Complete	8/23/2011	5/9/2011
1.4.2.1.1.9	L3 CP - Ladder Board Prototype Phase I Complete	10/31/2011	7/6/2011
1.4.4.1.1.2	L3 CP - PCB for Ladder Board Cable Ready for Fabrication	11/2/2011	9/2/2011
1.4.2.3.2.2	L3 CP - Production DAQ Design Review Completed	11/28/2011	11/28/2011
1.4.2.2.1.15	L3 CP - SSD RDO Design Finished	1/27/2012	
1.4.1.2	L3 CP - Mechanical Design of SSD components on OSC complete - HFT design Review to sign off	6/1/2012	6/1/2012
1.4.4.2.9	L3 CP - Power Supply Design Review Complete	6/29/2012	2/8/2012
1.4.2.2.2.4	L2 CP - SSD Preproduction Design Review of RDO	7/13/2012	5/30/2012
1.4.2.1.2.10	L3 CP - Preproduction Ladder Board PCB Received	8/10/2012	8/31/2012
1.4.2.1.3.2	L3 CP - Production Ladder Board Internal Review Completed	10/8/2012	10/29/2012
1.4.2.1.3.4	L2 CP - SSD Production of Ladder Boards Ready to Begin	11/6/2012	11/29/2012
1.4.2.1.3.7	L3 CP - Production Ladder Board PCB Received	1/22/2013	2/12/2013
1.4.4.4.2.12	L3 CP - Slow controls ready for testing	1/30/2013	4/18/2012
1.4.2.2.3.7	L3 CP - Production RDO Board Received	3/22/2013	2/6/2013
1.4.1.7	L3 CP - Mechanical Components on OSC Installed	4/1/2013	4/1/2013
1.4.2.5	L3 CP - Electronics Complete	6/14/2013	7/22/2013
1.4.3.1.5	L3 CP - Survey Complete	7/9/2013	5/30/2013
1.4.4.3.15	L3 CP - Installation of cooling on STAR platform and Magnet Endcap complete	8/16/2013	7/31/2013
1.4.3.2.7	L2 CP - SSD Assembled on OSC Ready for Installation	8/28/2013	7/1/2013

Complete
Future
Late

Project Requirements: CD-4 Deliverables

- Instrument 20 of the existing SSD ladders with new readout electronics compatible with STAR TPC readout
- SSD to be installed on the Outer Support Cylinder
- Provide cabling and cooling compatible with the IDS structure and FGT

SSD CD4 Requirements on Dead time



- Dead-time as a function of random trigger rate
  - Simulated performance with 3% occupancy
- The SSD will have 4 buffers as part of the firmware
- Multiple buffers hide the downstream DAQ from the dead-time of the system for randomly arriving triggers

Summary

- The SSD upgrade project is moving ahead rapidly
- We have a well developed prototype, test and fabrication plan
- We are just starting the fabrication of our pre-production LB and RDO boards
- The coming year will be dominated by fabrication of production electronics, mechanical engineering, software development and integrated testing.
- Resources necessary for the completion of the project are in hand and, for the most part, readily available
- The costs are under control.
- Keeping to schedule will be a challenge; including testing the new electronics on one ladder, as well as integrated testing of the full system at STAR.
- Our goal is to install the full SSD in time for Run 14 (2013-2014)

Backup Slides

Modifications Needed for the SSD Upgrade

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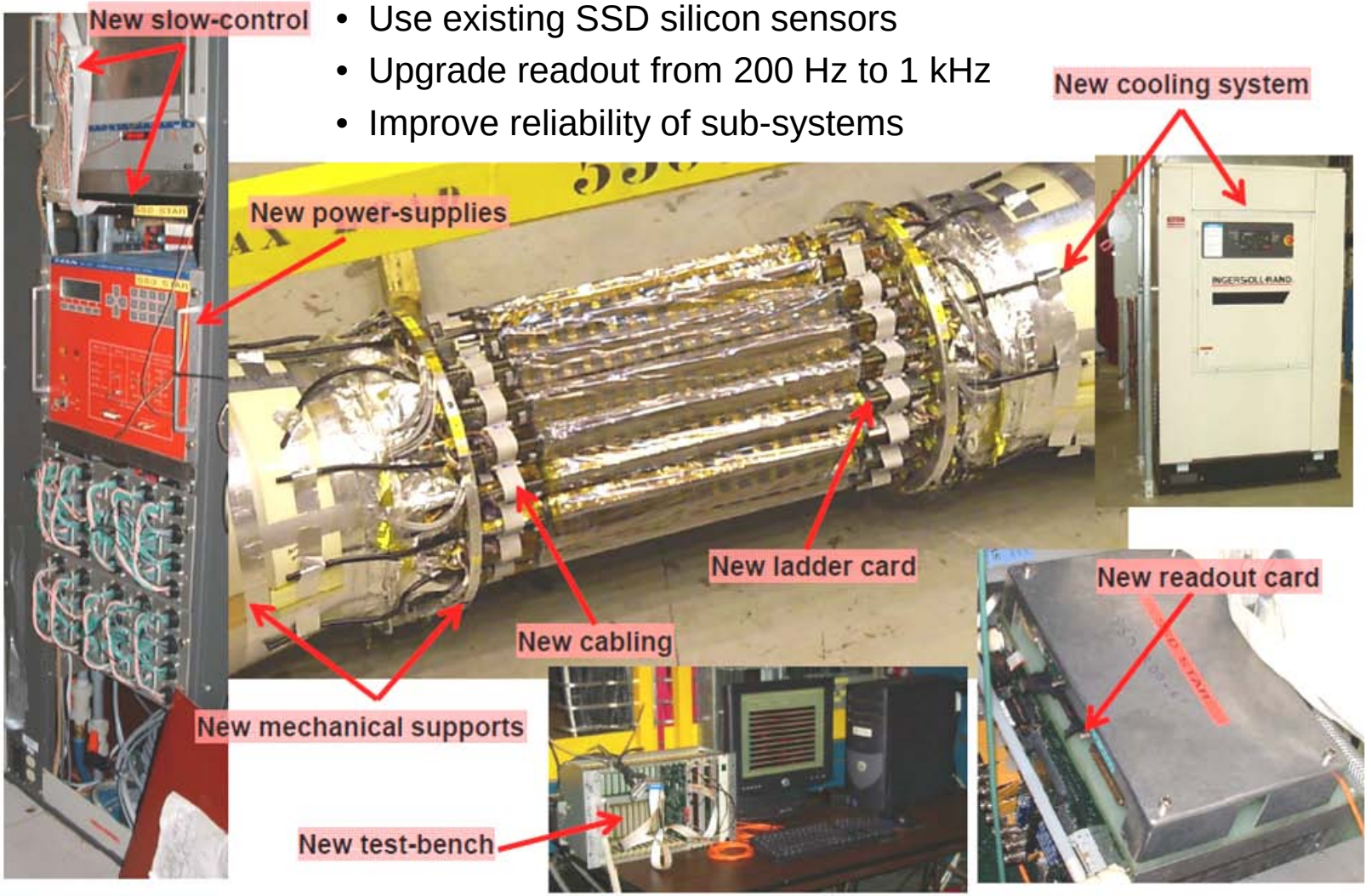
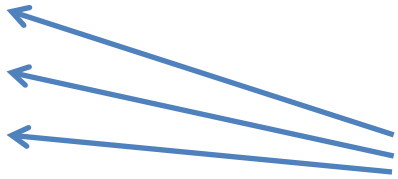
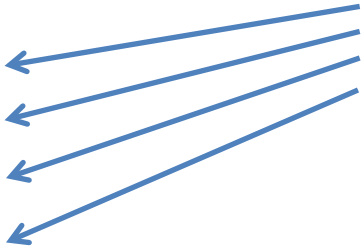
- Use existing SSD silicon sensors
- Upgrade readout from 200 Hz to 1 kHz
- Improve reliability of sub-systems



SSD WBS

- 1.4.1 Mechanics
- 1.4.2 Electronics
  - 1.4.2.1 Ladder Board
  - 1.4.2.2 RDO Board
  - 1.4.2.3 DAQ Board
- 1.4.3 Detector Assembly
  - 1.4.3.1 Survey
  - 1.4.3.2 OSC Assembly
- 1.4.4 Infrastructure
  - 1.4.4.1 Cables
  - 1.4.4.2 Power Supply
  - 1.4.4.3 Cooling
  - 1.4.4.4 Slow Controls
  - 1.4.4.5 FPGA Software





The Work Breakdown Structure reflects the elements shown on the previous page

We kept the SSD, it is a beautiful detector!

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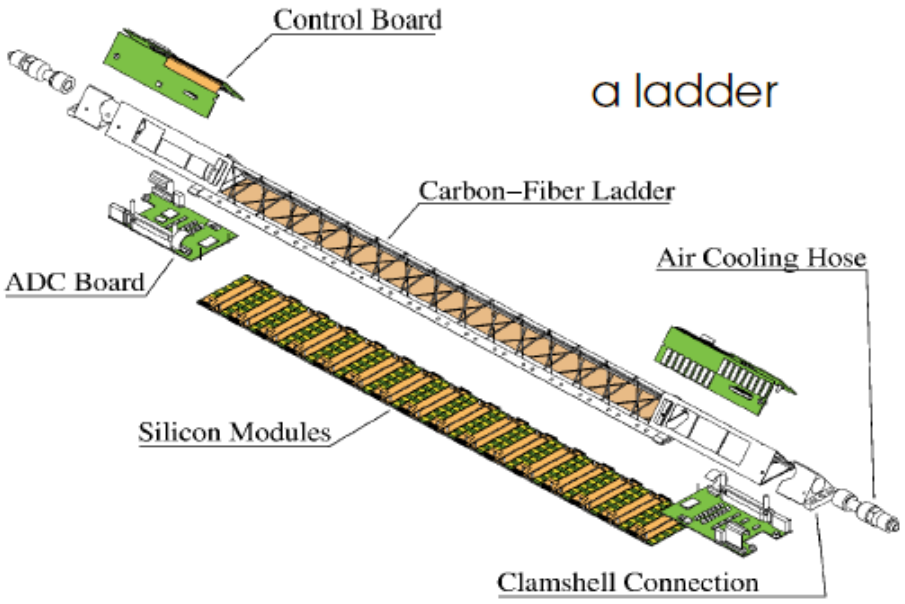

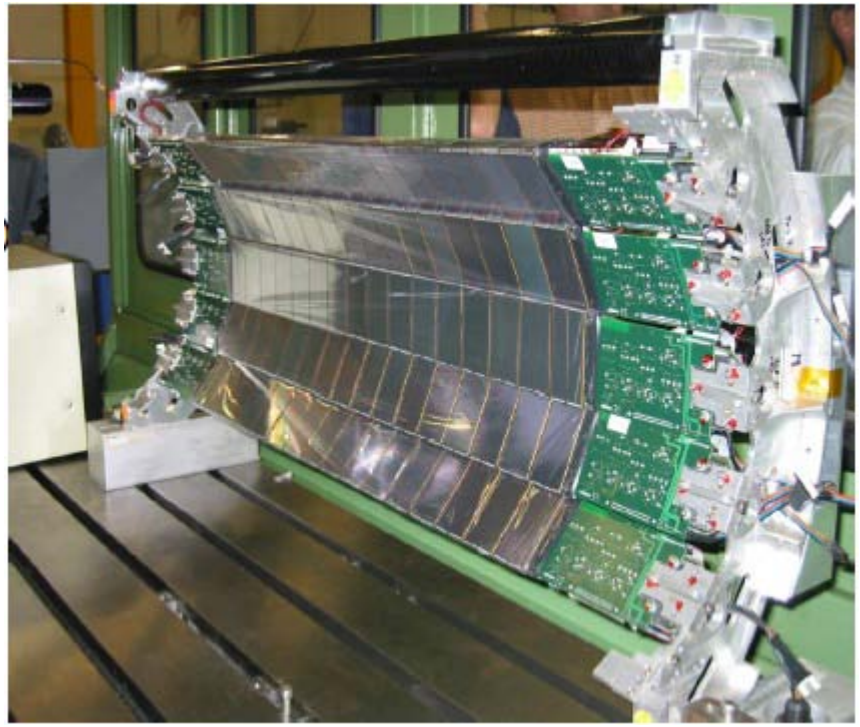

- The SSD is thin
  - 1% - double sided Si
- The SSD lies at an ideal radius
  - 22 cm - midway between IP and IFC
- The SSD has excellent resolution
  - (rumor says better than design)
- Replacing the SSD was not an option
  - too expensive

Getting a Boost from the TPC

- The TPC provides good but not excellent resolution at the vertex
  - ~ 1 mm
- The TPC provides an excellent angular constraint on the path of a predicted track segment
  - This is very powerful. It gives a parallel beam with the addition of MCS from the IFC
- The best thing we can do is to put a pin-hole in front of the parallel beam track from the TPC
  - This is the purpose of the SSD and IST
- The SSD and IST do not need extreme resolution. Instead, they maintain the parallel beam and don't let it spread out
  - MCS limited
  - The PXL does the rest of the work