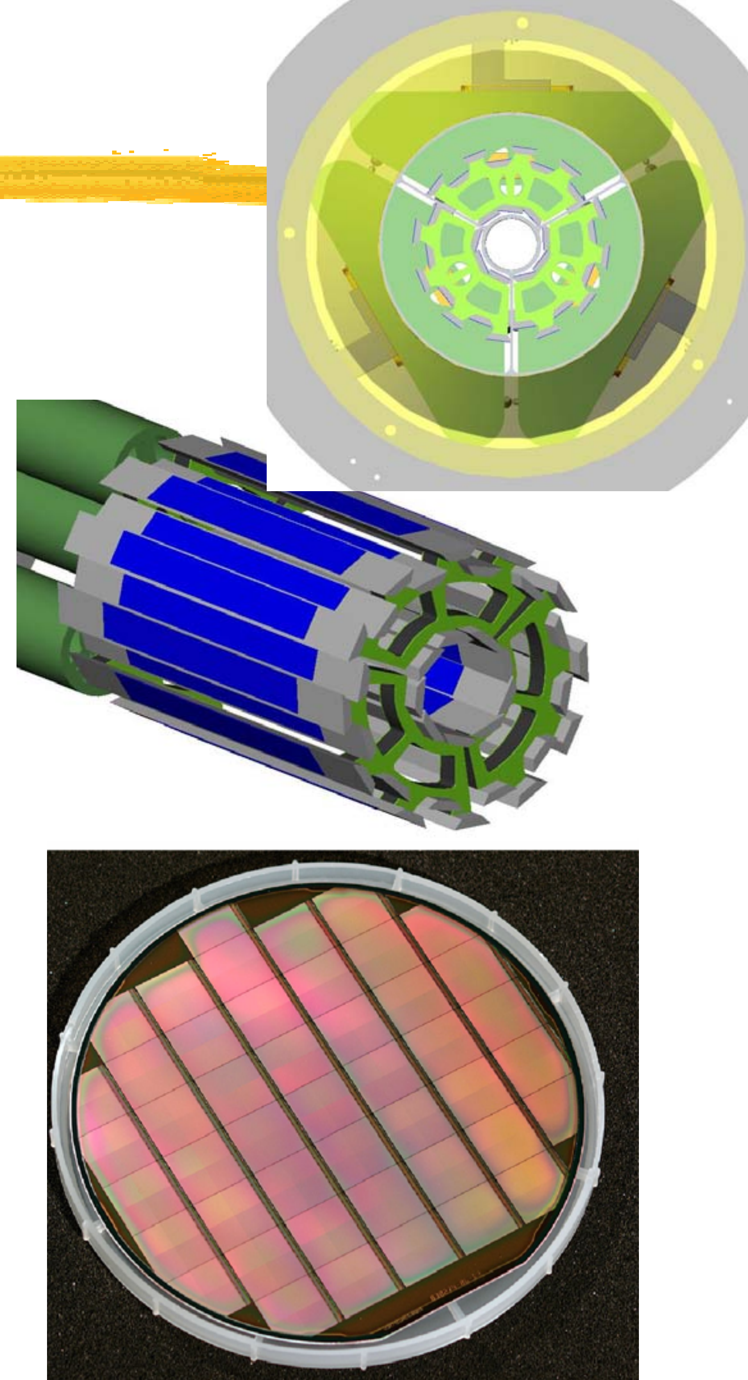
Wieman
RNC
LBNL

Jan 2007
DAC review

Topics, mechanical

- The challenge
- Mechanical Concept (2 cm beam pipe)
  - Simplified concept for support arms
- Thermal studies
- Run 7 MIMOSTAR2 telescope in STAR, mechanical aspects
  - Covered in detail by Michal Szelezniak
  - Detector Verification in STAR Environment
  - Measure small radius track density

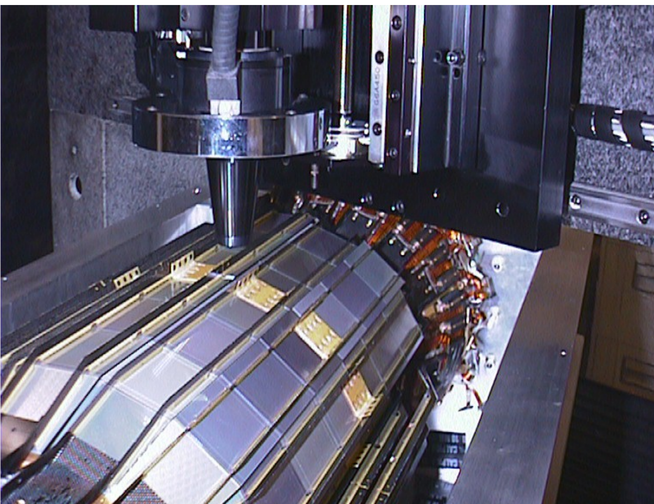


- MIMOSTAR 2 Latch up and Upset tests
- Chip development
- Ultra
- The future for pixels, exciting new opportunities

Some HFT features (the challenge)

Pointing resolution	$(13 \oplus 12\text{GeV}/p \cdot c)$ μm
Layers	Layer 1 at 2.5 cm radius Layer 2 at 6.5 cm radius
Pixel size	30 μm X 30 μm
Hit resolution	8.7 μm
Position stability	10 μm
Radiation thickness per layer	$X/X0 = 0.28\%$
Beam pipe radiation thickness	$X/X0 = 0.14\%$
Number of pixels	135 M
Integration time (affects pileup)	R&D phase 4 ms Final detector 0.2 ms
Rapid installation and replacement	Reproducible positioning

HFT Mechanical requirements



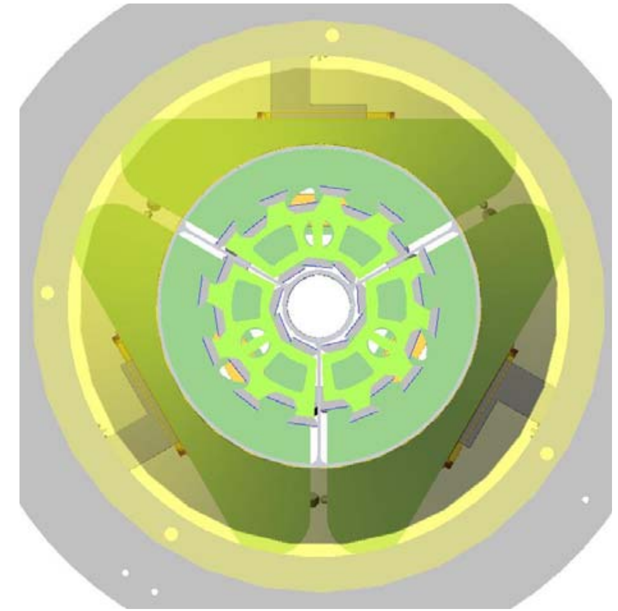
(mapping of BarBar with visual coordinate machine)

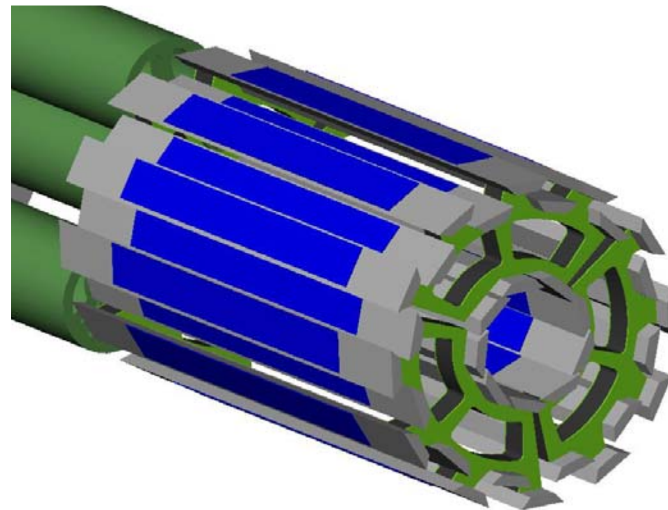
Full self consistent spatial mapping prior to installation

Installation and removal does not disturb mapping

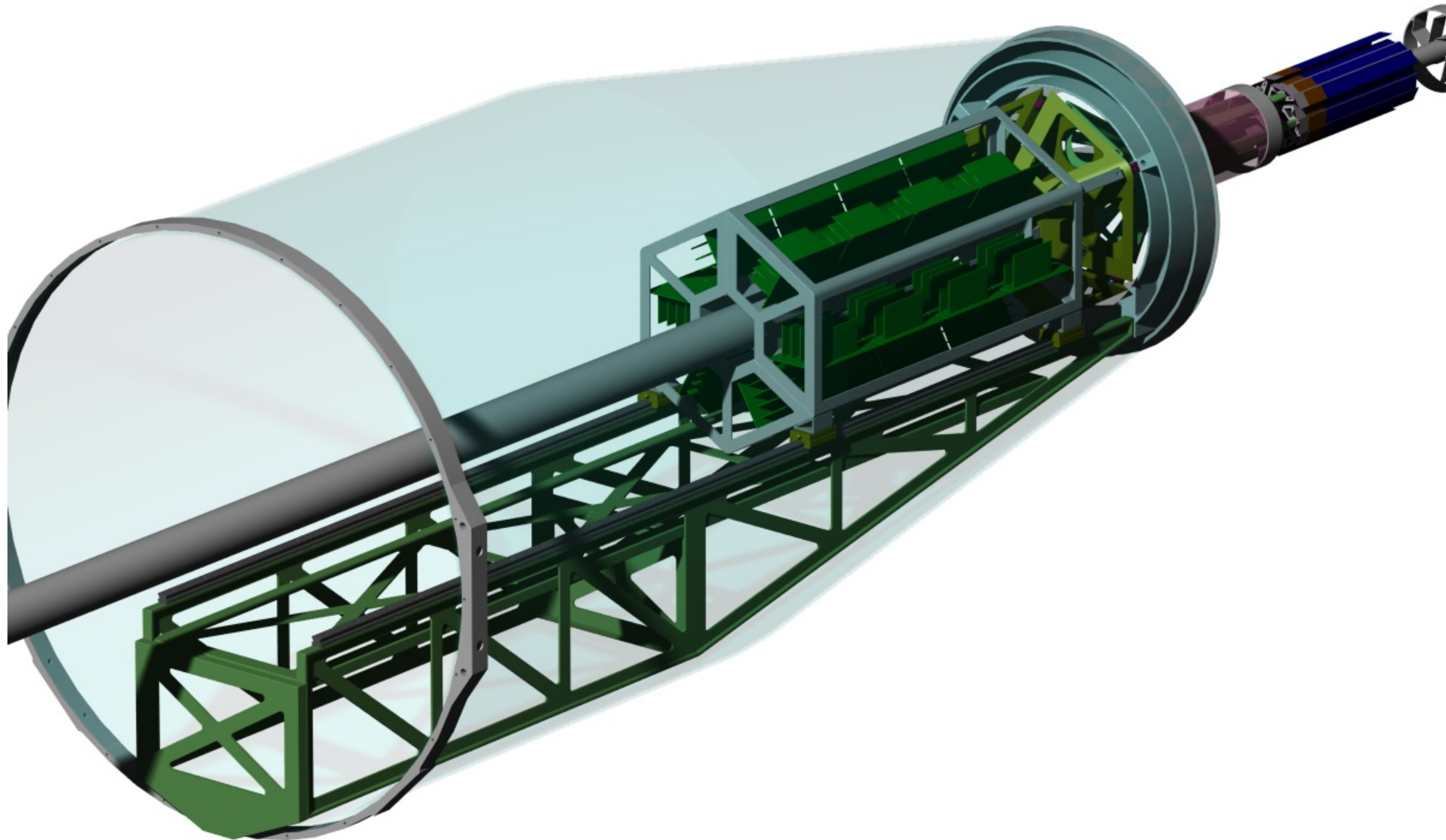
Rapid replacement

10 Micron stability

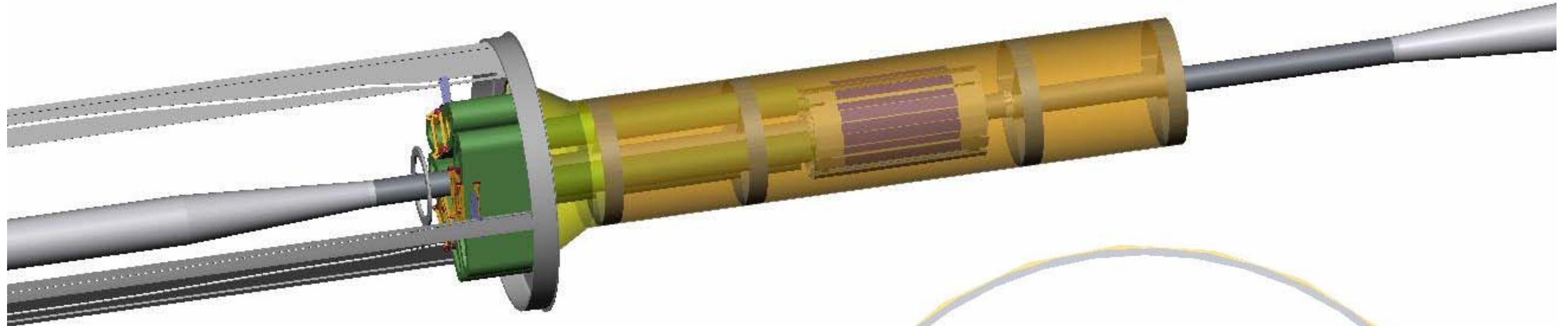


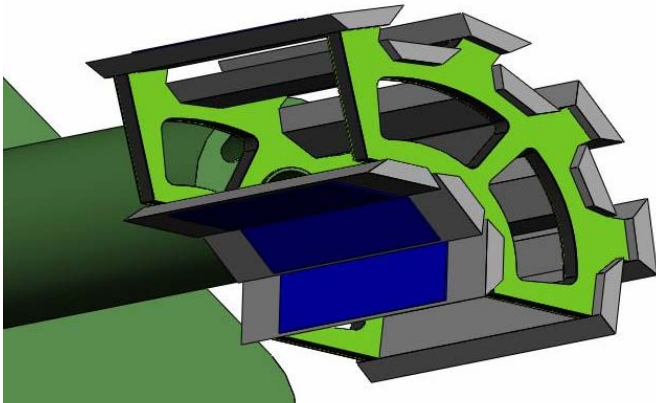


Conceptual mechanical design



2 cm radius beam pipe option





Simplified support concept for ease of analysis and construction

End view

2.5 cm

Inner layer

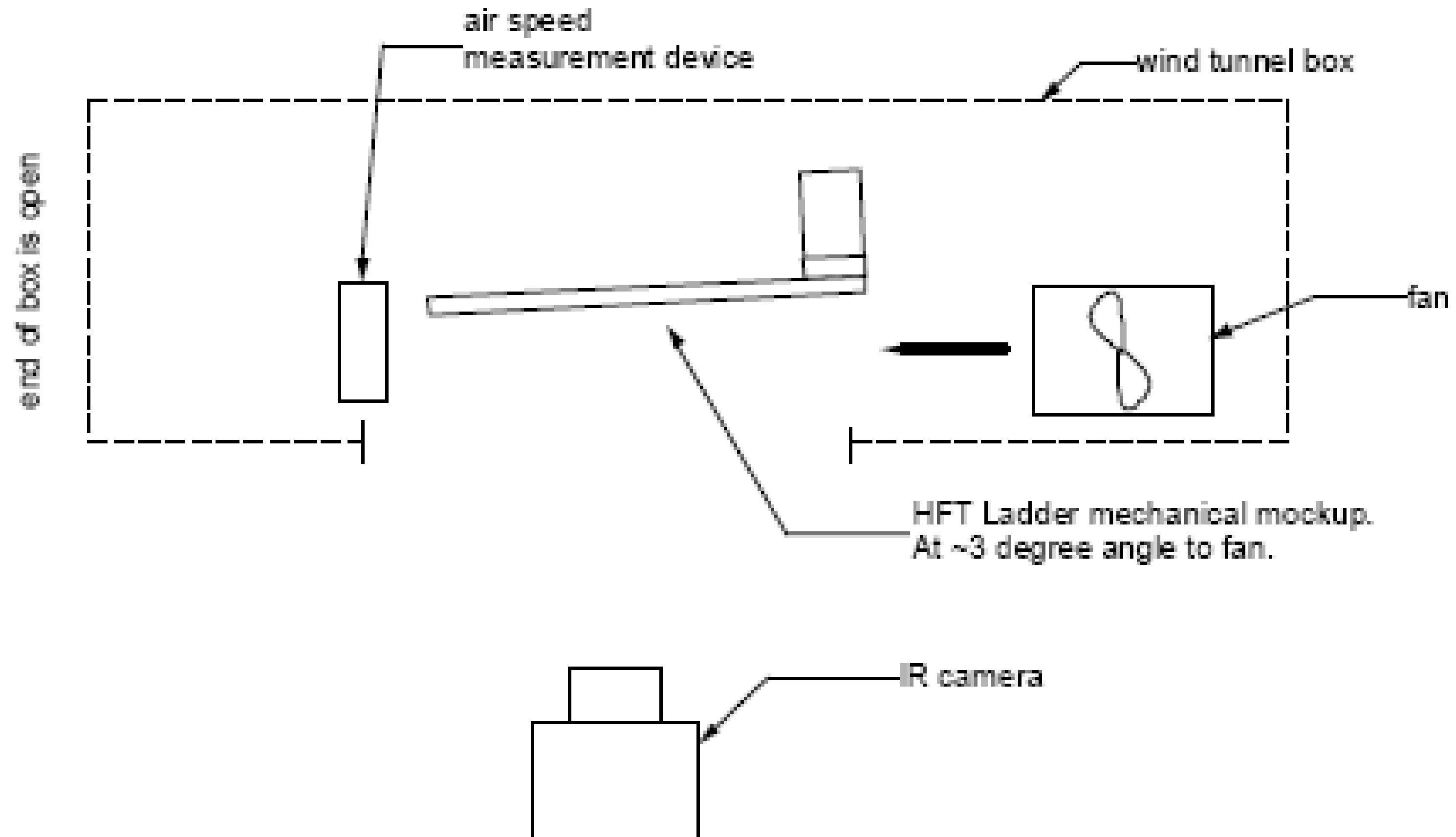
6.5 cm

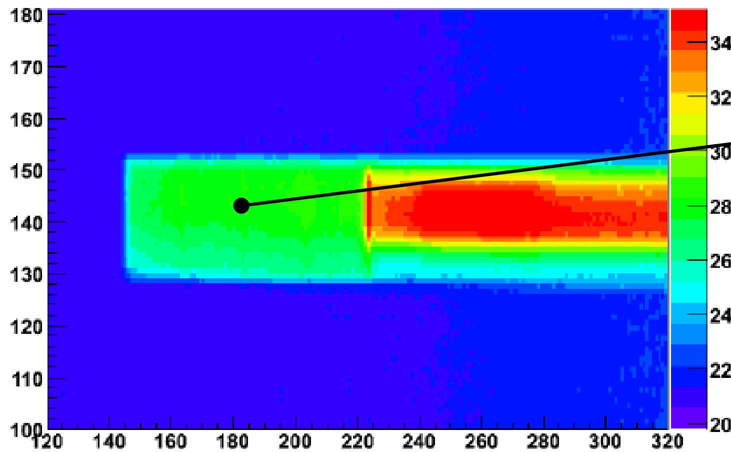
Outer layer

Beam pipe exoskeleton

10 cm

Thermal, a more comprehensive test confirming older measurements





Thermal conductivity of silicon is sufficient to get uniform temperature even though a non uniform heating profile was used.

10 °C rise over ambient at 1 m/s air velocity

Data

Airspeed m/s	Temperature
off (pre-test)	21.016 C
0.65 m/s	32.828 C
1.1 m/s	31.092 C
2.0 m/s	30.44 C
3.5 m/s	28.288 C
4.5 m/s	27.24 C
off (after test)	21.344 C
0 (larger heater on at 80mW/cm^2)	53 C

Mechanical effort

- Still no serious mechanical engineering effort this last year.
- Negotiating to bring in outside composite engineering capability
- Would very much like ATLAS pixel effort to complete so that we can bring home the LBNL mechanical engineering talent and expertise in composite design to help us

- This year we focused our effort (including mechanical) on MIMOSTAR2 telescope for beam tests

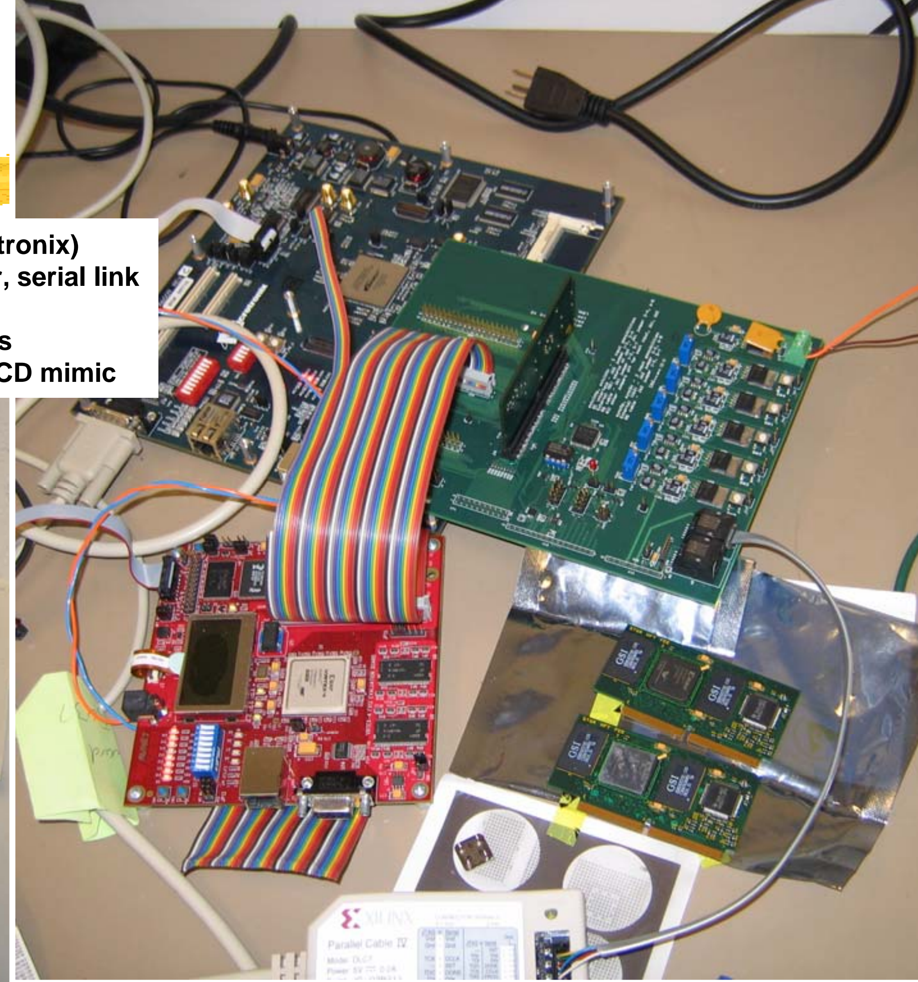
Planned beam test with 3 chip MIMOSTAR 2 Telescope

- This has been the main program this year
- Purpose
  - Develop electronics
  - Measure STAR environment close to the beam
- Some associated mechanics

- Test MIMOSTAR-2 at the BNL SEU Tandem Facility, latch up and single event upset

Readout development, run 7 telescope test

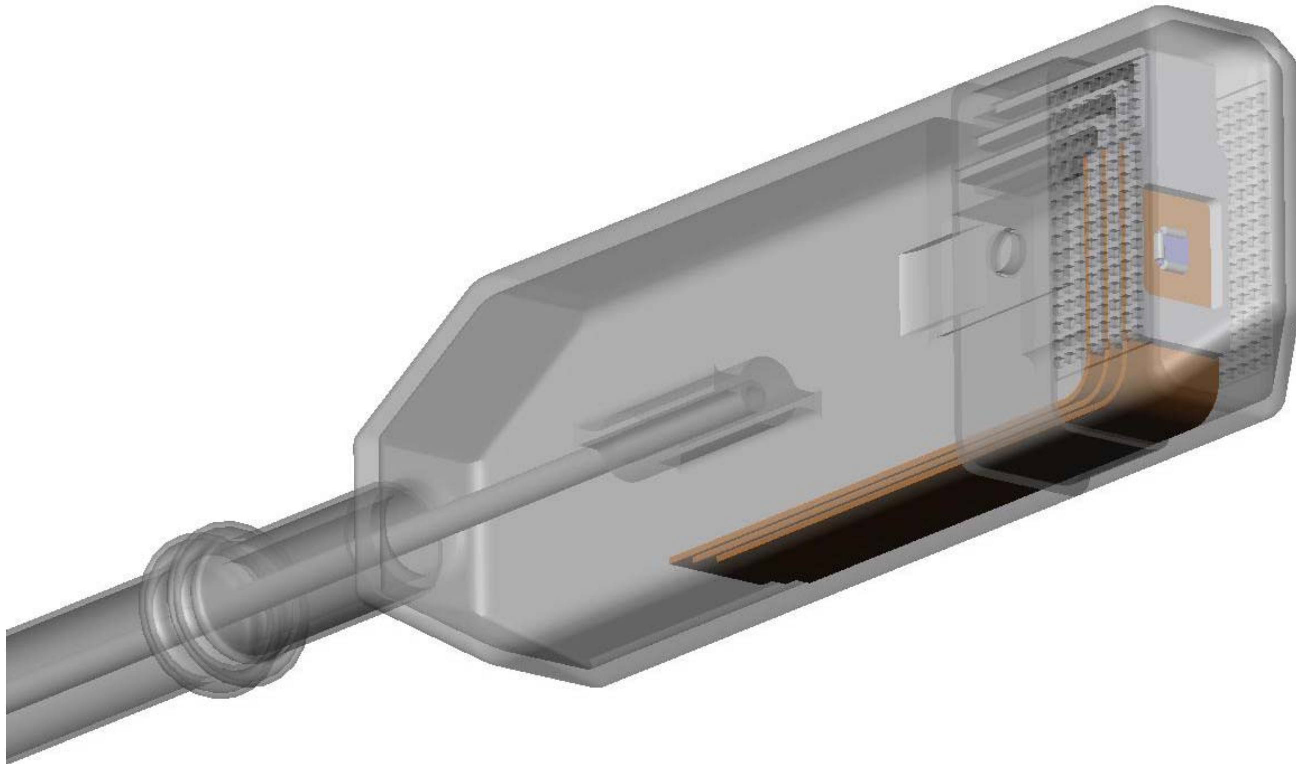
ALTERA FPGA development board (Microtronix)
NIOS Embedded processor, serial link
Mother board
Daughter board, Xilinx FPGA, SRAM, ADCs
Xilinx FPGA development board, trigger TCD mimic



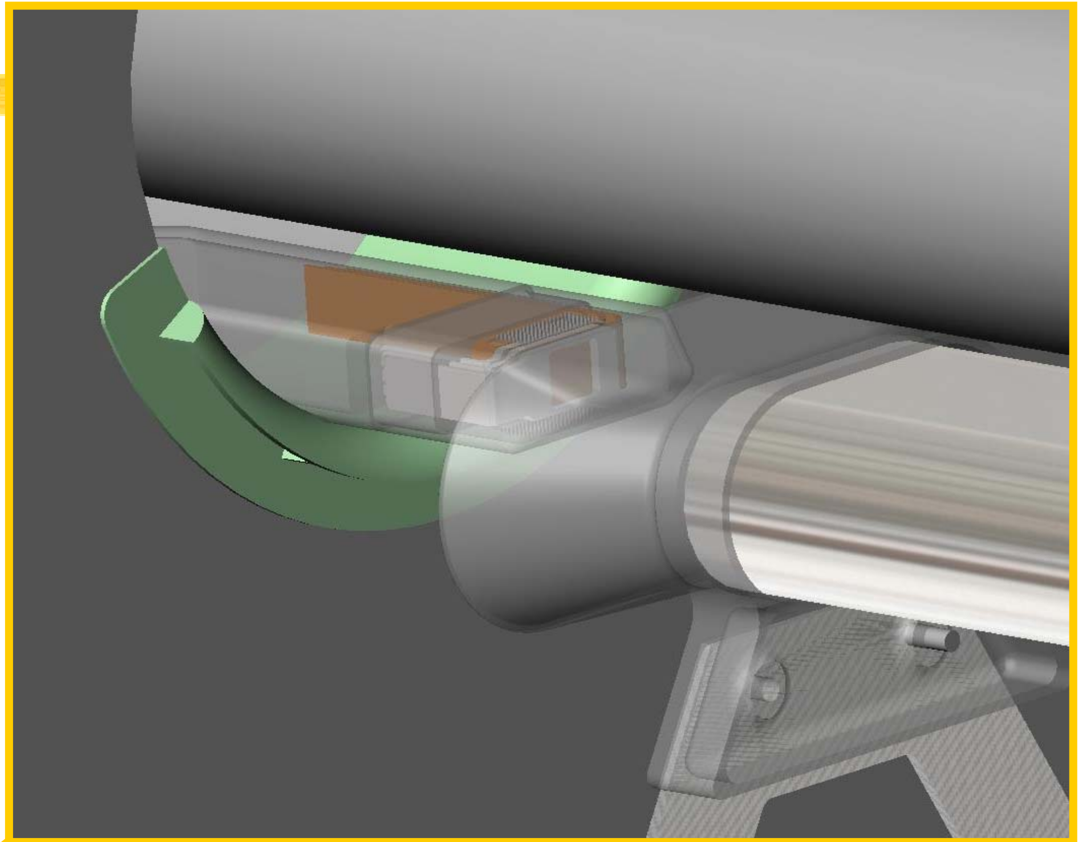
Leo Greiner
Xiangming Sun
<u>Michal Szelezniak</u>
Chinh Vu
Thorsten Stezelberger
(Fred Bieser)
(Robin Gareus)

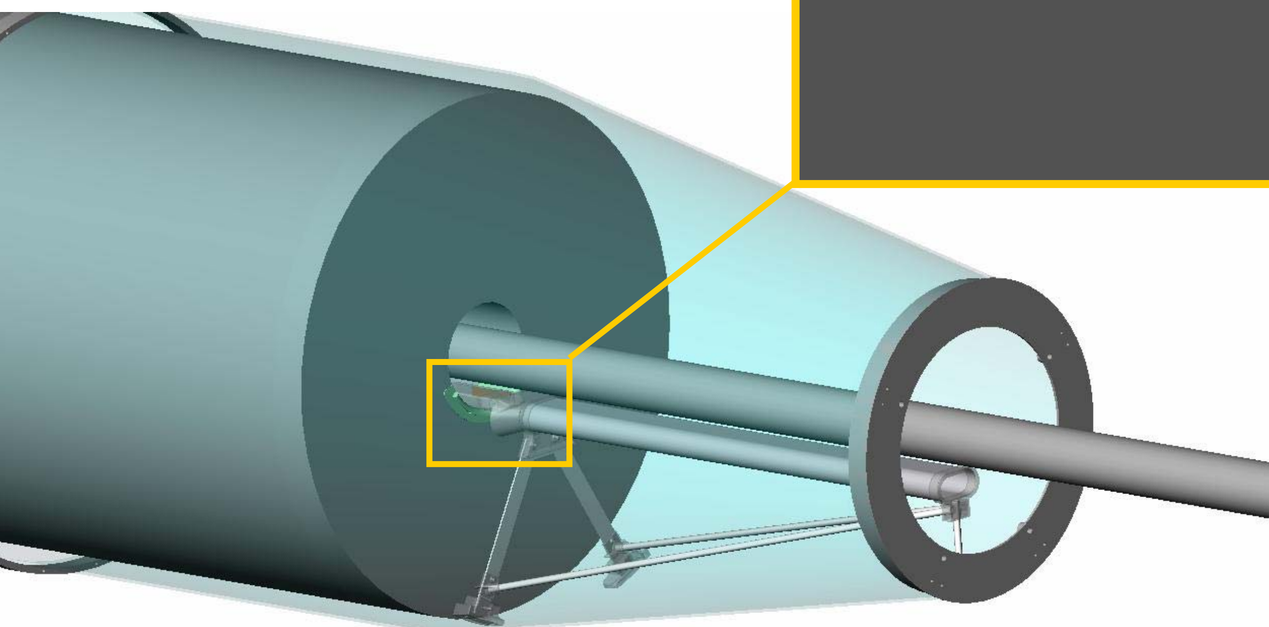
MIMOSTAR2 Telescope, Run 7 STAR test

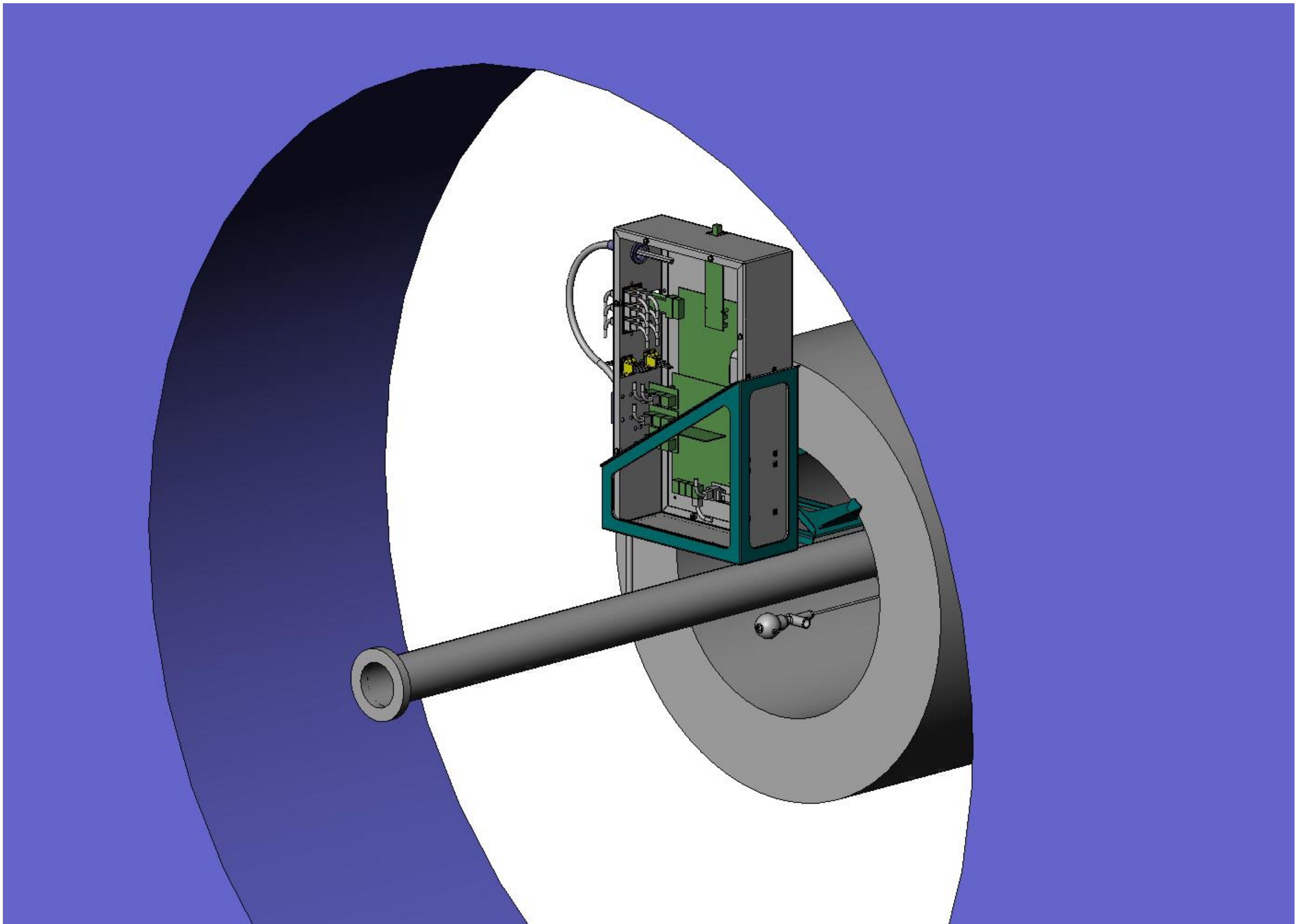
- 3 MIMOSTAR2 chips mounted as close together as reasonably possible
- Insertable close to the beam line within 60 cm of the interaction point
- Measure STAR track densities
- Test MIMOSTAR technology
- Test DAQ/TRIGGER system for HFT



Insertion in STAR







Latch up tests

- Tests of MIMOSTAR 2
- Facility: SEUTF at BNL, tandem

Description and Results of latch up tests
May 24, 25 2006

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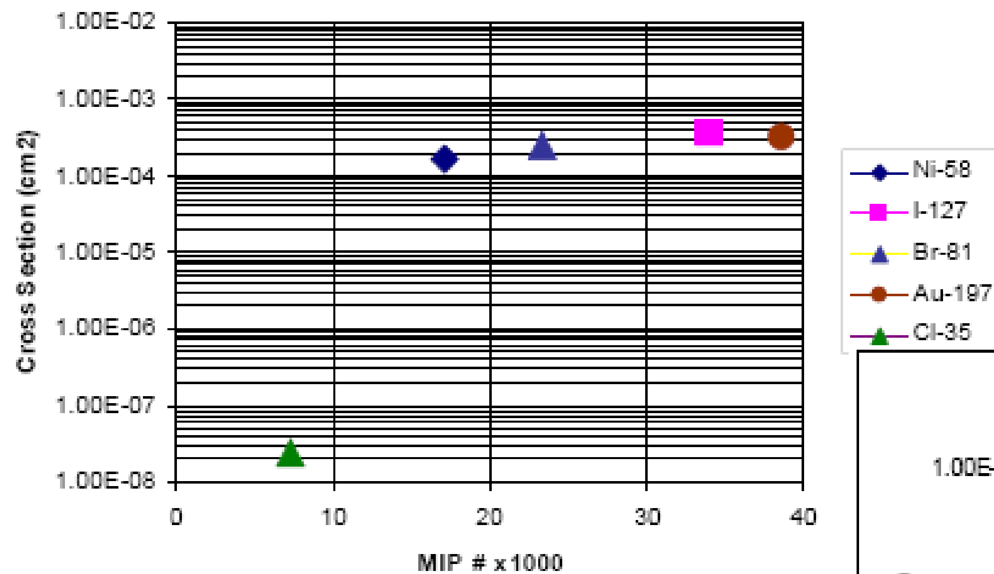
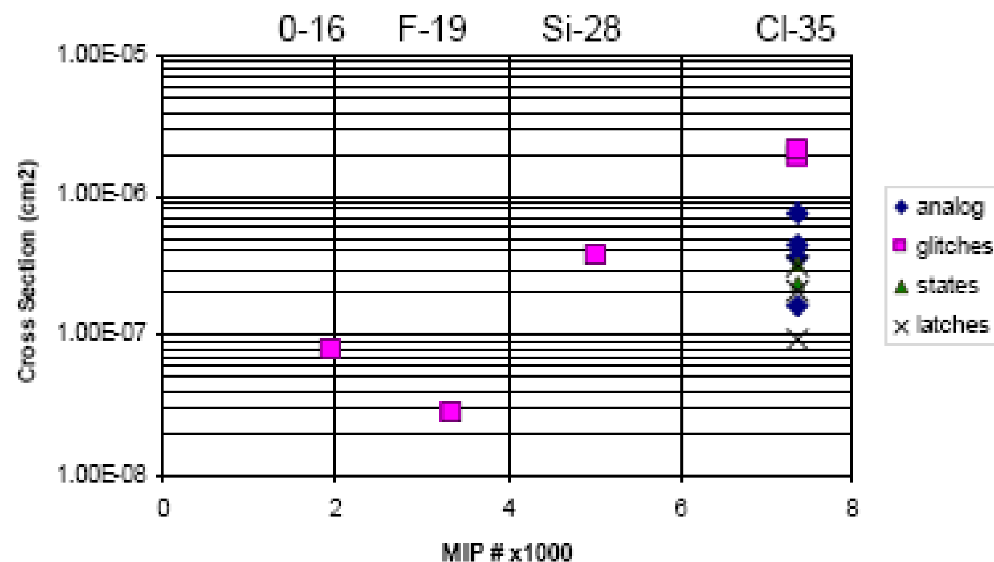
Figure 1 SEUTF at BNL. The MimoStar2 test setup is visible in the front. Visible in the back is vacuum chamber open to allow fixing the device under test.

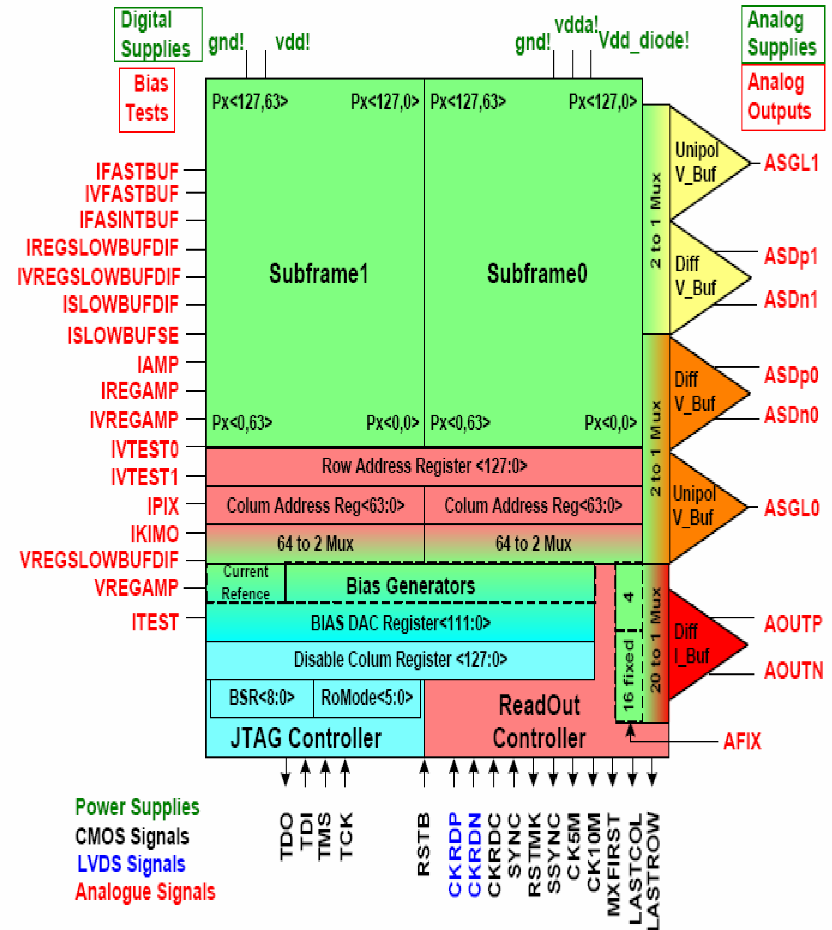
Latch up and upset results





IPHC/IReS MIMOSTAR chips

- MIMOSTAR1 (0.25 μm TSMC)
  - Reduced size prototype but sophisticated chip with complete functions for operation in a real detector system
  - Everything operating except pixel signal because of 0.25 μm TSMC feature: Unexpected short signal decay time compared to theory and AMS experience.
- MIMOSTAR2(0.35 μm AMS optical process)
  - Tested in beam
  - 700-800 e most probable for Min-I
  - 10-12 e-rms, noise.
  - Signal decay time 100 ms



MimoStar2 functional view

Ultimate (fast APS detector) - good for high luminosity at RHIC

- Submitted requirements list to IReS/IPHC.
  In discussion

Ladder active area	2cm × 20cm
Pixel size	30µm × 30µm
~Pixel mapping on the ladder	640 × 6400
Minimum operating distance from beam	1.5 cm
Power	≤100 mW/cm²
Operating temperature	≥30 °C
Integration time[1]	≤0.2 ms
Mean silicon thickness	≤100µm
Readout time	≤1 ms
Efficiency (min I)[2]	≥98%
Accidental cluster density	≤50/cm²
Binary readout, number of threshold bits[3]	2
Radiation tolerance [4]	≥124 kRad
Number of conductors supporting the ladder (10 chips/ladder)[5]	≤140
Triggered readout, maximum trigger delay[6]	2 µs

Technology MIMOSA8

A Fast Monolithic Active Pixel Sensor with Pixel Level Reset Noise Suppression and Binary Outputs for Charged Particle Detection

Yavuz Değerli, *Member, IEEE*, Grzegorz Deptuch, *Member, IEEE*, Nicolas Fourches, *Member, IEEE*, Abdelkader Himmi, Yan Li, Pierre Lutz, and Fabienne Orsini

Abstract—In order to develop precision vertex detectors for the future linear collider, fast active monolithic active pixel sensors are studied. Standard CMOS 0.25 µm digital process is used to design a test chip which includes different pixel types, column-level discriminators and a digital control part. In-pixel amplification is implemented together with double sampling. Different charge-to-voltage conversion factors were obtained using amplifiers with different gains or diode sizes. Pixel architectures with DC and AC coupling to charge sensing element were proposed. As far, hits from conversion of ^{55}Fe photons were registered for the DC-coupled pixel. Double sampling is functional and allows almost a complete cancellation of fixed pattern noise.

I. Introduction

In the next generation of linear colliders required for future high energy physics experiments, such as the Next Linear Collider (NLC), the Japanese Linear Collider (JLC) and the TeV Energy Superconducting Linear Accelerator (TESLA), precise vertex detectors will be necessary to study the Higgs mechanism. Secondary vertex measurements make a high-resolution vertex detector a necessary part of the detecting system. Precision vertex measurements will be a step forward. Improvements in the spatial resolution are requested making the use of Active Pixel Sensors (APS) an attractive alternative to Hybrid Pixel Sensors (HPS), chosen for the forthcoming Large Hadron Collider (LHC) experiments, both in terms of electronic/detector integration and material thickness. Precision vertex measurements will be a requirement. There has been significant progress done by the IReS/LEPSI-Strasbourg group in the use of the monolithic active pixel sensors (MAPS) for the detection of Minimum Ionizing Particles (MIP) [1]. An array of active sensors with a readout circuitry is integrated in a monolithic structure of a silicon chip. These sensors are designed with standard CMOS technology and have significant advantages over Charge Coupled Devices (CCDs). Two exemplary strong points of MAPS are the high radiation hardness and the flexibility of the readout architecture design. In this paper the chip design with new all-NMOS pixel architectures with integrated correlated double sampling (CDS), suitable for charged particle detection is presented.

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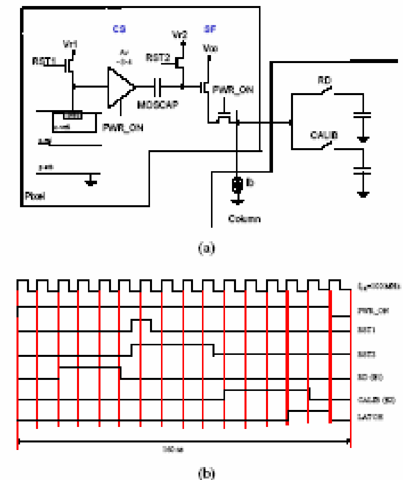
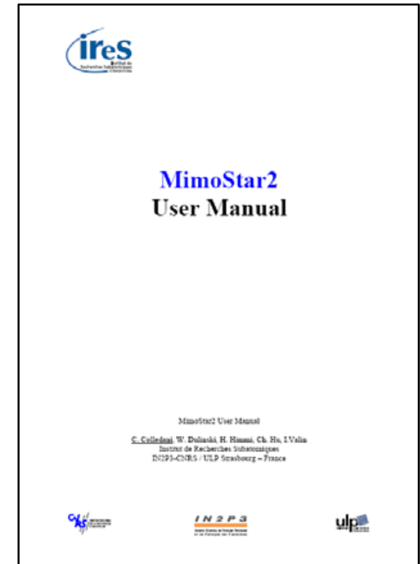


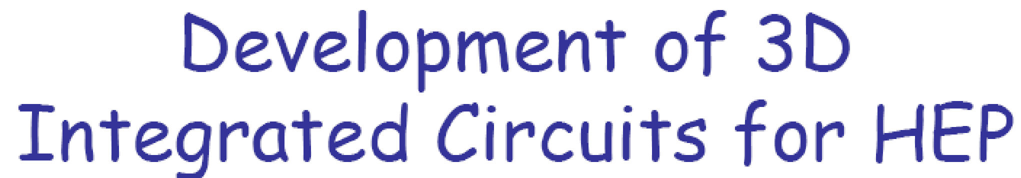
Fig. 1. (a) Schematic of the proposed DC-coupled pixel and, (b) related timing (clocking stimuli) with f_{CK}=100 MHz. RD, CALIB and LATCH signals are used by the column readout circuitry.

MIMOSTAR chip development at Strasburg

- MIMOSTAR 1 -
  - full system functionality
  - 4 ms integration
- MIMOSTAR 2 –
  - full system functionality
  - 4 ms integration
  - 1/25 th reticule
- MIMOSTAR 3 –
  - Same as MIMOSTAR 2, but ½ reticule
  - Engineering run, submitted July 06, foundry will re-run
- MIMOSTAR 4 –
  - Same as MIMOSTAR 2 and 3, but full reticule
  - 640 k pixels
- MIMOSTAR ULTRA
  - 200 μs integration time
  - Based on MIMOSA 8 technology with on pixel analogue storage



Some material from Grzegorz Deptuch



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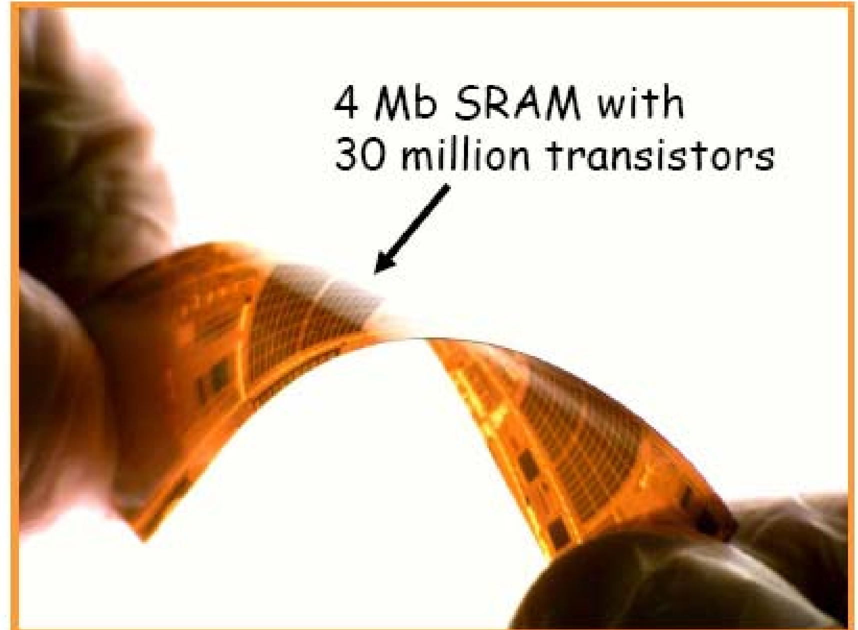
Batavia, Illinois

12th LHC Electronics Workshop,
Valencia, Spain
September 25-29, 2006

Thinned SOI Wafers

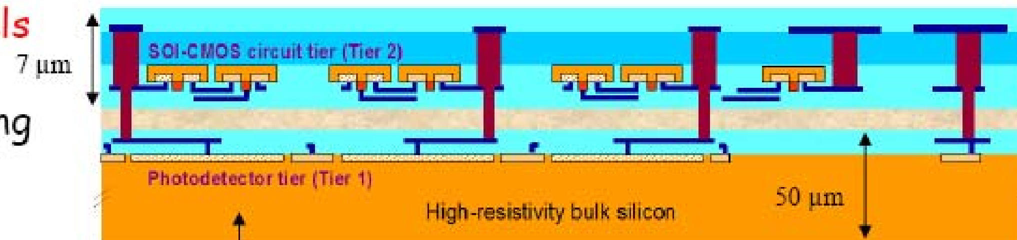


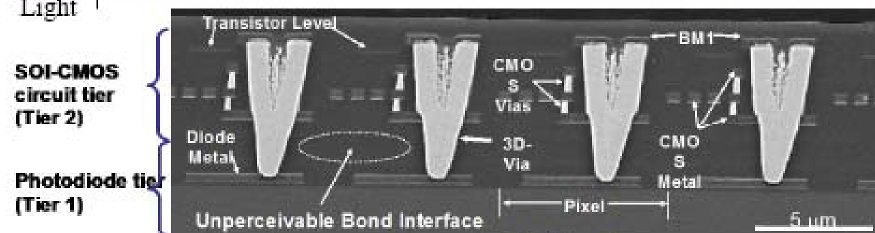
Wafer thinned to 6 microns and mounted to 3 mil kapton (MIT LL)

The future is here, Yarmia

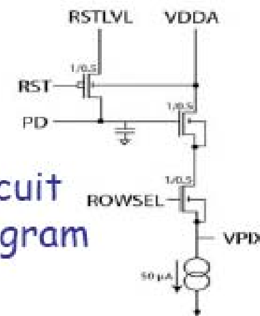
3D Megapixel CMOS Image Sensor[8]

- 1024 x 1024, 8 μm pixels
- 2 tiers
- Wafer to wafer stacking (150 mm to 150 mm)
- 100% diode fill factor
- Tier 1 - p+n diodes in >3000 ohm-cm, n-type sub, 50 μm thick
- Tier 2 - 0.35 um SOI CMOS, 7 μm thick
- 2 μm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- 1 million 3D vias
- Pixel operability >99.999%
- 4 side abuttable array





Drawing and SEM Cross section



Circuit Diagram

Image

3D IC Advantages

- Increased circuit density without going to smaller feature sizes
  - ILC demonstrator has 175 transistors in a 20 μm pixel
- Unlimited use of PMOS and NMOS transistors
- 100% diode fill factor
- SOI Advantages
  - High resistivity substrate for diodes provide large signals
  - Minimum charge spreading with fully depleted substrate
  - Inherently isolated vias
- 3D may be used to add layers above other sensors types currently under development.

FERMILAB design in OKI SOI 0.15 mm process

detector diodes

discriminator

CSA

D-flip/flop

Flip/flops form 12 bit counter

shaper

pixel

26 μm

end