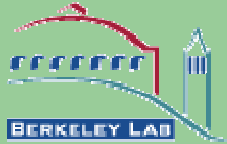


Research and Development for the HFT at STAR



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Recent progress in
hardware and firmware
development

Outline

- Design of the HFT
- Development of the MimoStar family of sensors
- Motivation for the prototype telescope
- Realization of the telescope
 - System architecture
 - Hardware
 - Firmware
- Current status and future plans

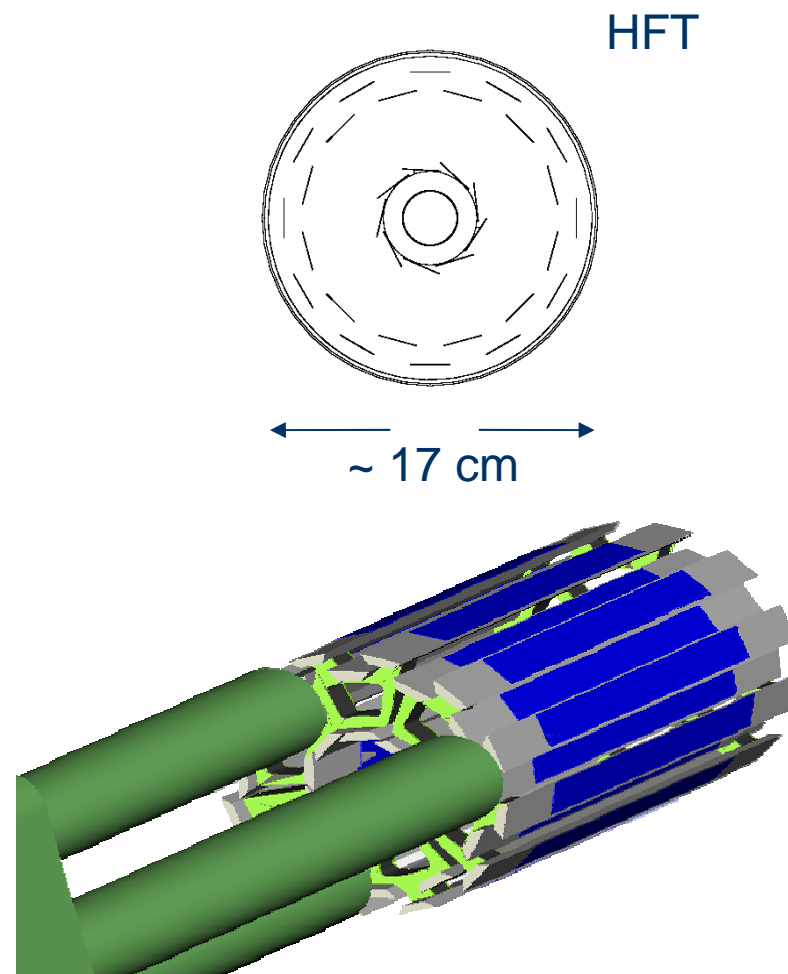
Design of the HFT

Purpose:

Greatly improve charm hadron capability in STAR

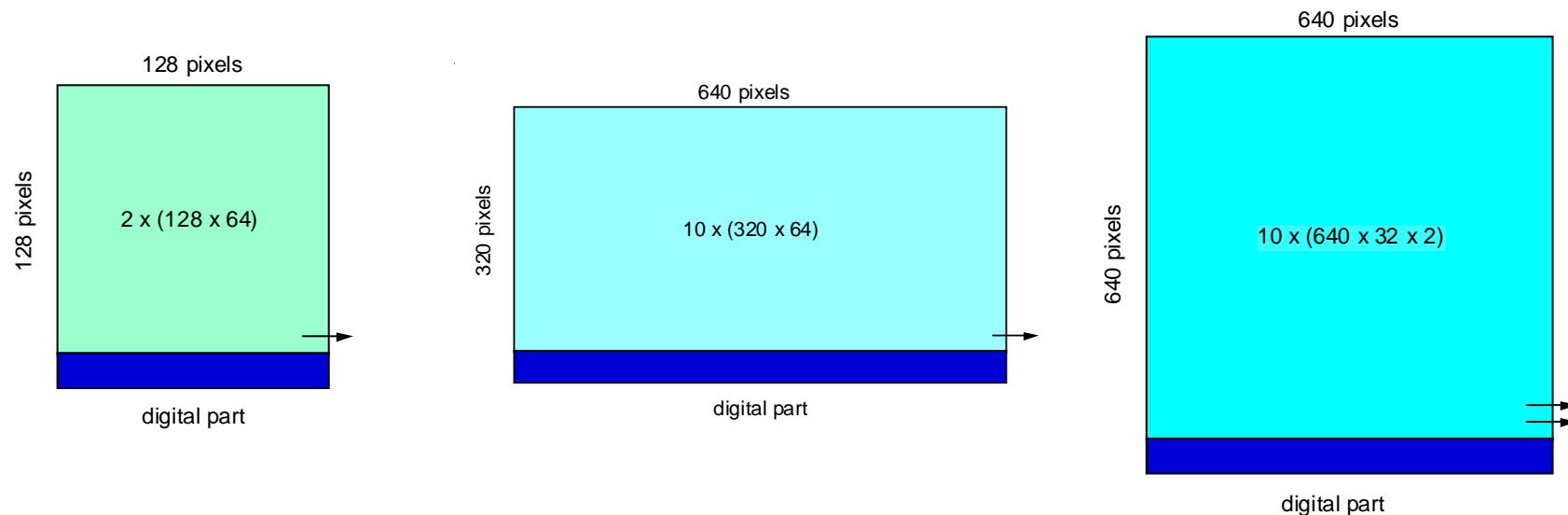
Characteristics:

- Two layers at 2.5 & 7 cm radius (9+24 ladders)
- 0.28 % radiation length/layer
- air cooled
- Active Pixel Sensors
 - thinned to 50 μm thickness
 - 30 μm x 30 μm pixels
 - ~135 M pixels



MAPS development @ IPHC, Strasbourg for the STAR Upgrade

- JTAG controlled (internal reference voltages and currents set with integrated DACs)
- Serial data readout @ high frequency (we are using 50 MHz)



	MimoStar 2	MimoStar3	MimoStar4
Sent for Fabrication	June 2005	June 2006	(?)
Pixels	128 x 128	320 x 640	640 x 640
Sub arrays	2 + 8 virtual	10	20
Goal	validate design	assess yield	for the detector with 4ms readout time

Motivation for the telescope

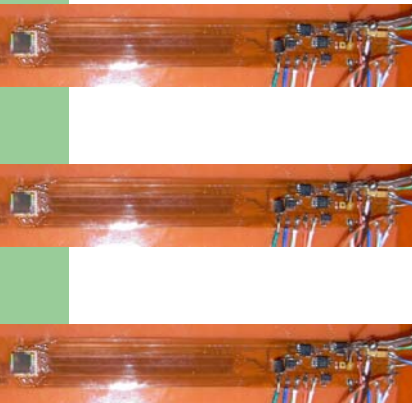
- ☺ **The telescope is a small prototype and contains all elements easily scalable to meet the requirements of the HFT**

test functionality of a prototype MIMOSTAR2 detector in the environment at STAR 2006-2007:

- Charged particle environment near the interaction region in STAR.
- The noise environment in the area in which we expect to put the final HFT.
- Performance of the MIMOSTAR2 sensors.
- Performance of our cluster finding algorithm.
- Performance of our hardware / firmware as a system.
- Functionality of our tested interfaces to the other STAR subsystems.

Realization of the telescope

MimoStar2 chips on kapton cables



Analog signals
Clock & control
JTAG
LU prot. Power

MOTHER BOARD



Analog signals
Clock & control
Cluster FIFO
Hot Pixel Map
Memory Acces:
(for full frame)
Trigger info
Power

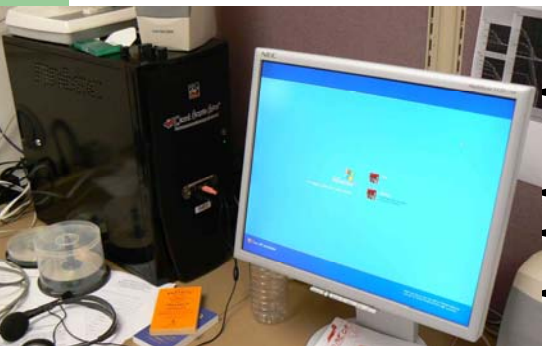
DAUGHTER CARD



Trigger, Clock
from MWPC

Power
from MWPC

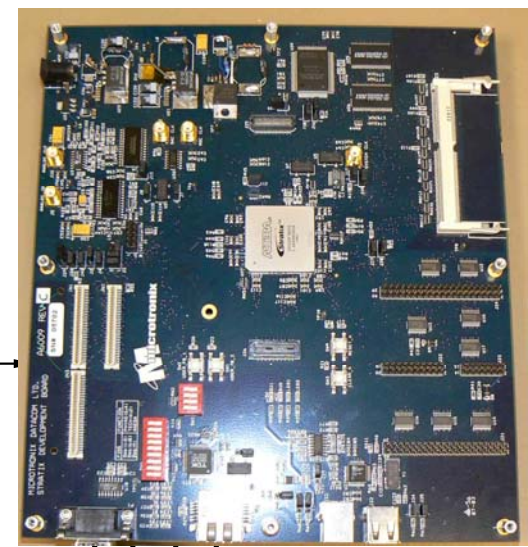
Control PC (Win)



JTAG
x3 for MIMOSTAR
x1 for daughtercard

Latch up
monitor and reset

Trigger, Clock
Cluster FIFO
Busy to trigger



STRATIX

JTAG

serial / ip connection

DDL to Linux PC

power

Acquisition Server (Linux)



RORC SIU

Realization of the telescope

MimoStar2 chips on kapton cables

Analog signals
Clock & control
JTAG
LU prot. Power

MOTHER BOARD

Analog signals
Clock & control
Cluster FIFO
Hot Pixel Map
Memory Acces:
(for full frame)
Trigger
Power

DAUGHTER CARD

Continuous MimoStar2 readout

(2) TCD trigger

(0) Data acquisition

(1) CDS, sorting, CF

(3) Building event

complex Hardware and Firmware development

Trigger, Clock
Cluster FIFO
Busy to trigger

(4) Formatted Event

JTAG
x3 for MIMOSTAR
x1 for daughtercard

Latch up
monitor and reset

JTAG

serial / ip connection

STRATIX

(5) Transfer data for this event

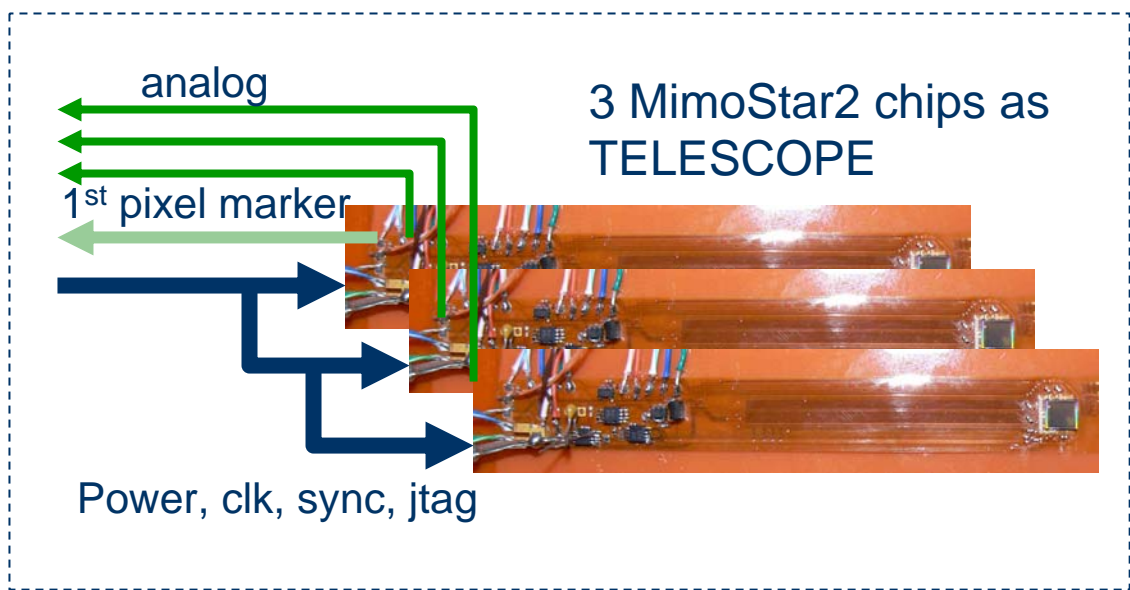
Linux PC

power

Acquisition Server (Linux)

RORC SIU

Hardware - telescope head



Kapton cable:

- 2 Cu layers
- Thickness 25 μ m (kapton only)

✓ **DONE & UNDER TEST**

Hardware components I



Mother board

- ✓ Trigger interface to TCD
- ✓ Latch up protection on all power supplies
- ✓ Remote FPGA programming



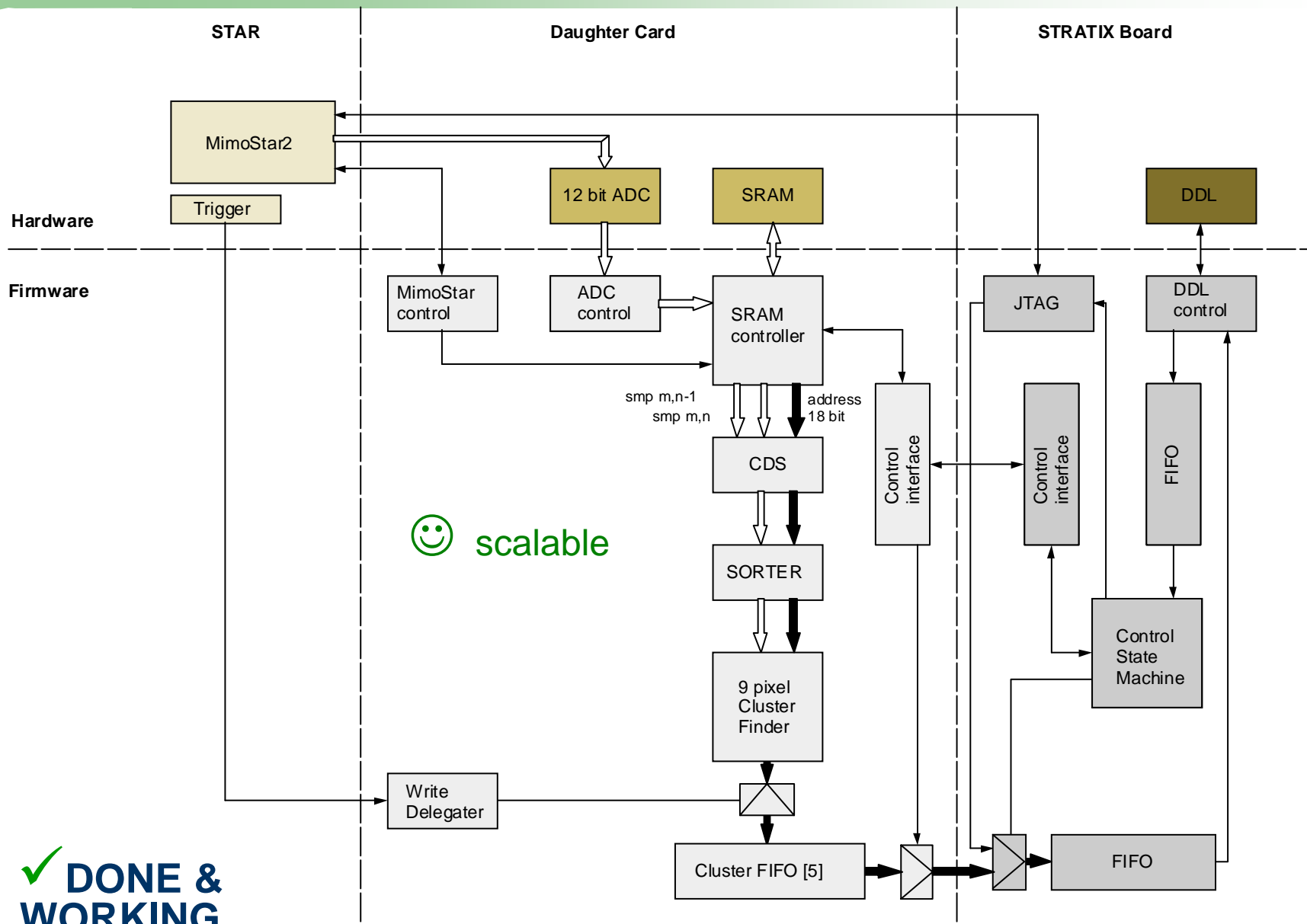
Daughter Card

- ✓ 50 MHz 12bit ADCs with serial readout
- ✓ SRAM
- ✓ Accept and respond to triggers
- ✓ CDS
- ✓ Data resorter (because sub-arrays of MimoStar2 are multiplexed for serial readout and reconstruction of arrays is necessary for raster scan is cluster finder module)
- ✓ Cluster finder (slide 12)
- ✓ Cluster FIFO (slide 14)
- ✓ Event builder

Daughter card form the previous stage of development – in the future probably integrated into MB

✓ **DONE & WORKING**

Firmware - overview

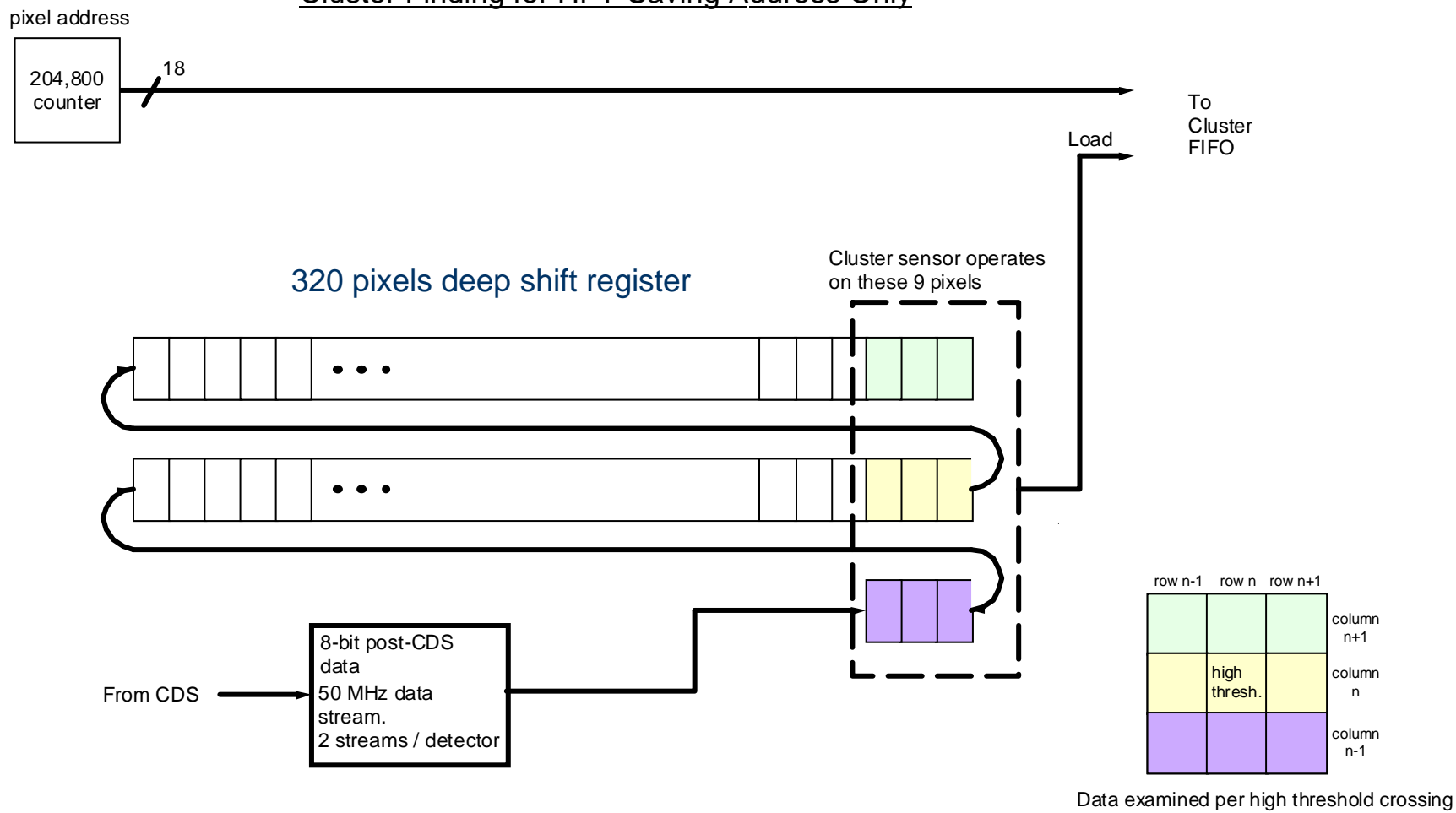


✓ **DONE & WORKING**

Firmware - Cluster Finder

😊 on line cluster finding will allow to reduce data flow at HFT by about **three** orders of magnitude

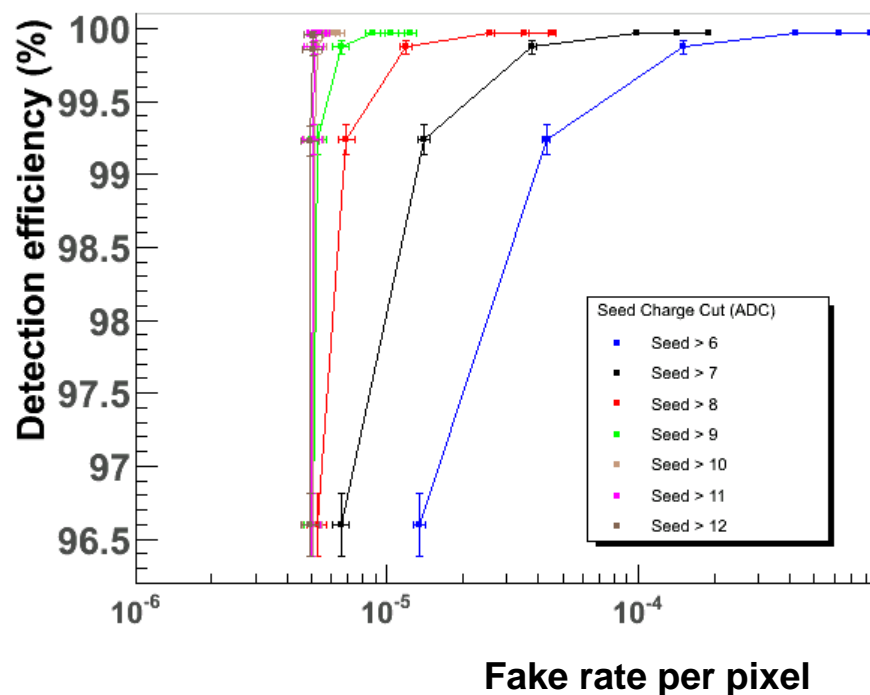
Cluster Finding for HFT Saving Address Only



✓ **DONE & WORKING**

Firmware - Cluster Finder - efficiency

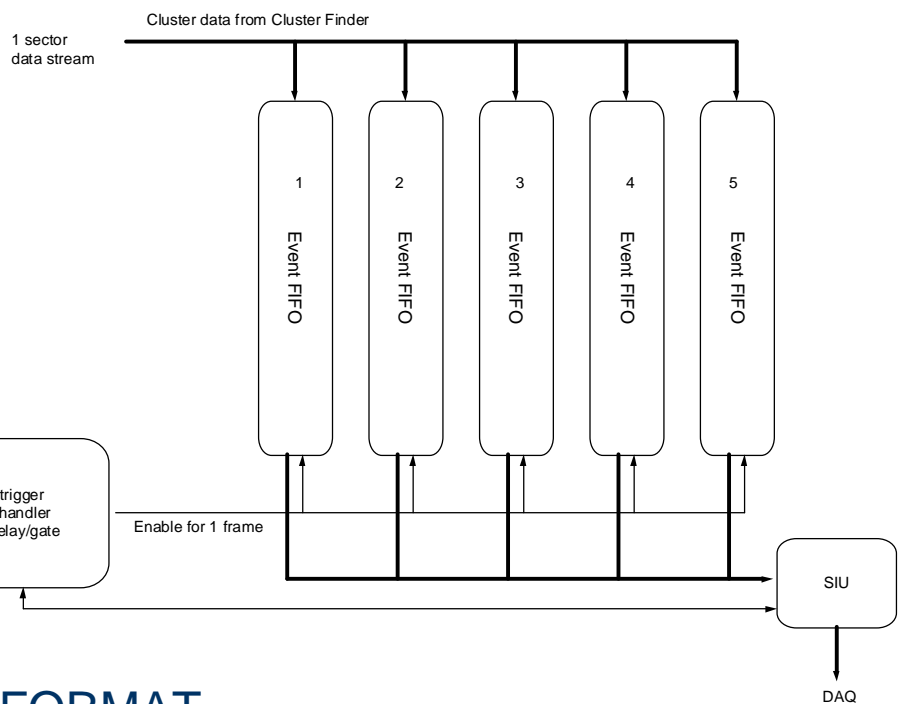
Mimosa 9. Efficiency VS Fake



By Auguste Besson, IPHC, Strasbourg

- From a prototype in the same technology as MIMOStar
- Small diode, pixel pitch 20 μ m, measured @ 20 °C
- Noise ~10 electrons
- ADC cut on central pixel: 6,7,8,9,10,11,12
- ADC sum of 8 neighbors: 0,3,9,13,17
- Each line – fixed central cut, variable cut on neighbors
- Efficiency >99.9 with a fake rate of ~10e-5 is possible
- In reality noise will be higher but a similar efficiency should be achieved for a fake rate below 10e-4

Firmware - Event builder

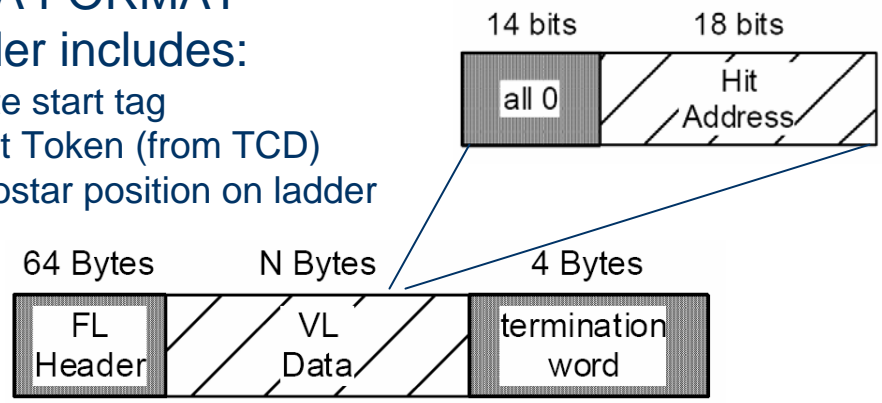


- Each Trigger enables an empty Event FIFO for 1 frame (204,800 clocks = 4ms) with an offset to the enable that aligns the event start time with the location of the first pixel in the event.

- Each event FIFO is a separate trigger event stream and can be enabled independently. This allows events to be triggered at ~1 ms intervals with our 4 ms latency.

DATA FORMAT header includes:

- 4 byte start tag
- 12 bit Token (from TCD)
- Mimostar position on ladder



- Each sector event FIFO is emptied by the SIU at the end of it's triggered frame.

✓ **DONE & WORKING**

Current status and future plans

- Hardware:**
- ✓ Mother board
 - ✓ Daughter card
 - ✓ Stratix card
 - ✓ DDL
 - 3 MimoStar2 telescope

- Firmware:**
- ✓ Testing interface
 - ✓ JTAG
 - ✓ Full frame RDO (CDS)
 - ✓ DDL – RORC
 - ✓ Cluster finder, cluster FIFO
 - Full functionality interface

- Software:**
- ✓ lab tests – ^{55}Fe calibrations
 - Complete system control

- ✓ Infrastructure

^{55}Fe calibrations
 Analysis and evaluation
 Gain adjustment

ALS
 (1.5 GeV electrons)
 Tests, evaluation,
 tuning

BNL
 Tests outside and
 inside the magnet

- ✓ DONE & WORKING
- under development

