

# **The STAR Heavy Flavor Tracker**

## **An Introduction to the Project Cost and Schedule**

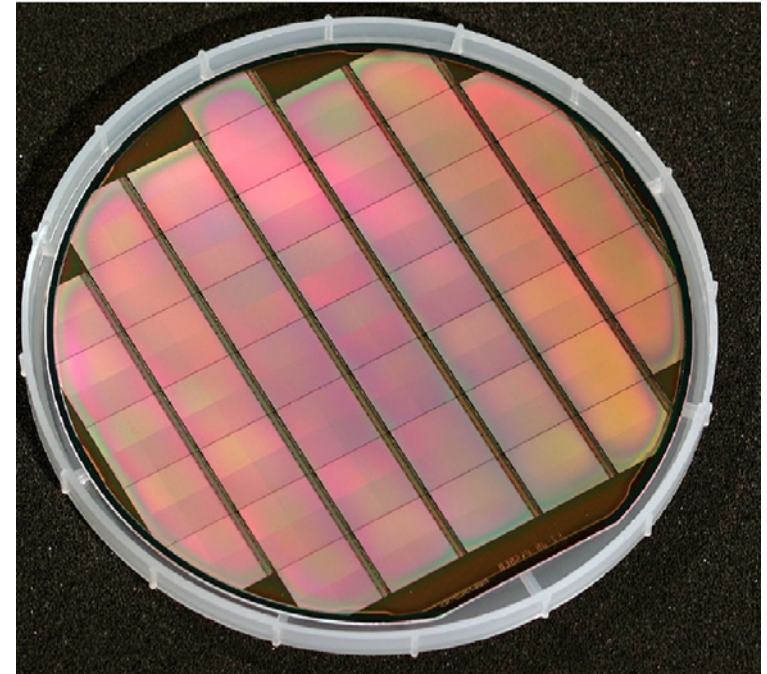
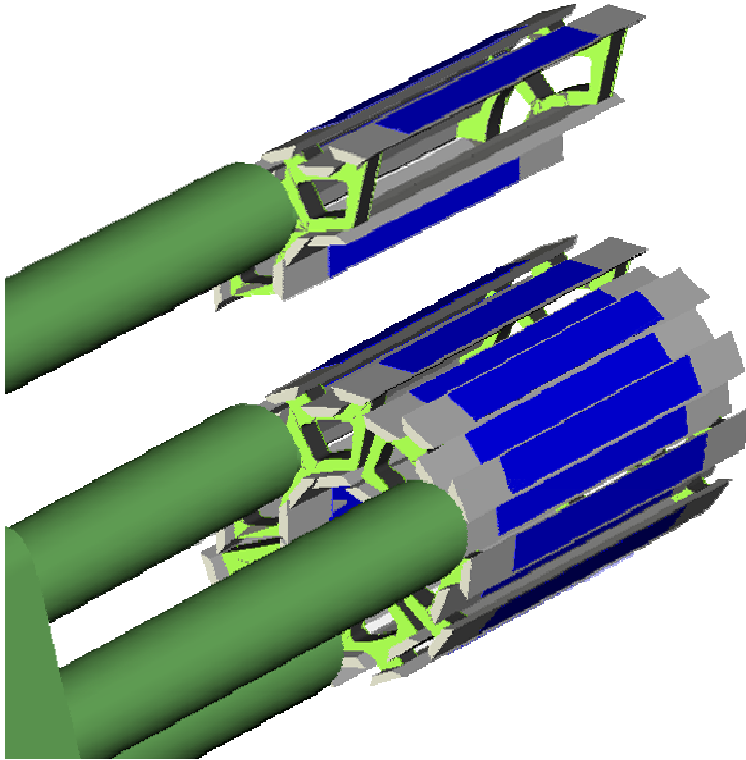
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**January 30<sup>th</sup>, 2007**

# The Technically Driven Schedule



Driven by the availability of CMOS Active Pixel Sensors



Technically driven schedule has slipped one year

1999	2001	2003	2004	2005	2006/7	2008	2009/10
Mimosa-1	Mimosa-4	Mimosa-8	MimoSTAR-1	MimoSTAR-2	MimoSTAR-3	MimoSTAR-4	Ultra STAR

The technical schedule is ahead of any realistic project schedule

# The Availability of Funds



- The previously published BNL Mid-Term Plan included funding for STAR

## Proposed HFT Profile

06	07	08	09	10
300K	1M	800K+300K	2.5M	2.5M
R&D	R&D	R&D+Const	Const	Const

- Changes since our discussion last year
  - Tremendous progress on Electrical Engineering for the HFT
  - Annus Horribilis for funding of science ... many things didn't start
  - Little progress on Project Engineering and Mechanical Engineering for HFT
- The full schedule of activities that we described last year are still required
  - The full list of activities is still required
  - The full integral of funds is still required

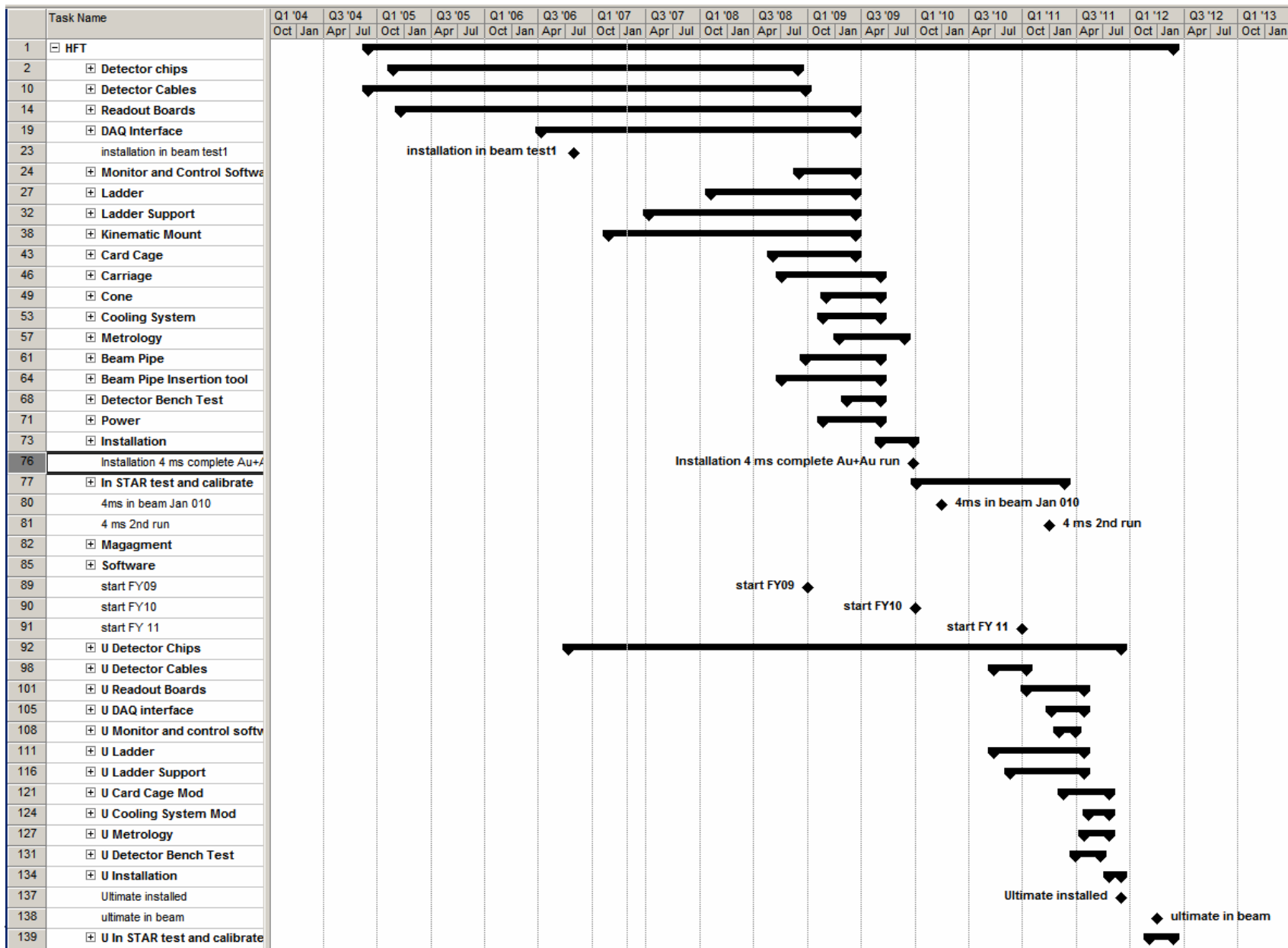
# A proposal that allows us to move forward



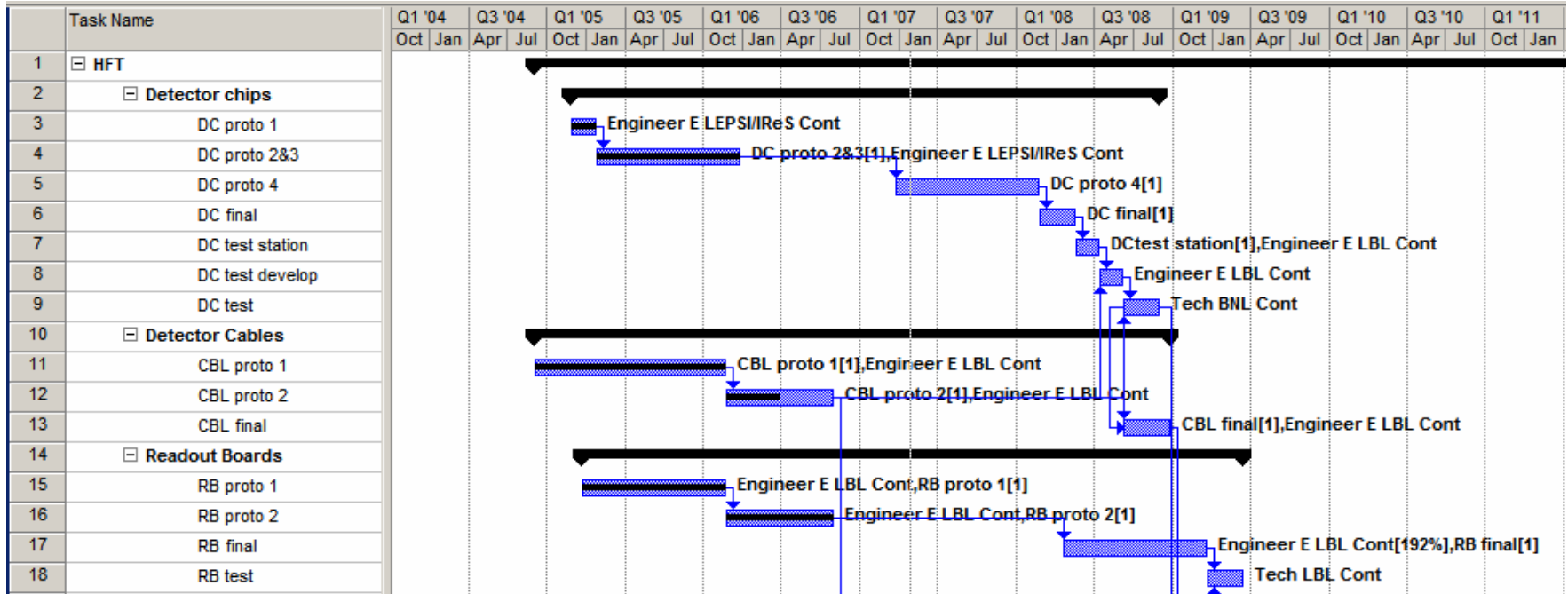
- Propose to *start* the construction project in '09, *finish* the project in '11
  - Propose to keep the integral of funds the same, but shift the profile of funds
  - Obvious question of how to handle funds in '07 and '08
    - A complex question involving all RHIC detectors ... discussion w/BNL req'd
- We don't like it ... it delays the scientific output of the program
- Critical milestones that are the key to success (science & technology)
  - In-beam end of CY09 with 4 msec frame rate prototype
    - Do extensive prototyping with MimoSTAR-4 chips and readout electronics
    - Mount them in STAR, real beam pipe, real beam rates, real background
    - Critical test of mechanical insertion device, critical test of alignment tools
  - In-beam end of CY11 with 200  $\mu$ sec frame rate detector
    - The project has the 200  $\mu$ sec readout chip as the final goal
    - Compatible with RHIC II luminosities

Delay completion of the project by 1 year  
but keep the FY '09 start date

# Schedule for R&D and Construction of the HFT



# “Enterprise Management” – Schedule Details



- The Gantt Chart tracks the full enterprise of activities
  - not a ‘project’ Gantt chart because it tracks more than the ‘project’
  - some pre-conceptual design activities are included and complete
  - we do not track, or cost out, the IPHC/Strasbourg contributions
- For the most part, it’s a conventional project with R&D and construction activities tracked across time
  - Engineering, technical, and contributed labor are included
- Still some awkward gaps that require professional care
  - Contingency is in dollars, schedule contingency needs work

- **Challenging HFT technologies**
  - **The Silicon Chips**
    - Further refinement of on-chip electronics
  - **Readout Electronics**
    - speed, heat dissipation, compatibility with DAQ
  - **The Mechanical Arms to insert the detector**
    - Alignment and stability
  - **Calibration, Tracking & Software**
    - New levels of precision
  - **The beam pipe**
    - Unusual design and extra robustness required due to length

- **Six years of Experience developing CMOS Active Pixel Sensors**
- **Long term goal of developing sensors for the ILC, CBM and STAR**
- **Outstanding staff and students**
  - **10 Engineers**
  - **3 Physicists**
  - **7 Ph.D. students**
- **Commitment to the project**
  - **MimoSTAR -1, -2, -3 have consumed 2 physicists and 3 engineers over the past 3 years**
- **Financial equivalent value of their contribution**
  - **Approximately \$2.5 Million so far**
  - **Not including substantial savings due to shared wafer costs for R&D**

Not costed to the Project



# Cost of Si Production for R&D



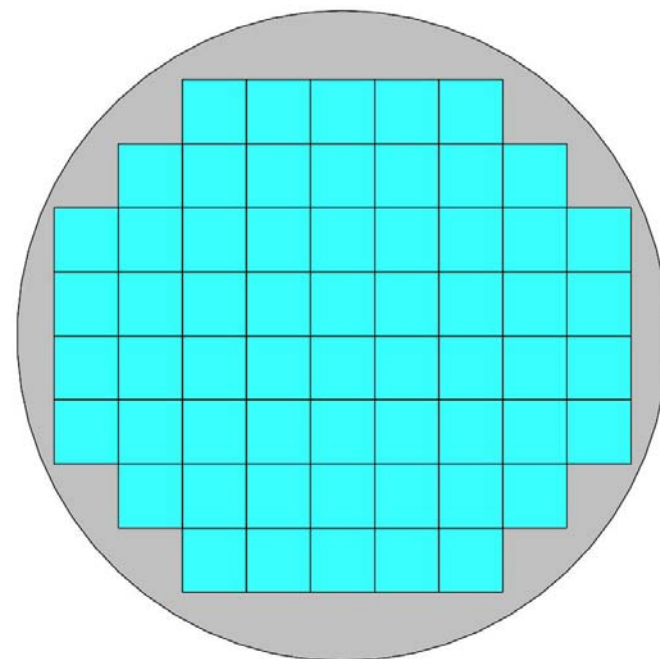
- MimoSTAR-1
  - MimoSTAR-2
  - MimoSTAR-3
  - MimoSTAR-4
- } Approximately one generation each year
- We pay partial cost for R&D and test runs
    - Share mask costs
    - Share space on the wafers
  - We pay full cost for production runs
  - For a non-production run, LBL has be paying 30K – 50K per run
    - IPHC has been absorbing or sharing the remainder of the costs

# Silicon Production Costs for Chips



<b>Chips per ladder</b>	<b>10</b>
<b>Ladders per Detector</b>	<b>33</b>
<b>Number of Detector Copies</b>	<b>4</b>
<b>Number of working chips</b>	<b>1320</b>
<b>Yield</b>	<b>60%</b>
<b>Total chips</b>	<b>2220</b>
<b>Total wafers</b>	<b>37</b>
<b>Wafer Cost Each</b>	<b>7.2 k\$</b>
<b>Wafer Costs</b>	<b>265 k\$</b>
<b>Mask Cost</b>	<b>220 k\$</b>
<b>Total</b>	<b>485 k\$</b>

**8 inch wafers**  
**60 chips/wafer**



# Contingency Levels used on the Gantt Chart



- **Contingency on Si**
  - 50% on fabrication costs
- **Contingency on Engineering**
  - 50% for the first time a component is designed
  - 25% if there has been a prior (significant) R&D test
    - pertains to Ultra Chip
- **Contingency on Hardware procurements**
  - 75%
- **Contingency on Fabricated elements (in house)**
  - 75%

- **MimoSTAR IV chips (4 msec readout)**
  - two copies for R&D work
- **Ultra Chips (200  $\mu$ sec readout)**
  - four copies for the MIE Detector
- **Readout electronics**
  - 100% spares for the MIE Detector

# Cost of Labor



	<b>Base Rate</b>	<b>With OverHead</b>	<b>With 75% Contingency</b>
<b>Engineering</b>	65.60 / hr	132.00 / hr	231 / hr
<b>Technical</b>	43.75 / hr	88.00 / hr	154 / hr

# Cost of Materials for the full enterprise



	Resource Name	Cost	Baseline Cost	Variance	Actual Cost	Standard Rate	Cost Per Use
	<input checked="" type="checkbox"/> Type: Material	\$2,745,841.78	\$0.00	\$2,745,841.78	\$170,830.00		\$2,818,441.78
41	BP procur	\$288,750.00	\$0.00	\$288,750.00	\$0.00	\$0.00	\$288,750.00
36	CA fab	\$3,850.00	\$0.00	\$3,850.00	\$0.00	\$0.00	\$3,850.00
21	CBL final	\$38,500.00	\$0.00	\$38,500.00	\$0.00	\$0.00	\$38,500.00
19	CBL proto 1	\$19,250.00	\$0.00	\$19,250.00	\$19,250.00	\$0.00	\$19,250.00
20	CBL proto 2	\$19,250.00	\$0.00	\$19,250.00	\$0.00	\$0.00	\$19,250.00
22	CBL rework	\$0.00	\$0.00	\$0.00	\$0.00	\$0.00	\$3,850.00
35	CC fab	\$3,850.00	\$0.00	\$3,850.00	\$0.00	\$0.00	\$3,850.00
37	CONE procur	\$3,850.00	\$0.00	\$3,850.00	\$0.00	\$0.00	\$3,850.00
38	COOL procur	\$7,700.00	\$0.00	\$7,700.00	\$0.00	\$0.00	\$7,700.00
27	DAQ Purch	\$19,250.00	\$0.00	\$19,250.00	\$0.00	\$0.00	\$19,250.00
17	DC final	\$451,687.50	\$0.00	\$451,687.50	\$0.00	\$0.00	\$451,687.50
15	DC proto 1	\$0.00	\$0.00	\$0.00	\$0.00	\$0.00	\$26,400.00
16	DC proto 2	\$29,700.00	\$0.00	\$29,700.00	\$29,700.00	\$0.00	\$29,700.00
48	DC proto 3	\$118,800.00	\$0.00	\$118,800.00	\$118,800.00	\$0.00	\$118,800.00
18	DCtest station	\$19,250.00	\$0.00	\$19,250.00	\$0.00	\$0.00	\$19,250.00
42	Insertion parts	\$3,850.00	\$0.00	\$3,850.00	\$0.00	\$0.00	\$3,850.00
40	Installation procur	\$3,850.00	\$0.00	\$3,850.00	\$0.00	\$0.00	\$3,850.00
34	KM final	\$5,775.00	\$0.00	\$5,775.00	\$0.00	\$0.00	\$5,775.00
33	KM proto	\$1,925.00	\$0.00	\$1,925.00	\$0.00	\$0.00	\$1,925.00
31	L final	\$19,250.00	\$0.00	\$19,250.00	\$0.00	\$0.00	\$19,250.00
30	L proto	\$9,625.00	\$0.00	\$9,625.00	\$0.00	\$0.00	\$9,625.00
49	LS final	\$19,250.00	\$0.00	\$19,250.00	\$0.00	\$0.00	\$19,250.00

# 'Enterprise' Labor Summaries



- **Engineering labor**
  - ~ 13.5 FTEs
- **Technical labor**
  - ~ 7.5 FTEs
- **Management & Management support**
  - ~ 3 FTEs
  
- **Costed Labor**
  - **Project** ~3.5M (up by 0.5M from last year due to stretch)
- **Contributed labor**
  - **BNL** ~1.2M (spread over ~3 years)
  - **LBL** ~2.5M (n.b. including 0.75 M completed in FY04-FY06)  
(remainder spread over ~4 years)

# Checkup on Last FYears R&D Activities



- **Significant activities studied in FY06 included:**
  - ✓ QA & test of MimoSTAR II chips from Strasbourg
  - ✓ Conceptual design of readout boards for the Strasbourg chips
  - 1/2 Prototype ladders to support the chips
  - ✓ DAQ interface prototype
  - Develop AI clad cable technology
  - Conceptual Design of the kinematic mounts to hold the ladders
  - ✓ R&D for MimoSTAR III chip
- **Expenses**
  - ~ 100K Procurements
  - ~ 100K Engineering Research Salaries
  - ~ 100K Contributed Engineering



- **Significant activities to be studied in FY07 include:**
  - QA & test of MimoSTAR III chips from Strasbourg
  - Prototype readout boards for the Strasbourg chips
  - Prototype ladders to support the chips
  - Conceptual Design of the kinematic mounts to hold the ladders
  - Carbon Fiber engineering research
  - Live Beam tests in STAR using MimoSTAR II chips
  - Initial discussion of the beam pipe
  
- **Expenses**
  - ~ 150K Procurements
  - ~ 500K Engineering Research (guess, depends on continuing resolution)
  - ~ 150K Contributed Engineering

- **Significant activities to be studied in FY08 include:**
    - QA & test of the MimoSTAR IV chips from Strasbourg
    - Live Beam tests in STAR using MimoSTAR III chips and prototype kinematic mounts
    - Integration studies for the support of the HFT and Cone modifications
    - Design kinematic mount prototype & test
    - Development of alignment and calibration techniques
    - Design and test of the thin walled beam pipe in STAR
    - Develop and test interface to STAR DAQ
    - R&D for the Ultra Chip
  - **Expenses**
    - ~ 800K Procurements (files show 650K for MimoSTAR IV fab run)
    - ~ 900K Engineering Research Salaries
    - ~ 900K\* Contributed Engineering
- \* not realistic

# Milestones in 2009 and Beyond



- **Prototype Detector Module Element in Beam** 1Q '09
- **Full Prototype Detector in beam (4 msec)** 1Q '10
- **Cable for Ultra Chips** 4Q '10
- **Readout Boards complete** 4Q '10
- **Ladder and Ladder Support** 4Q '10
- **DAQ Interface** 4Q '10
- **Ultra Chip testing complete** 1Q '11
- **Complete Ultra Detector – start testing** 2Q '11
- **Metrology** 3Q '11
- **Installation in STAR** 4Q '11
- **Ultra Detector Installed, RHIC beam on** 4Q '11 / 1Q '12

- **We have a compelling Scientific Program**
- **We have innovative, new, technology that works**
- **IPHC/Strasbourg has made large contributions to the Enterprise**
- **There are interesting challenges in putting the technology to work**
- **A vigorous R&D program is appropriate**
- **We have a reasonable project management plan**