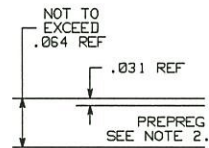
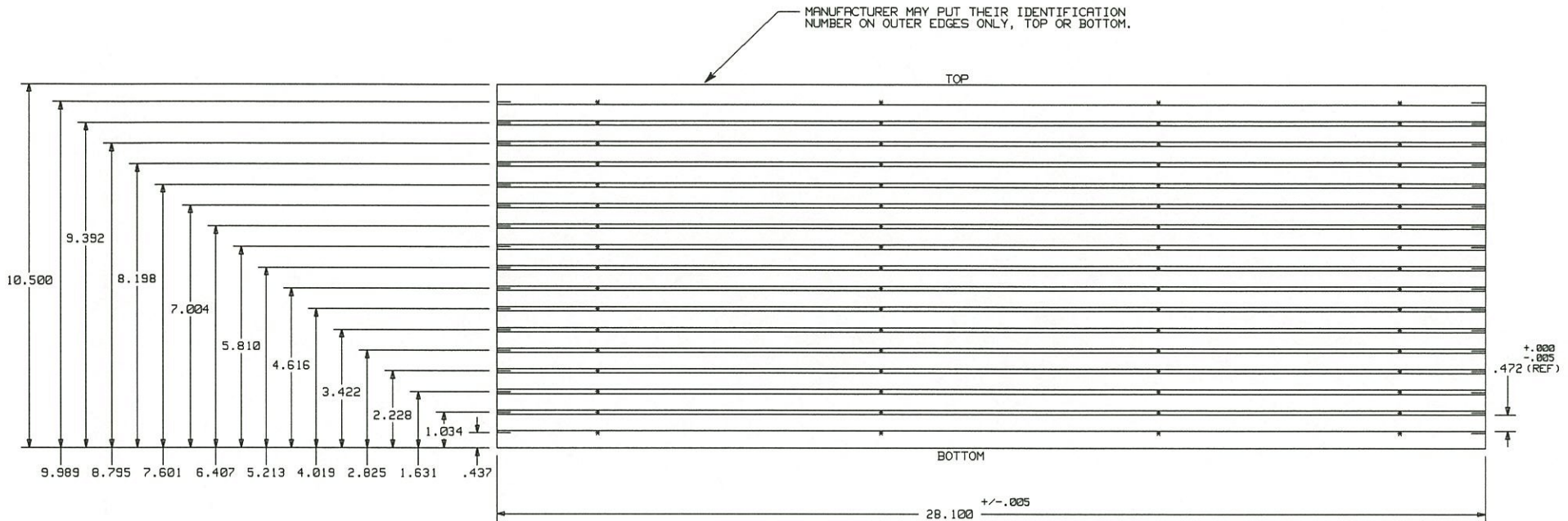


REV.	CHANGES	DRAWN	DATE	CHKD.	DATE



LAYER 1 (WIRE MT. PADS) } SEE DRAWING 24A4503 E-2
 LAYER 2 (PADS AND TRACES) } FOR DRILLING LAYERS 1
 LAYER 3 (NO COPPER) } AND 2. (5,440 HOLES)
 LAYER 4 (HV PADS) } SEE DRAWING 24A4503 E-3
 } FOR DRILLING LAYERS 1
 } THRU 4. (34 HOLES)

NOTES:

- BOARD MATERIAL: .031 THICK G10 PER MIL-P-55617 FL-GEN 031C-1/1-A1A (1 OZ. COPPER EACH SIDE). THIS IS A MULTILAYER BOARD (4 LAYERS). TOTAL THICKNESS NOT TO EXCEED .064.
- PREPREG THICKNESS TO BE DETERMINED BY MANUFACTURER PER IPC-L-109A OR MIL-P-55617.
- PLEASE NOTE THAT THERE IS NO COPPER ON LAYER 3.
- BOARD PANEL SIZE IS 10.500 +/- .010 X 28.100 +/- .005. SINGLE BOARD SIZE IS .472 +/- .000/- .010 X 28.100 +/- .005. DIMENSIONS ARE IN INCHES.
- * = APPROXIMATE PLACEMENT OF .050 TABS. SLOTS TO BE .125 WIDE.
- REFERENCE DRAWINGS:
 24A4502 E-1 a000896e1 HOLE SCHEDULE - SINGLE BOARD
 24A4503 E-2 a000896e2 HOLE SCHEDULE - PANEL OF 16 (BLIND VIAS)
 24A4503 E-3 a000896e3 HOLE SCHEDULE - PANEL OF 16
 24A4502 M-1 a000896m1 BOARD OUTLINE - SINGLE BOARD

D I:		TITLE STAR TPC			
I I:		INNER SECTOR ELECTRONICS			
T III:		GATED GRID WIRE MOUNT BOARD - PANEL OF 16			
SHOW ON:		BOARD OUTLINE - 24A4501 U-2 (A000896U2)			
ACCOUNT NUMBER	8052-24	DRAWN	DATE	LAWRENCE BERKELEY LABORATORY	
SERIAL NUMBER		CHECKED	DATE	UNIVERSITY OF CALIFORNIA	
DATE ISSUED		APPROVED	DATE	OFFICE OF ELECTRONICS ENGINEERING	
DATE RECD.		ENGINEER	JIM HUNTER	FILE NO.	a000896m2
DEL. TO:		SCALE	NONE	SIZE	3
				DRAWING NO.	24A4503 M-2
				REV.	
					SHEET 2 OF 2