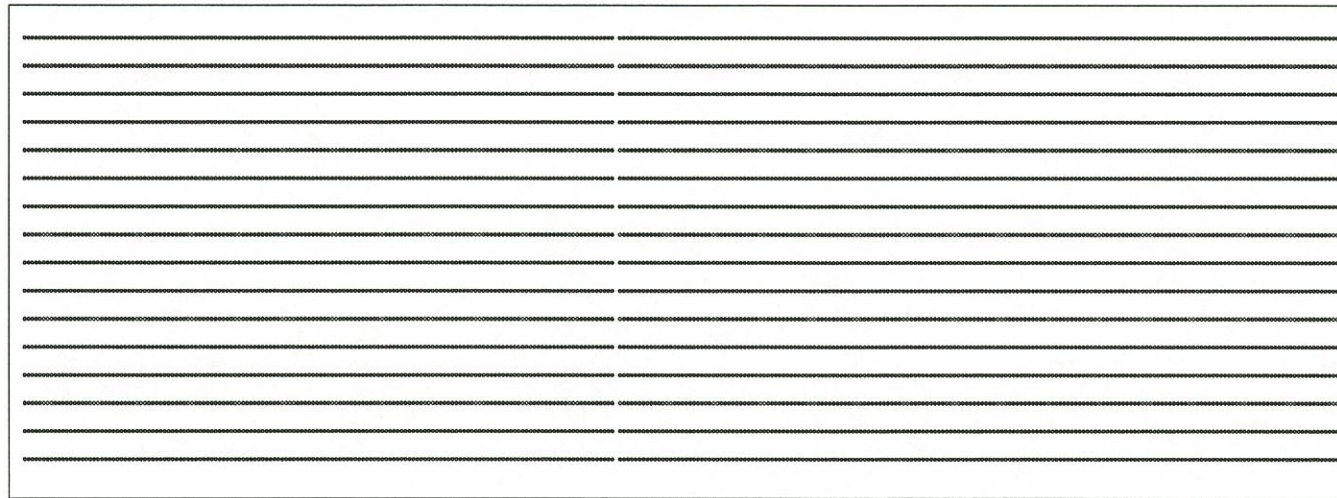


REV.	CHANGES	DRAWN	DATE	CHKD.	DATE

LAYER TWO VIEW

SCALE: NONE

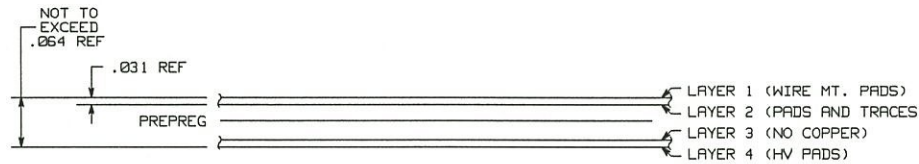
TOP



INNER RADIUS

MANUFACTURER MAY PUT THEIR IDENTIFICATION NUMBER ON OUTER EDGES ONLY, TOP OR BOTTOM.

OUTER RADIUS



USE .015 DIA HOLE (5,440 HOLES) THESE HOLES ONLY GO THROUGH LAYERS 1 AND 2 (BLIND VIAS). SEE THIS DRAWING.

USE .020 DIA HOLE (32 HOLES). DRILL THESE HOLES AFTER ASSEMBLY OF ALL LAYERS, SEE DRAWING 24A4503 E-3.

NOTES:

- BOARD MATERIAL: .031 THICK G10 PER MIL-P-55617 FL-GEN 031C-1/1-A1A (1 OZ. COPPER EACH SIDE). THIS IS A MULTILAYER BOARD (4 LAYERS). TOTAL THICKNESS NOT TO EXCEED .064.
- PLEASE NOTE THAT THERE IS NO COPPER ON LAYER 3.
- THIS BOARD TO BE THROUGH HOLE PLATED.
- SPECIFIED HOLE DIA. SIZES ARE FOR FINISHED HOLES AFTER PLATING.
- BOARD SIZE IS 10.500 +/- .010 X 28.100 +/- .005. DIMENSIONS ARE IN INCHES. BOARD OUTLINE DRAWING IS 24A4503 M-2 (a000896m2).
- SOLDERMASK IS NOT USED ON THIS BOARD.
- REFERENCE DRAWINGS:  
 24A4502 M-1 a000896m1 BOARD OUTLINE - SINGLE BOARD  
 24A4503 M-2 a000896m2 BOARD OUTLINE - PANEL OF 16  
 24A4502 E-1 a000896e1 HOLE SCHEDULE - SINGLE BOARD  
 24A4503 E-3 a000896e3 HOLE SCHEDULE - PANEL OF 16

HOLE SCHEDULE		
CODE	HOLE DIA.	COUNT
NONE	.015	5,440

D I S T		TITLE STAR TPC	
I:		INNER SECTOR ELECTRONICS	
II:		GATED GRID WIRE MOUNT BOARD - PANEL 0F 16	
III:		HOLE SCHEDULE - 24A4501 U-2 (BLIND VIAS)	
SHOWN ON		LAWRENCE BERKELEY LABORATORY	
ACCOUNT NUMBER 8052-24	DRAWN STIRAKLINEN	DATE 4/08/94	UNIVERSITY OF CALIFORNIA
SERIAL NUMBER	CHECKED	DATE	OFFICE OF ELECTRONICS ENGINEERING
DATE ISSUED	NO. REGD.	APPROVED	FILE NO.
DATE RECD.		JIM HUNTER	SIZE 3
DEL. TO	SCALE NONE	DRIVING NO. 24A4503 E-2	REV.
		CB,E14	SHEET 2 OF 3