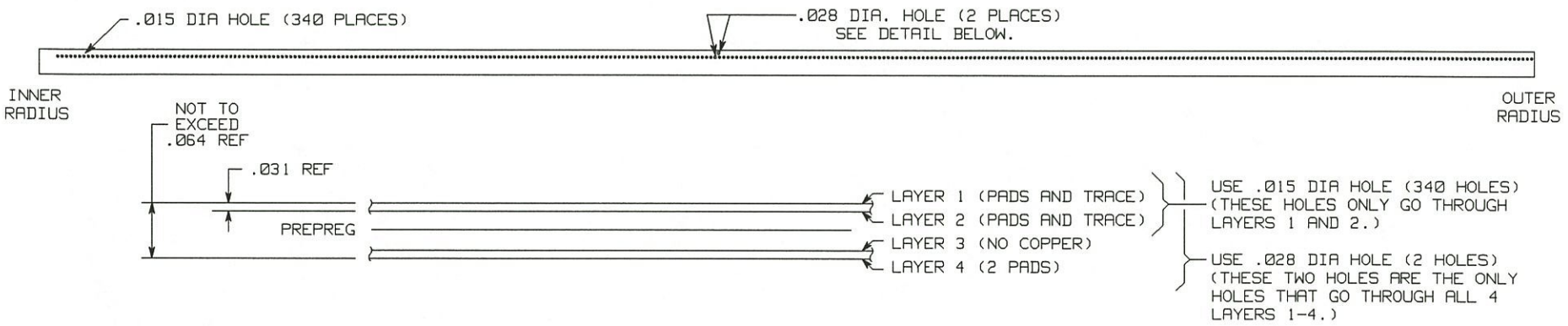
REV.	CHANGES	DRAWN	DATE	CHKD.	DATE

LAYER ONE VIEW



NOTES:

1. BOARD MATERIAL: .031 THICK G10 PER MIL-P-55617 FL-GEN 031C-1/1-A1A (1 OZ. COPPER EACH SIDE). THIS IS A MULTILAYER BOARD (4 LAYERS). TOTAL THICKNESS NOT TO EXCEED .064.
2. MANUFACTURER MAY NOT PUT ANY IDENTIFICATION NOMENCLATURE ON PRINTED CIRCUIT BOARD.
3. PLEASE NOTE THAT THERE IS NO COPPER ON LAYER 3.
4. THIS BOARD TO BE THROUGH HOLE PLATED. SEE DETAIL FOR BLIND VIAS (340 HOLES).
5. SPECIFIED HOLE DIA. SIZES ARE FOR FINISHED HOLES AFTER PLATING.
6. BOARD SIZE IS .472 +.000/-.010 X 28.100 +/-.005. DIMENSIONS ARE IN INCHES. BOARD OUTLINE DRAWING IS 24A4502 M-1 (a000896m1).
7. SOLDERMASK IS NOT USED ON THIS BOARD.
8. REFERENCE DRAWINGS:

24A4502 M-1	a000896m1	BOARD OUTLINE - SINGLE BOARD
24A4503 M-2	a000896m2	BOARD OUTLINE - PANEL OF 16
24A4503 E-2	a000896e2	HOLE SCHEDULE - PANEL OF 16 (BLIND VIAS)
24A4503 E-3	a000896e3	HOLE SCHEDULE - PANEL OF 16

DIST I:		TITLE	STAR TPC		
DIST II:			INNER SECTOR ELECTRONICS		
DIST III:			GATED GRID WIRE MOUNT BOARD - SINGLE BD.		
SHOWN ON			HOLE SCHEDULE - 24A4501 U-1 (A000896U1)		
ACCOUNT NUMBER	8052-24	DRAWN STIRKKINEN	DATE 4/8/94	LAWRENCE BERKELEY LABORATORY	
SERIAL NUMBER		CHECKED	DATE	UNIVERSITY OF CALIFORNIA	
DATE ISSUED	NO. REQD.	APPROVED	DATE	OFFICE OF ELECTRONICS ENGINEERING	
DATE REQD.		ENGINEER	JIM HUNTER	FILE NO. a000896e1 / SIZE 2 / DRAWING NO. 24A4502 E-1 / REV.	
DEL. TO		SCALE	NONE	E2, C3	SHEET 1 OF 3