

ALICE128C TECHNICAL REPORT

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1 Introduction

ALICE128C is a AMS1.2 CMOS fullcustom ASIC designed to fulfill the requirements of the readout electronics for the Silicon Strip Detectors (SSD) of the ALICE experiment. It is a 128 channels chip. Each channel amplifies, shapes and stores as a voltage signal the charge deposited on a strip of the detector. An analog multiplexer allows a sequential readout of the data through an output buffer shared by the 128 channels. A slow control mechanism using the JTAG protocol was implemented to bias accurately the different analog blocks and to control the shaping time and a test pulse generator. We chose to implement the three most perturbing logic signals (the readout clock, the hold signal and test requesting signal) by use of LVDS (Low Voltage Differential Signal) levels to reduce the noise they may induce.

2 ALICE128C block diagram

Figure 1 gives the block diagram of ALICE128C. Each block is now described briefly.

2.1 Block diagram of the amplifying channel

Figure 2 shows the block diagram of the amplifying channel. The input current pulse is amplified shaped and stored on C_{HOLD} . The shaping time is adjustable from $1.4\mu s$ to $1.8\mu s$ by tuning the V_{shaper} voltage from $2V$ to $-0.5V$. This is done using the bias generator through a 8 bits voltage DAC.

The bias currents I_{preamp} , I_{shaper} , I_{inbuff} and the preamplifier feedback MOS resistor (V_{preamp}) are also tuned using the bias generator.

The whole gain of the channel is $48mV/MIP$ assuming 22000 electrons for one MIP. The input range is $\pm 13MIPs$.

2.2 Analog output multiplexer and Output buffer controller

The output analog multiplexer is made of two 128 bits shift registers plus an extra bit flip-flop cell (Tempo) as explained on figure 3. The *OnOff shift register* controls the on/off switching mechanism which switches on the intermediate buffers only during the readout cycle. More accurately, only 3 buffers are switched on, the buffer " n " corresponding to the channel being read (of course!) and the two adjacent buffers which surround it, buffer " $n - 1$ " and buffer " $n + 1$ ". At the same time, the buffer " $n - 2$ " is switched off and the buffer " $n + 2$ " is switched on. This means that only 4 intermediate buffers are dissipating power during the readout. The first memory cell named *Tempo* is used to delay by one clock pulse the TOKENIN signal in order to switch on the first two intermediate buffers before beginning the readout cycle. The output buffer must be also switched on during the readout. This is made through the *Outbuff controller*. This controller is made of one memory cell set at 1 when reading the first channel and set at 0 after reading the last channel. Note that the TOKENOUT signal is picked up just before the last channel in order to allow a daisy chain of several ALICE128C circuits without requiring an extra clock pulse between two chips. The only restriction is that an extra clock pulse after the arrival of the TOKENIN is required for the first chip of the chain and an another extra clock pulse is required after reading the last channel of the last chip of the chain in order to switch off the buffers of this last chip. This functional mode corresponds to the **normal mode**.

An another functional mode, named **serial mode** is provided by ALICE128C. The choice between the two modes

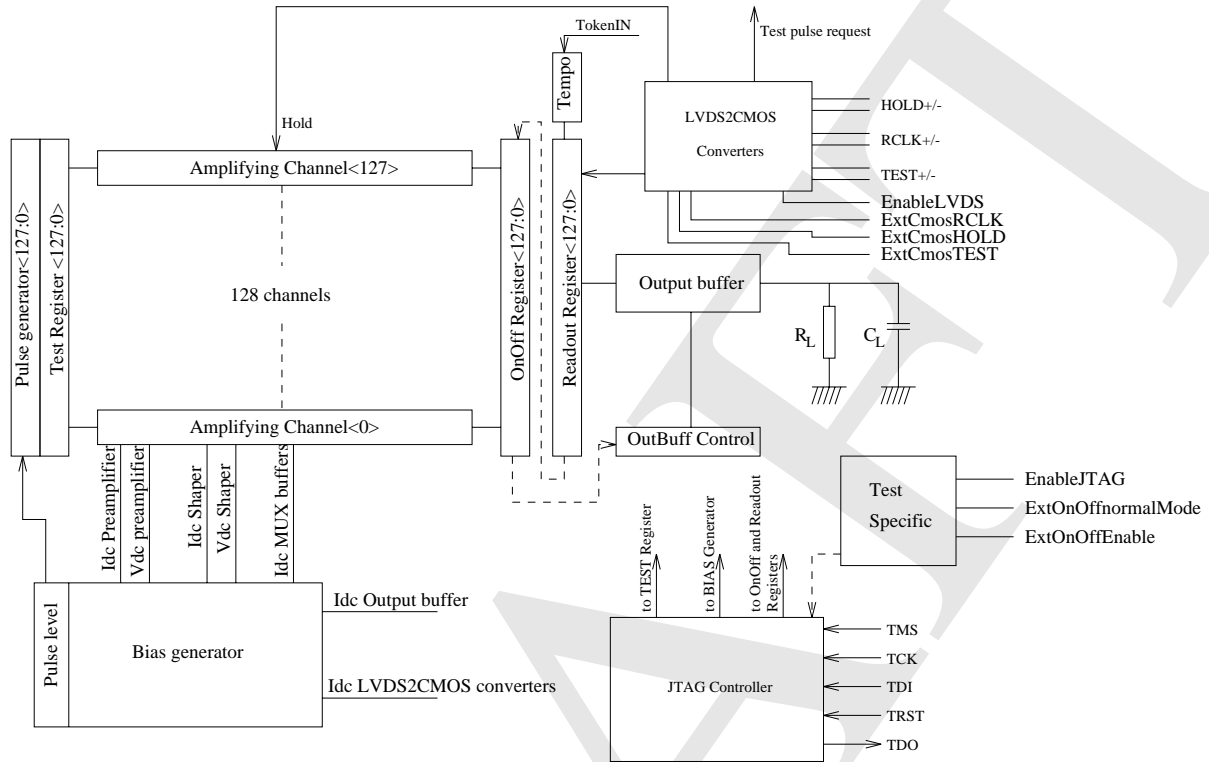


Figure 1: ALICE128C main block diagram

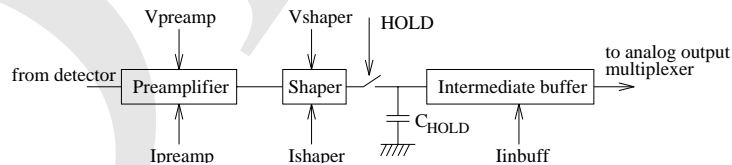


Figure 2: Amplifying channel diagram

is made through the JTAG controller. In this mode, the memory cell *Tempo*, the shift register *Readout* $\langle 127 : 0 \rangle$, the shift register *OnOff* $\langle 127 : 0 \rangle$ and the memory cell *Outbuff controller* are connected in serie as a huge 258 shift register in order to be able to write any 258 bits stream. During writing, all the buffers are automatically disabled, and the buffers corresponding to bits set to “1” are enabled at the end of the sequence. This mode can be used for test purpose or when using the pulse generator in order to connect the channel under test to the analog output.

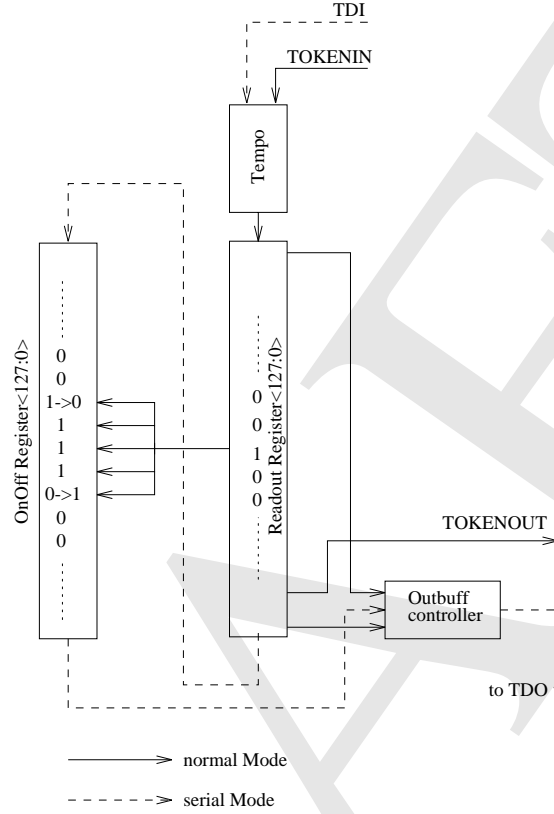


Figure 3: Analog output multiplexer and Output buffer controller blocks diagram

2.3 Bias generator and Test pulse level generator

The bias generator provides 5 dc currents to bias all the analog modules and two dc voltages to tune the MOS feedback resistors on the preamplifier and the shaper. The dc currents are provided by 8 bits current DACs. Since the dc voltages bias high impedance MOS gates, they are done by using similar current DACs which feed a $9.8K\Omega$ resistor.

The test pulse level is chosen by setting the current the pulse generator switches to provide the desired positive or negative pulse. A linear relation exists between the value of this current and the pulse level in MIPs. This current is also provided by a 8 bits current DAC.

The setting of all these DACs is made through the JTAG controller. The 7 DACs of the bias generator must be set sequentially in the following order :

1. Ipreamp \rightarrow Preamplifier biasing current
2. Vpreamp \rightarrow Preamplifier feedback resistor
3. Ishaper \rightarrow Shaper biasing current
4. Vshaper \rightarrow Shaper feedback resistor
5. Iinbuff \rightarrow Intermediate buffer biasing current
6. Ioutputbuff \rightarrow Output buffer biasing current

7. Ilvds \rightarrow LVDS2CMOS converter biasing current

Note that the setting of the test pulse level has to be done separately because while it corresponds to a dc level it has not a biasing function!

Table 1 gives the simulated nominal and extreme values for all the currents. The corresponding nominal hexadecimal value to set into the DAC is also given.

Name	Min (μA)	Nominal (μA)	Max (μA)	Step (μA)	Nominal Hexa	Note
Ipreamp	0	100	255	1	H64	source
Vpreamp	$0 \equiv -2V$	$160 \equiv -400mV$	$255 \equiv 0.5V$	$1 \equiv 9.8mV$	Ha0	source, $R = 9.8K\Omega$
Ishaper	0	30	127.5	0.5	H1e	source
Vshaper	$0 \equiv 2V$	$120 \equiv 850mV$	$255 \equiv -0.5V$	$1 \equiv 9.8mV$	H78	sink, $R = 9.8K\Omega$
Iinbuff	0	25	127.5	0.5	H19	source
Ioutputbuff	0	100	255	1	H64	sink
Ilvds	0	10	127.5	0.5	H0a	source
Ipulse	$0 \equiv 0MIP$	-	$255 \equiv 14.5MIPs$	$1 \equiv 56.7mMIP$	-	source

Table 1: Bias generator and test pulse level generator

2.4 Pulse generator and Test register

The pulse generator switches the current setting in the *test pulse level generator* from one branch of a differential stage to the other branch. This switching is asked by changing the level of the LVDS TEST signal. **A positive front edge asks for a positive test pulse while a negative front edge asks for a negative test pulse.**

Through the JTAG controller, one can write in the 128 bits test shift register to set the channels where to inject the test pulse. A 1 means that the test pulse will be injected into the corresponding channel.

Note that the total switched current during a test pulse injection must not exceed the value of $27mA$. This means that when injecting the highest pulse ($\equiv 512\mu A$), one must careful to not select more than $27000/512 \simeq 50$ channels.

2.5 Output buffer

The output buffer is shared by the 128 channels and is assumed to be loaded by $R_L = 100\Omega$ in parallel with $C_L = 20pF$. It is a unity gain, single ended buffer designed to provide the analog output signal in $30ns$ to $50ns$ in order to allow a readout rate of $10MHz$. Its open-loop gain is around $65dB$ which means that its contribution to the whole non-linearity can be neglected.

The buffer can be switched off. In this case, its output is under high impedance. With $R_L = 100\Omega$ and $C_L = 20pF$, the switching on/off is established in less than $50ns$ which allows a daisy chaining of several ALICE128C circuits.

2.6 LVDS2CMOS converter

Three logic signals have been implemented through the LVDS (Low Voltage Differential Signal) level. They are the *Read clock signal*, the *HOLD signal* and the *TEST signal*. The *LVDS2CMOS converters* converts the LVDS level ($\pm 100mV$ around a dc level of $1.2V$) into the internal CMOS level ($\pm 2V$). They have been designed to work at a frequency up to $30MHz$.

To use these converters, the *EnableLVDS* signal must be set to 1. Otherwise, the three previous signals must be given through using a $\pm 2V$ level through the three external signals named *ExtCmosRCLK*, *ExtCmosHOLD* and *ExtCmosTEST*. This feature has been provided mainly for test purpose.

2.7 JTAG controller

The JTAG controller is used to set the working configuration of ALICE128C (bias setting, Token bypass,...). It is also used for test purpose (test pulse level setting, functional test,...). It is implemented with the JTAG IEEE Standard 1149.1. Table 2 gives the nine instruction codes implemented in the chip. Table 3 defines the height Test Data Registers (TDR).

Remarks

1. **Reset (TRSTB)** : After activating TRSTB (low) :

Name	Code	Note
Bypass	11111	mandatory
Extest	00000	mandatory
Sample/Preload	00101	mandatory
Bias_gen	01001	user defined
Pulse_gen	01101	user defined
Test_reg	10001	user defined
Read_reg	10101	user defined
OnOff_enable	11001	user defined
Token_enable	11101	user defined

Table 2: Instruction Register (IR) - 5bits

Name	Size (bits)	Note
Bypass Register	1	mandatory
Boundary Scan Register	8	mandatory
Bias Register	56	user defined
Pulse Level Register	8	user defined
Test Register	128	user defined
Read Register	258	user defined
OnOffEnable Register	1	user defined
TokenEnable Register	1	user defined

Table 3: Test Data Registers (TDR)

- the JTAG controller is in the reset state
- all ALICE128C registers are reseted (bias reg., test reg.,...)
- the TokenIn is bypassed to the TokenOUT ($TokenOUT = TokenIN$).
- the intermediate buffers and the output buffer on/off switching logics are enabled ($OnOffEnable\ Register = 1$)

2. **Normal functional mode** : The following steps have to be executed in this order with the JTAG protocol

- Bias setting
- Token bypass switching off
- JTAG controller placed in the reset state

3. **Test Modes** : In order to use the on chip test features, you can perform the following steps :

- Bias setting
- Token bypass switching off
- Test pulse level setting
- Tested channels choice (Test register - Logical 1 to select the corresponding channel)
- After these settings, place the JTAG controller in the **Run_Test/idle** state
- Inject the pulse through the LVDS_TEST external logic signal
- Perform the readout (TokenIN + Read clock)

You can also test only one channel by setting a logical 1 corresponding to the tested channel in the Test Register, the Readout Register, the OnOff Register and the Outbuff Control Register. These three last registers are merged in the 258 bits Read Register (see table 3 and figure 1).

The mandatory Boundary Scan Register is a 8 bits register composed by the following signals : TOKENOUT, HOLDB and HOLD (picked up at the output of LVDS2CMOS converter), TESTB and TEST (picked up at the output of LVDS2CMOS converter), RCLK and RCLKB (picked up at the output of LVDS2CMOS converter), TOKENIN.

4. An OnOffEnable Register (see table 3) has been implemented for specific electrical tests (designers additional test feature).

2.8 Test specific module

Every functional command pass through the JTAG controller. Any problem in the controller would prevent the test of the circuit. So to secure the design, ALICE128C provides a feature to “bypass” the JTAG controller. It is enable by setting at 0 the *EnableJTAG* signal. In this case, one must use the *ExtOnOffnormalMode* to select between the normal functional mode or the serial mode (see section 2.2 for an explanation about these two modes). As extra feature, one can disable the biasing of the buffers (intermediate and output buffers) by setting at 0 the *ExtOnOffEnable* signal.

Note that, in serial mode, it is possible to write any binary stream into the huge 258 bits shift register. But it is not possible to read completely this register as it is the case when using the JTAG controller. One can read this the first 128 bits of this huge register through the *TOKENOUT*!

3 ALICE128C physical implementation

Figure 4 shows the layout of ALICE128C. The main dimensions are $W = 6080\mu\text{m}$ for the width and $L = 8643\mu\text{m}$ for the length. The pitch of the pads connected to the detector is $44\mu\text{m}$. Two sets of 128 pads are provided, each set is made of two columns of 64 pads.

The 43 pads at the back of the circuit have a pitch of $136\mu\text{m}$. They are summarized in table 4.

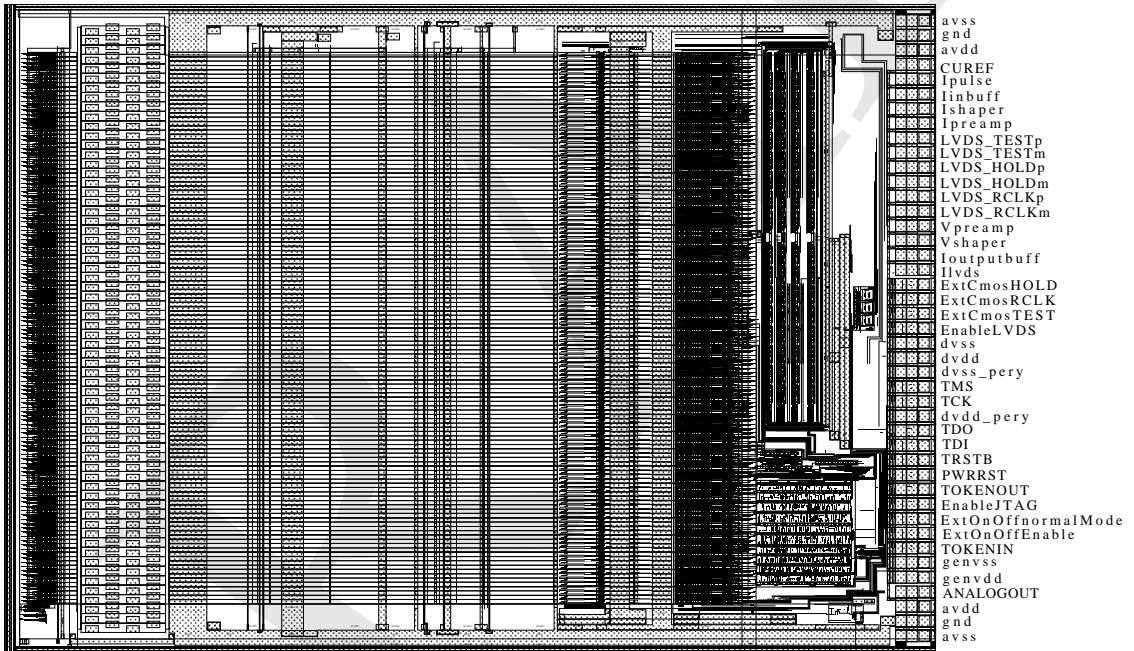


Figure 4: ALICE128C layout

Pin name	Operation	Note
avss	-2V analog	Must be always connected
gnd	0V analog ground	
avdd	+2V analog	
CUREF	analog current reference for DACs	56K Ω connected to avdd
Ipulse	current for test pulse level	for test purposes only
Iinbuff	bias current for intermediate buffers	for test purposes only
Ishaper	bias current for shaper	for test purposes only
Ipreamp	bias current for preamplifier	for test purposes only
LVDS_TESTp	differential + LVDS Test pulse	0 \rightarrow 1 for positive pulse
LVDS_TESTm	differential - LVDS Test pulse	1 \rightarrow 0 for negative pulse
LVDS_HOLDp	differential + HOLD pulse	
LVDS_HOLDm	differential - HOLD pulse	
LVDS_RCLKp	differential + Read out CLock pulse	
LVDS_RCLKm	differential - Read out CLock pulse	
Vpreamp	bias voltage for preamplifier	for test purposes only
Vshaper	bias voltage for shaper	for test purposes only
Ioutputbuff	bias current for the output buffer	for test purposes only
Ilvds	bias current for LVDS2CMOS converter	for test purposes only
ExtCmosHOLD	Cmos level HOLD	for test purposes only (pulled up to +2V)
ExtCmosRCLK	Cmos level Read out CLock	for test purposes only (pulled up to +2V)
ExtCmosTEST	Cmos level TEST	for test purposes only (pulled up to +2V)
EnableLVDS	enable LVDS	for test purposes only (pulled up to +2V)
dvss	-2V digital	
dvdd	+2V digital	
dvss_pery	-2V digital peripheral supply for pads	
TMS	JTAG Mode Select	(pulled up to +2V)
TCK	JTAG ClocK	
dvdd_pery	+2V digital peripheral supply for pads	
TDO	JTAG Data Output	
TDI	JTAG Data Input	(pulled up to +2V)
TRSTB	General RESET	Active at low level (pulled up to +2V)
PWRRST	POWeR ReSeT after power up	RC on digital power supply
TOKENOUT	Readout TOKEN OUTput	
EnableJTAG	enable JTAG	for test purposes only (pulled up to +2V)
ExtOnOffnormalMode	normal Mode select	0 \rightarrow serial mode (pulled up to +2V)
ExtOnOffEnable	Buffers enabling	(pulled up to +2V)
TOKENIN	Readout TOKEN INput	One extra RCLK pulse before reading
genvss	-2V for the test pulse generator	
genvdd	+2V for the test pulse generator	
ANALOGOUT	ANALOG OUTput	$Z_c = 100\Omega // 20pF$
avdd	+2V analog	
gnd	0V analog ground	
avss	-2V analog	Must be always connected

Table 4: Pad list - All logic levels, except LVDS, are $\pm 2V$ with respect to gnd.