JTAG notes

# JTAG

A JTAG interface is a special four/five-pin interface added to a chip, designed so that multiple chips on a board can have their JTAG lines daisy-chained together if specific conditions are met, and a test probe need only connect to a single "JTAG port" to have access to all chips on a circuit board. The connector pins are

1. TDI (Test Data In)

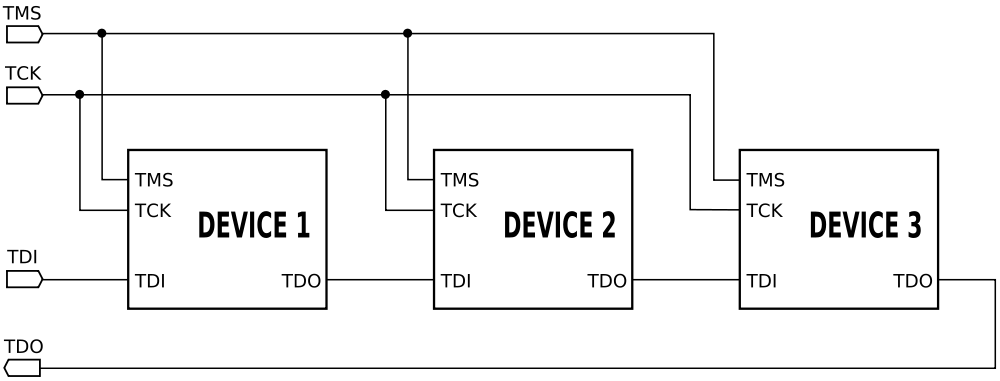
2. TDO (Test Data Out)

3. TCK (Test Clock)

4. TMS (Test Mode Select)

5. TRST (Test Reset): optional

Test reset signal is not shown in the image



# CORELIS (old slow control)

The control signals are generated by Corelis VME module. In our case 4 JTAG ports are used for the 4 parts of the detector and 1 JTAG port is used for the programming of FPGAs.

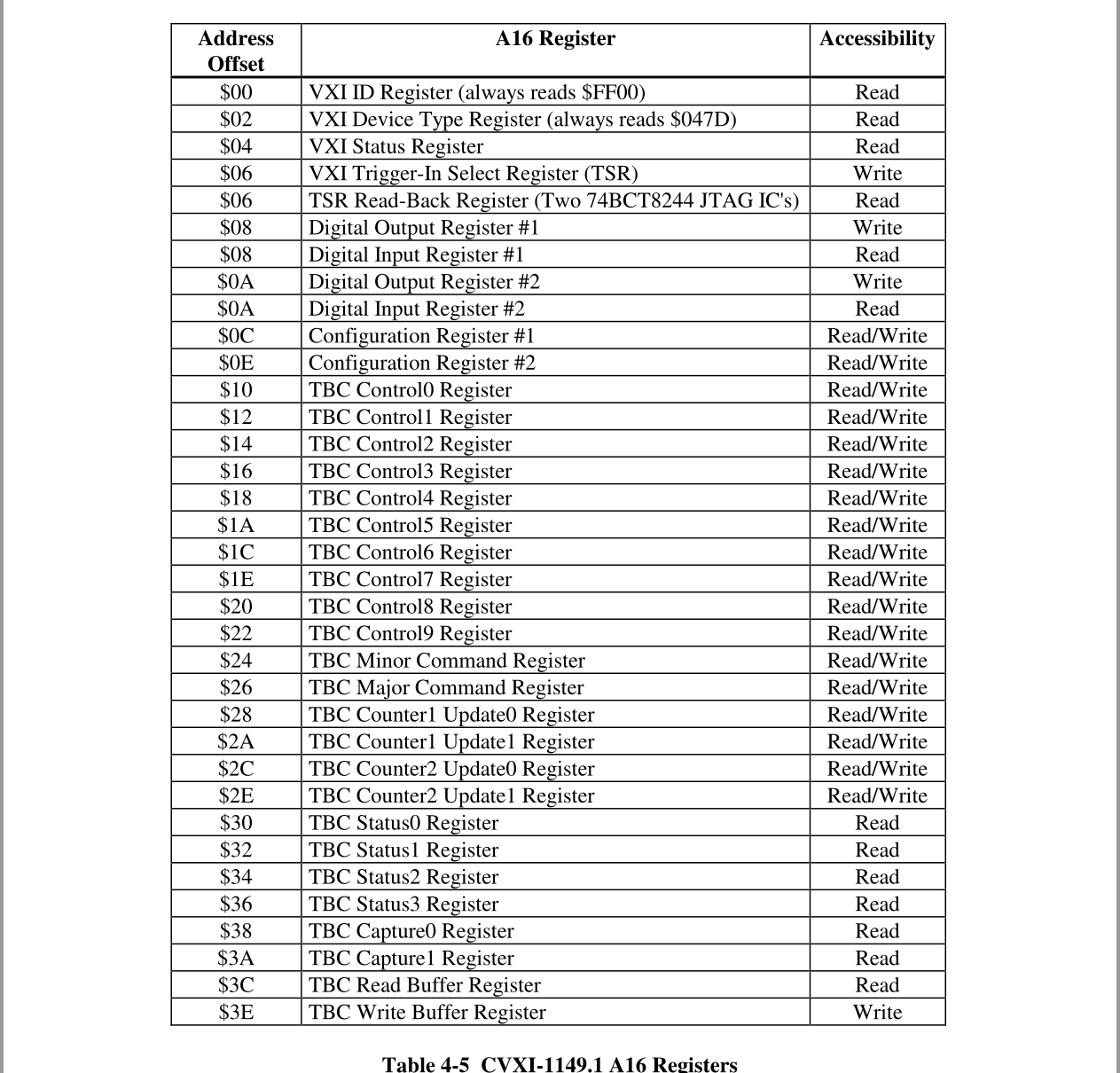
The integrated circuit which is the core of the CVME module is the TI 74ACT8990. The required signals of the JTAG serial-test bus –TCK, TMS, TDI, and TDO can be connected from the test bus controller (TBC) to a target device without additional logic. The TBC operates under the control of a host microprocessor/microcontroller via the 5-bit address bus and the 16-bit read/write data bus. In addition to control and status registers, the TBC contains two command registers, a read buffer, and a write buffer.



## Registers

Thirty two 16 bit registers are provided. 10 - 3e are registers of SN74ACT8990 TBC.

See the Figure below.



## Functions

The functions provided can be classified in two categories:

1. Scanning

The Scanning functions provide a higher level access to the operation of the SN74ACT8990 IC.

**scan\_ir(unsigned short \*output, unsigned short length, unsigned short \*input)**

**scan\_dr(unsigned short \*output, unsigned short length, unsigned short \*input)**

**circulate\_dr(unsigned short length, unsigned short \*data)**

1. Utility/Low-level access

The utility/low-level functions are as follows:

**hard\_reset(unsigned short target, unsigned short divider)**

**wait\_jtag\_state(short state)**

**soft\_reset(void)** //not used

**check\_ready(void)** //not used

**wait\_for\_ready(void)**

**write\_tbc(unsigned short register\_offset, unsigned short data)**

**read\_tbc(unsigned short register\_offset, unsigned short \*data)** //not used

**write\_buf(unsigned short data)**

**read\_buf(unsigned short \*data)**

# ****jtagCommon.h/****jtagCommon.c

There are 6 functions are used heavily by jtag communications with ALICE128, READOUT, COSTAR and CONNEXION.

**init\_stream(unsigned short \*, unsigned short)**

**get\_stream(unsigned short \*,unsigned short, unsigned short)**

**set\_stream(unsigned short \*, unsigned short, unsigned long, unsigned short)**

**The above 3 functions has little to do with the hardware.**

//Scans a bit stream into the TAP instruction register

**scan\_ir(unsigned short \*, unsigned short, unsigned short \*)**

//Scans a bit stream out the TAP data path

**scan\_dr(unsigned short \*, unsigned short, unsigned short \*)**

//Circulates a bit stream thru the TAP controller data path

**circulate\_dr(unsigned short, unsigned short \*)**

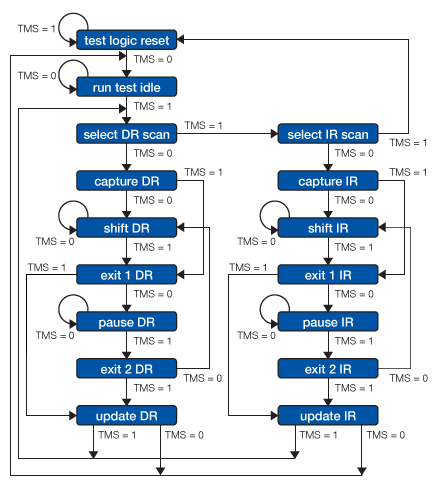
**A function invoking relation graph is shown below:**



There are also several other functions called in A128CRecord.c.

## TAP State Machine

IEEE 1149.1 describes a simple architecture for chips implementing boundary scan testing. In its minimal configuration, it provides four external pins, a clock (TCK), data in (TDI), data out (TDO) and a management signal (TMS). Collectively these pins are known as the Test Access Port (TAP).



The TAP controller, a state machine whose transitions are controlled by the TMS signal, controls the behavior of the JTAG system.

## registers

There are two types of registers associated with boundary scan. Each compliant device has one instruction register and two or more data registers.

Instruction Register – the instruction register holds the current instruction. Its content is used by the TAP controller to decide what to do with signals that are received. Most commonly, the content of the instruction register will define to which of the data registers signals should be passed.

Data Registers – there are two primary data registers, the Boundary Scan Register (BSR) and the BYPASS register. Other data registers may be present. 