5 The ladder card

5.1 Overview

The ladder card is the upgrade for the CONNEXION card (sometimes called C2D2 card) and for the ADC card.

5.2 Power management

typical	*Qty*	*5V*	*analog*	*3.3V*	*3.3V*	*2.5V*	*2.5V*	*1.2V*	
74LV125APW	2				0.20				quadruple bus buffer
74LV126APW	2				0.20				quadruple bus buffer
90LV031	12			23.00					quad cmos differential line drivers
AD7356	8					14.00			dual 12bits serial output ADC
AD8040	16		5.20						quad rail-to-rail op-amp
AFBR57M5APZ	1				210.00				optical fiber transceiver
Altera blaster	1						0.00		DEBUG altera cable
CMP04	4			0.80					quad comparator
CY7B991	1			28.40					roboclock
CY7B991	1				30.56				roboclock
DS90UR124	1				85.00				1 to 24 deserializer
DS90UR241	1				66.00				24 to 1 serializer
EP3C16FC484-6	1					11.34	21.98	42.99	FPGA
FAN2558S12X	1			43.14					low-dropout (1.7V) 1.2V regulator
LM1117MPX-2.5	2	77.66							low-dropout (1.2V) 2.5V regulator
LM1117MPX-3.3	2	376.85							low-dropout (1.2V) 3.3V regulator
LTC1662	1		0.01						dual 10bits serial input DAQ
MAX6575L	2			0.15					temperature sensor
MAX6575L	2				0.15				temperature sensor
IQD CFPS-32IB 40MHz	1					0.00			DEBUG local oscillator
UM245R	1				0.00				DEBUG usb interface
TOTAL		**909.0**	**83.2**	**351.0**	**392.7**	**123.3**	**22.0**	**43.0**	**mA**
4955		1670	416	1158	1296	308	55	52	mW

Table 54*: ladder card typical power requirement (normal operation)* [5a][6][7][8a][9][10][11][12][13][14][15]

CycloneIII FPGA require two separate 2.5V power planes (1 digital and 1 analog)

Analog voltage assumed to be 5V (as worst case) for power calculation: In old SSD, one had to adjust -2V around -2.2V and to adjust +2V around +2.5V to get -2V and +2V on all the hybrids. This was due to voltage loss along the flex cables on the ladder and to the sense cable being connected to the electronics at the end of the ladder.

maximum	*Qty*	*5V*	*analog*	*3.3V*	*3.3V*	*2.5V*	*2.5V*	*1.2V*	
74LV125APW	2				0.20				quadruple bus buffer
74LV126APW	2				0.20				quadruple bus buffer
90LV031	12			30.00					quad cmos differential line drivers
AD7356	8					20.00			dual 12bits serial output ADC
AD8040	16		6.00						quad rail-to-rail op-amp
AFBR57M5APZ	1				210.00				optical fiber transceiver
Altera blaster	1						0.10		DEBUG altera cable
CMP04	4			2.00					quad comparator
CY7B991	1			146.00					roboclock
CY7B991	1				146.00				roboclock
DS90UR124	1				105.00				1 to 24 deserializer
DS90UR241	1				90.00				24 to 1 serializer
EP3C16FC484-6	1					11.34	21.98	42.99	FPGA
FAN2558S12X	1			43.14					low-dropout (1.7V) 1.2V regulator
LM1117MPX-2.5	2	110.71							low-dropout (1.2V) 2.5V regulator
LM1117MPX-3.3	2	567.77							low-dropout (1.2V) 3.3V regulator
LTC1662	1		0.80						dual 10bits serial input DAQ
MAX6575L	2			0.40					temperature sensor
MAX6575L	2				0.40				temperature sensor
IQD CFPS-32IB 40MHz	1					18.00			DEBUG local oscillator
UM245R	1				15.00				DEBUG usb interface
TOTAL		**1357.0**	**96.8**	**557.9**	**567.6**	**189.3**	**22.1**	**43.0**	**mA**
7262		2484	484	1841	1873	473	55	52	mW

Table 55*: ladder card maximum power requirement (normal operation)* [5a][6][7][8a][9][10][11][12][13][14][15]

Analog voltage assumed to be 5V (as worst case) for power calculation: In old SSD, one had to adjust -2V around -2.2V and to adjust +2V around +2.5V to get -2V and +2V on all the hybrids. This was due to voltage loss along the flex cables on the ladder and to the sense cable being connected to the electronics at the end of the ladder.

typical	*Qty*	*5V*	*analog*	*3.3V*	*3.3V*	*2.5V*	*2.5V*	*1.2V*	
74LV125APW	2				0.20				quadruple bus buffer
74LV126APW	2				0.20				quadruple bus buffer
90LV031	12			8.00					quad cmos differential line drivers
AD7356	8					14.00			dual 12bits serial output ADC
AD8040	16		1.30						quad rail-to-rail op-amp
AFBR57M5APZ	1				0.00				optical fiber transceiver
Altera blaster	1						0.02		DEBUG altera USB-blaster cable
CMP04	4			0.80					quad comparator
CY7B991	1			28.40					roboclock
CY7B991	1				30.56				roboclock
DS90UR124	1				30.00				1 to 24 deserializer
DS90UR241	1				40.00				24 to 1 serializer
EP3C16FC484-6	1					11.34	21.98	42.99	FPGA
FAN2558S12X	1			43.14					low-dropout (1.7V) 1.2V regulator
LM1117MPX-2.5	2	86.67							low-dropout (1.2V) 2.5V regulator
LM1117MPX-3.3	2	141.35							low-dropout (1.2V) 3.3V regulator
LTC1662	1		0.01						dual 10bits serial input DAQ
MAX6575L	2			0.15					temperature sensor
MAX6575L	2				0.15				temperature sensor
IQD CFPS-32IB 40MHz	1					18.00			DEBUG local oscillator
UM245R	1				0.00				DEBUG usb interface
TOTAL		**456.0**	**20.8**	**171.0**	**101.7**	**141.3**	**22.0**	**43.0**	**mA**
2378		914	104	564	335	353	55	52	mW

Table 56*: ladder card typical power requirement (debug operation without hybrid, without RDO)* [5a][6][7][8a][9][10][11][12][13][14][15][16][17]

numbers in red are only guesses to match measured current on +5V power supply.

Analog voltage assumed to be 5V (as worst case) for power calculation: In old SSD, one had to adjust -2V around -2.2V and to adjust +2V around +2.5V to get -2V and +2V on all the hybrids. This was due to voltage loss along the flex cables on the ladder and to the sense cable being connected to the electronics at the end of the ladder.

5.3 Power connector

Figure 24*: Nicomatic power connector cabling*

Colors in Figure do not use general typographic convention defined in §2.1 of this document: Green is Analog Ground, Blue is Digital Ground (=-2V)

To protect the thin sense cables in case of a short circuit, all sense lines (+, - and ref) have a 0603L010 polyfuse[18] in series.

Cables have copper-clad aluminum wires[19]. AWG26 for sense and bias and AWG22 for low voltage power.

According to Table 54, Table 55 and Table 89, currents for one ladder end (each Nicomatic connector) are:

	-2V power supply	*+2V power supply*	*+5V power supply*
typical	870 mA	2172 mA	909 mA
maximum	883 mA	2186 mA	1357 mA

Table 57*: ladder-end current requirement for low voltage power supplies*

Bias current for one ladder (one Nicomatic connector per ladder) is:

	bias power supply
typical	16*5 µA
maximum	16*10 µA

Table 58*: ladder current requirement for bias power supply*

5.4 Grounding

The ground wire of the High voltage is available on the fixing hole of the lower part of the ladder card. It will be connected to the carbon-epoxy ladder only on the East side.

6.3.4 Hybrid power consumption[23][24]

currents needed (in µA) by each sub-part					
sub-part	*Qty*	*-2V*	*Agnd*	*+2V*	*usage*
Alice128 preamplifier (x128)	128	12	91	103	sampling and acquisition
Alice128 shaper (X128)	128	17	15	32	sampling and acquisition
Alice128 intermediate buffer (x4)	4	1850	0	1850	acquisition
Alice128 output buffer (x1)	1	8450	0	8450	acquisition

currents needed (in mA) by each chip					
chip	*Qty*	*-2V*	*Agnd*	*+2V*	*state*
Alice128	6	3,712	13,568	17,28	sampling
Alice128	note1	19,562	13,568	33,13	acquisition
costar	1	11	0	11	sampling and acquisition

currents needed (in mA) by each hybrid					
hybrid	*Qty*	*-2V*	*Agnd*	*+2V*	*state*
hybrid	16	33,272	81,408	114,68	sampling
hybrid	note2	49,122	81,408	130,53	acquisition

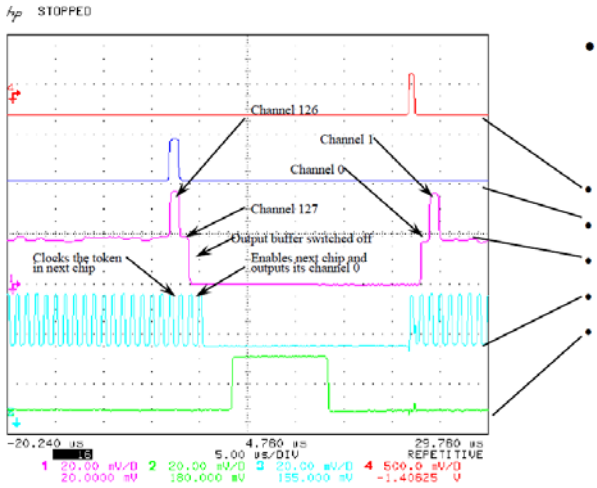
currents needed (in mA) by the hybrids on each ladder end					
SSD version	*Qty*	*-2V*	*Agnd*	*+2V*	*state*
old SSD	1	532,352	1302,528	1834,88	sampling
old SSD	note3	548,202	1302,528	1850,73	acquisition
SSD Upgrade	1	532,352	1302,528	1834,88	sampling
SSD Upgrade	1	785,952	1302,528	2088,48	acquisition

power consumed (in mW) by the hybrids on each ladder end			
SSD version	*Qty*	*power*	*state*
old SSD		4734,464	sampling
old SSD		4797,864	acquisition
SSD Upgrade		4734,464	sampling
SSD Upgrade		5748,864	acquisition

note1: For one hybrid, only one Alice128 chip should be in acquisition state
note2: (1 acquisition + 15 sampling) in old SSD and (16 acquisition) in Upgraded SSD
note3: in the old SSD, after an abort, there could be more than one hybrid in acquisition state (token out of the first hybrid but not out of the ladder)

Table 89: ***currents needed by the Front-End Electronics (FEE)*** [23][24]

6.3.5 Alice128C[4][4a] timing



- Full read out sequence
- TOKENIN in the first chip
- TOKENOUT
- Analog out
- Read clock
- Test request

Figure 51: ***Alice128C timing***[4a]

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