ULTIMATE

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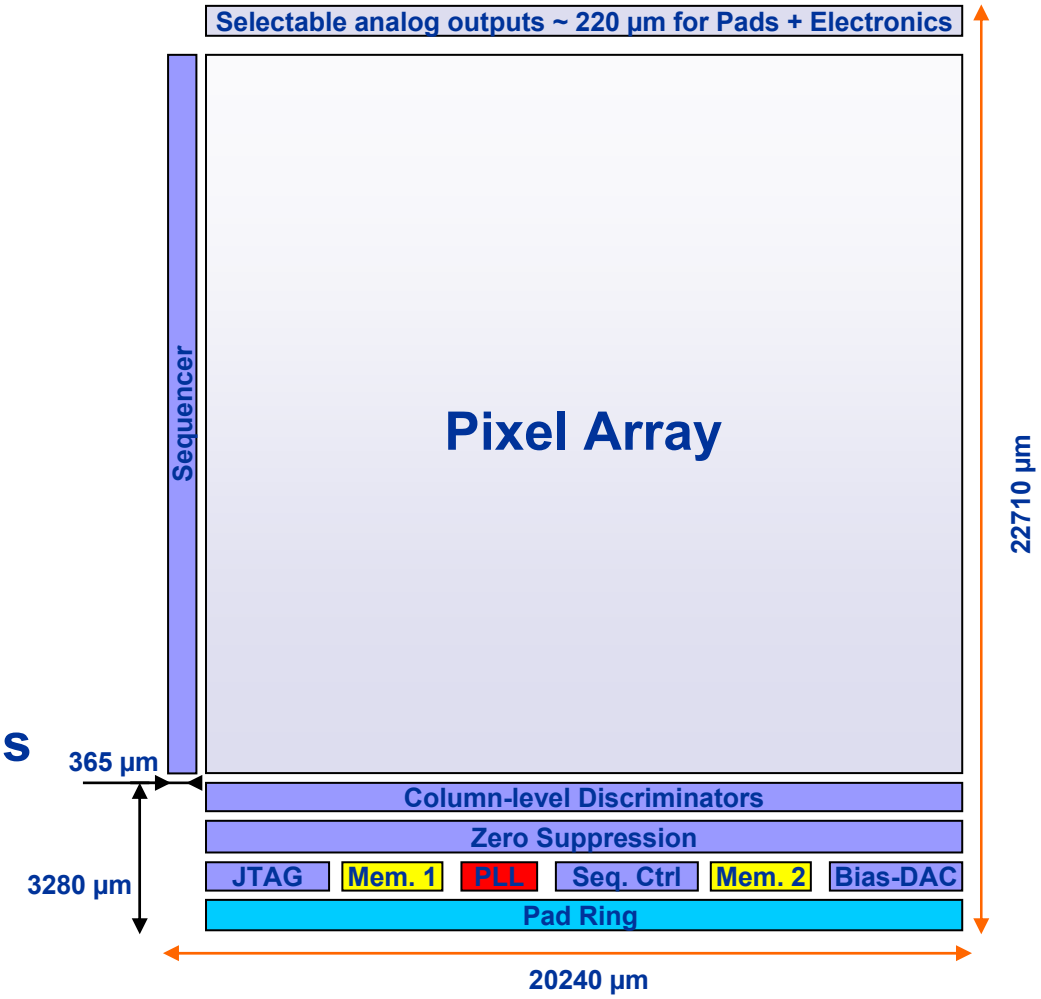
ULTIMATE chip design

- Design based on Mimosa26 architecture
  - Reticle size (~ 4 cm²)
    - 890 10^3 pixels
  - Reduced power dissipation
    - Vdd: 3V
    - Optimized pixel pitch v.s. Non ionising radiation tolerance
      - Estimated power consumption ~134 mW/cm²
    - Shorter integration time
      - Integration time = 185.6 µs
  - Improved pixel architecture
  - Optimized discriminator timing diagram
    - Reduced threshold non uniformity
  - Alleviated analogue to digital coupling
  - Higher hit density ➔ larger memories
    - 3.5 times larger than Mimosa26
  - Enhanced testability
  - Enhanced radiation tolerance
    - High res epitaxial layer process (400 Ω cm²)

ULTIMATE floor plan

- **Pixel Array:**
  - 928 rows x 960 columns
- **Pitch: 20.7 µm**
- **Active area: ~ 3.8 cm²**
  - X = 19872 µm
  - Y = 19209.6 µm
- **Chip size: ~ 4.6 cm²**
  - X = 20240 µm
  - Y = 22710 µm
- **AMS 0.35 high-res process**
  - 400 Ω.cm p^- EPI layer



Mimosa26HR, batch 2010

- *Preliminary results*
  - Standard EPI layer: 14 µm, 10 Ω.cm
  - 10 µm, 15 µm and 20 µm 400 Ω.cm EPI Layer
- Before irradiation

Analog calibration with X ^{55}Fe source, F=20 MHz, T=20°C, VDDA =3 V
* Calibration with beta ^{106}Ru source

EPI Layer	Noise (e-)	Cal.Peak (ADC u.)	Seed Pixel (%)	Cluster 3x3 (%)	S/N*
Standard	11.8	358	21	73	21
10 µm	11.7	363	36	96	35
15 µm	11.8	375	32	92	41
20 µm	11.8	376	22	77	36

- After non-ionizing irradiation at 6 10^{12} n_{eq}/cm^2

Analog calibration, F=20 MHz, T=15°C, VDDA =3.3 V
* Calibration with beta ^{106}Ru source

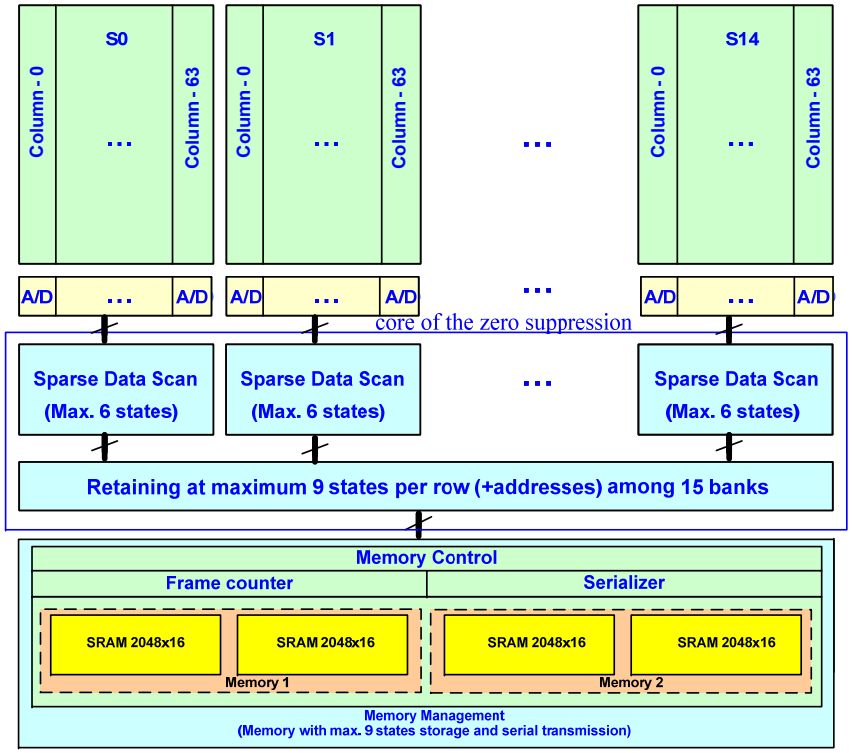
EPI Layer	Noise (e-)	Cal.Peak (ADC u.)	Seed Pixel (%)	Cluster 3x3 (%)	S/N*
Standard	12.6	387	15	47	10.7
10 µm	13.8	381	34	87	22
15 µm	15.7	385	30	85	28

Mimosa22HR

- Chip submitted in April 2010
- Improve the non-ionizing radiation tolerance
- Optimized pixel pitch
  - Pitch = 18.4 µm and 20.7 µm
- Improved pixel architecture
  - Higher depletion voltage (SNR, rad. tol.): 0.7 V ➔ 2 V
  - Cascode amplifier
- Improved pixel clamping voltage regulator
  - Vclp can be provided by the internal DAC
- This run includes also latch-up free memories design

SuZe

- **SuZe condition:**
  - ~ 600 hits/sensor/frame
    - Assumptions for LowRes EPI:
      - Isolate hits
      - 1 hit = 3x3 pixels
  - Noisy pixels: ~ 100 (10^{-4})
- **Read-out row by row**
- **Zero suppression algorithm**
  - Find max. 6 strings per group
    - 15 Groups of 64 columns
  - Find max. 9 strings per row
    - String (or state): up to 4 contiguous pixel signals above threshold
- **Memories store hits**
  - 2 memories of 2048x32 bits
  - Read/write ping-pong
- **Serial transmission**
  - Output freq. = 160 MHz

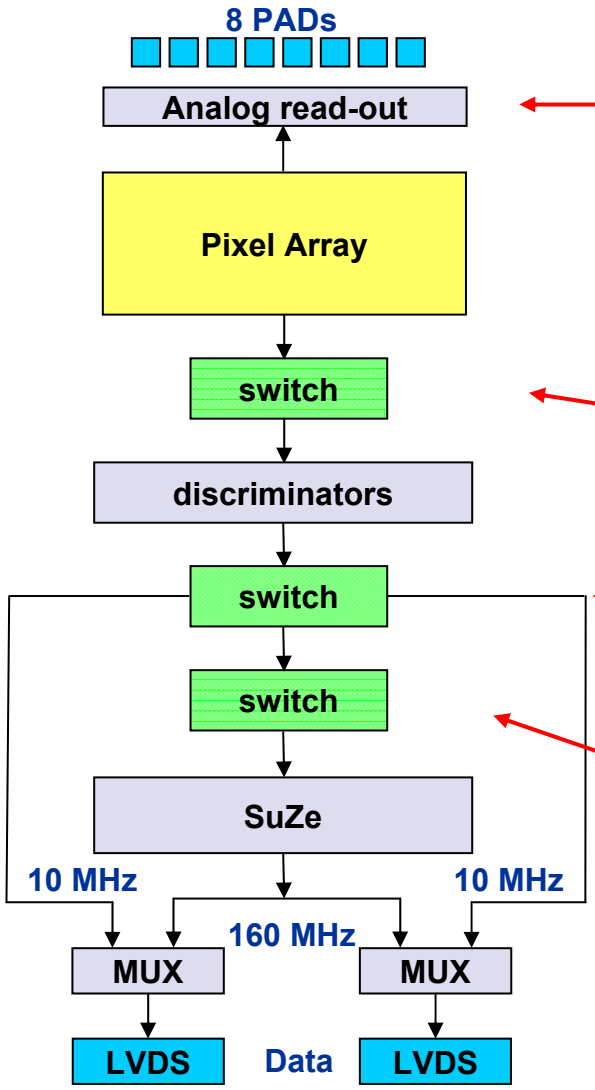


Block diagram of the sensor read-out architecture

Frequency distribution

- **Input:**
  - **Clk: 160 MHz**
    (Input LVDS @ 160 MHz or using the internal PLL @ 10 MHz)
- **Inside chip:**
  - **Pixels and discris: 5 MHz (200 ns ➔ 16 x 80 MHz)**
- **Output:**
  - **2 LVDS data out: 160 MHz**
  - **Markers (LVDS): 1 MkD (per frame) and 1 ClkD (160 MHz)**
    - MkD and ClkD LVDS drivers may be disable by JTAG
      - Only 1 MkD and 1 ClkD by ladder

Testing functionality



Mode 1: Analog Pixel Scan : The matrix is divided in stripes of 8 columns and fully scanned at each frame, then swapped with the next block of 8 columns at right and so on until all the columns are analyzed. 8 output pads. Max. Freq. = 20 MHz

Mode 2: Nominal speed: 8 pre-selected columns connected directly to the 8 output pads and read at 80 MHz

A test mode injects 2 Test Voltages to emulate pixels outputs

1- A test mode read one selected Row Register ; pixels and discris are in normal mode, t_{int} = 185 µs, Read-out freq. = 10 MHz via 2 LVDS output pads

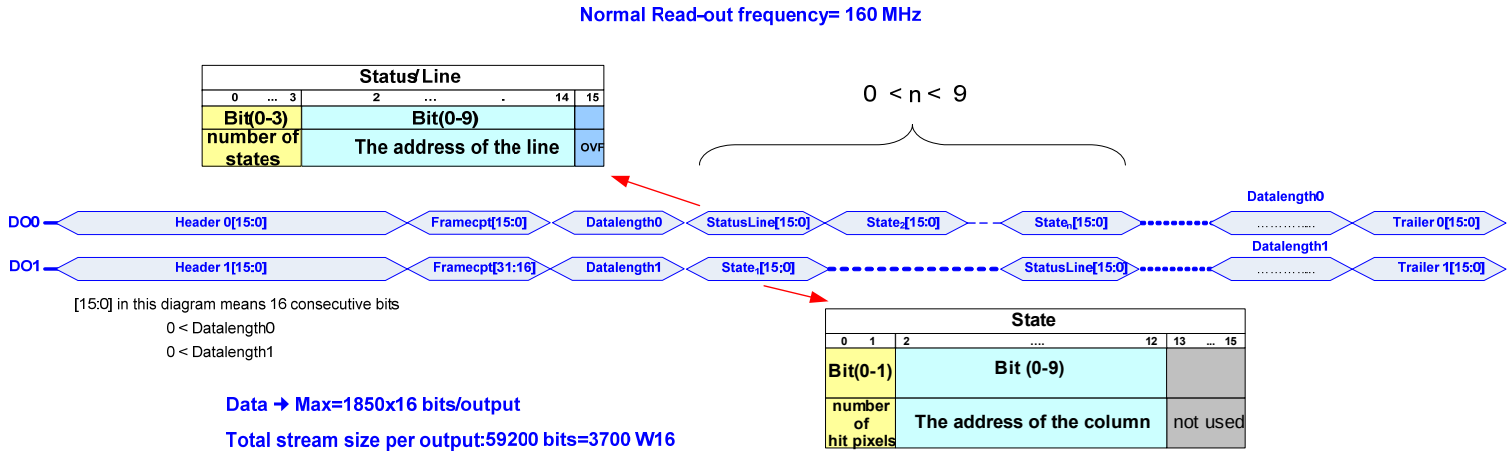
2- The row automatic scanning mode of whole matrix is implemented

1- A test mode injects 2 SuZeTest Rows to emulate the matrix. In SuZe, 2 functionalities are tested: the Sparse Data Scan and the Multiplexing Logic which gives at maximum the 9 states.

2- An external signal synchronized with the matrix read-out allows activating a line pattern during one or several selected rows

Data format

- The data format is the same as Mimosa26 but read-out frequency is doubled
- Mode test «pixels+discris»: read 1 row register, data split to 2 outputs at 10 MHz
- Mode «normal»: data split to 2 outputs at 160 MHz with LSB first



For each line with hit : one Status/line followed by up to 9 States. The following data stream is generated:

- **Status/Line word: Address of line, Number of States (9 Max., overflow flag if > 9)**
- **States list – One state = consecutive pixels at 1 in the line:**

  Column address of the first pixel at 1, Number of pixels at 1

Power dissipation

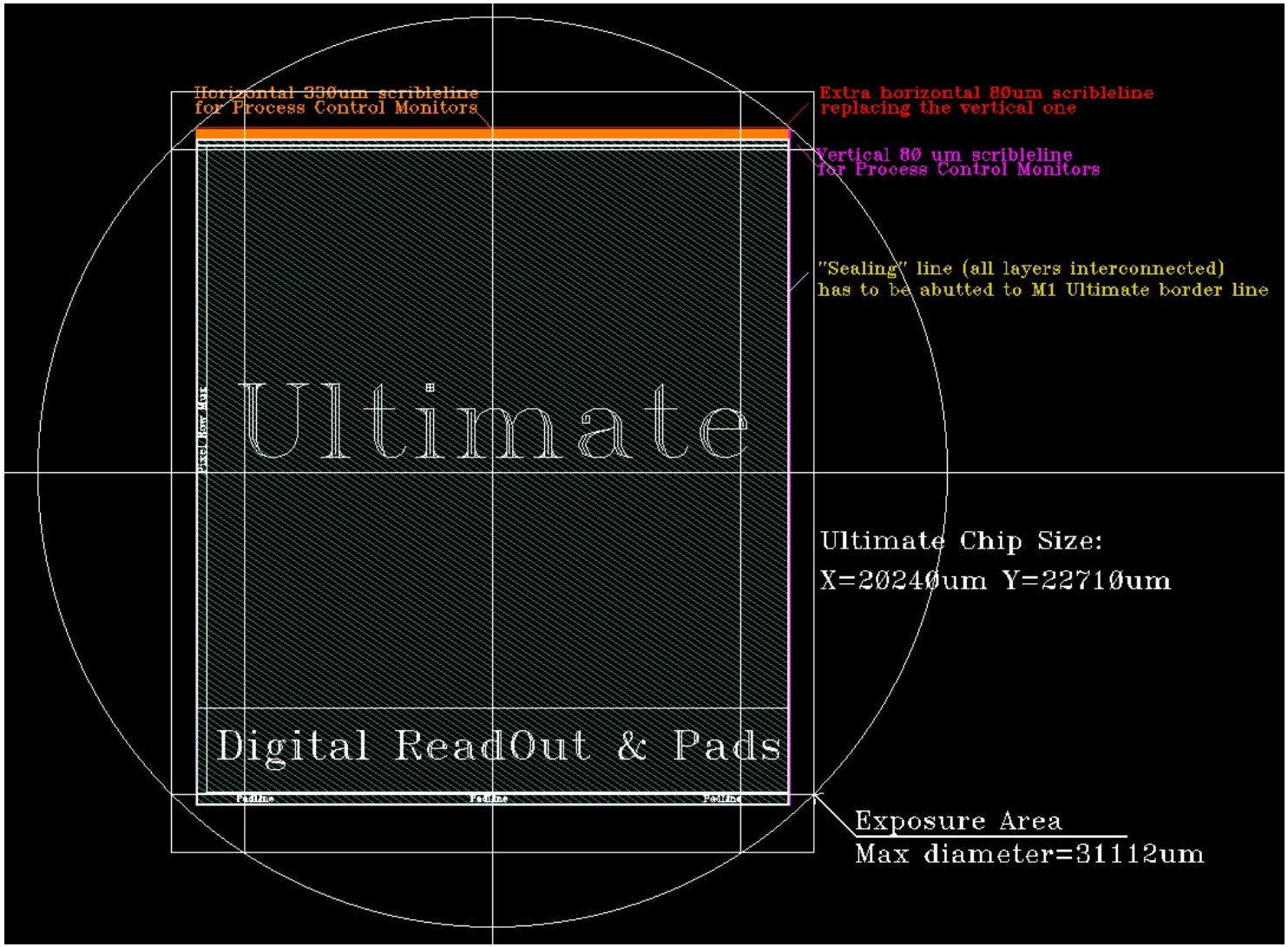
- **Estimated power consumption: 134 mW/cm^2**

Pixel pitch (µm)	Pixels (mW)	Discris (mW)	Buffer Ref. (mW)	DAC (mW)	Digital (mW)	LVDS (mW)	Total (mW)	Power (mW/cm^2)
20.7 (960 col.)	170	200	50	20	140	40*	620	134
18.4 (1088 col.)	200	250	50	20	150	40*	710	154

Conditions:
VDDA = 3 V
VDDD = 3 V
*** LVDS driver: reduced differential signal at +/- 200 mV**
Chip area: 4.6 cm^2

- **Continually optimisation of power consumption**
  - **Digital part**
  - **Ref. buffers, DAC**
  - **…**

Butting


Horizontal 330um scribleline
for Process Control Monitors
Extra horizontal 80um scribleline
replacing the vertical one
Vertical 80 um scribleline
for Process Control Monitors
"Sealing" line (all layers interconnected)
has to be abutted to M1 Ultimate border line
Ultimate
Ultimate Chip Size:
X=20240um Y=22710um
Digital ReadOut & Pads
Padline
Padline
Padline
Exposure Area
Max diameter=31112um

ULTIMATE planning