LG May 5, 2008 DRAFT

Production testing for the HFT Pixel Ultimate Sensor

The Ultimate sensor is being designed at IPHC to be the primary sensor for use at STAR in the Pixel vertex detector. The Ultimate sensor characteristics include the following; 18.4 micron square pixels, on chip CDS, column level discriminators, and a on-chip zero suppression system called SUZE. The sensor has a 200 us integration time and two outputs for digital address data. There is an analog output mode but it can not (we believe) be run in parallel with the normal data taking mode. These are full reticule size sensors. A functional schematic of the sensor is shown below

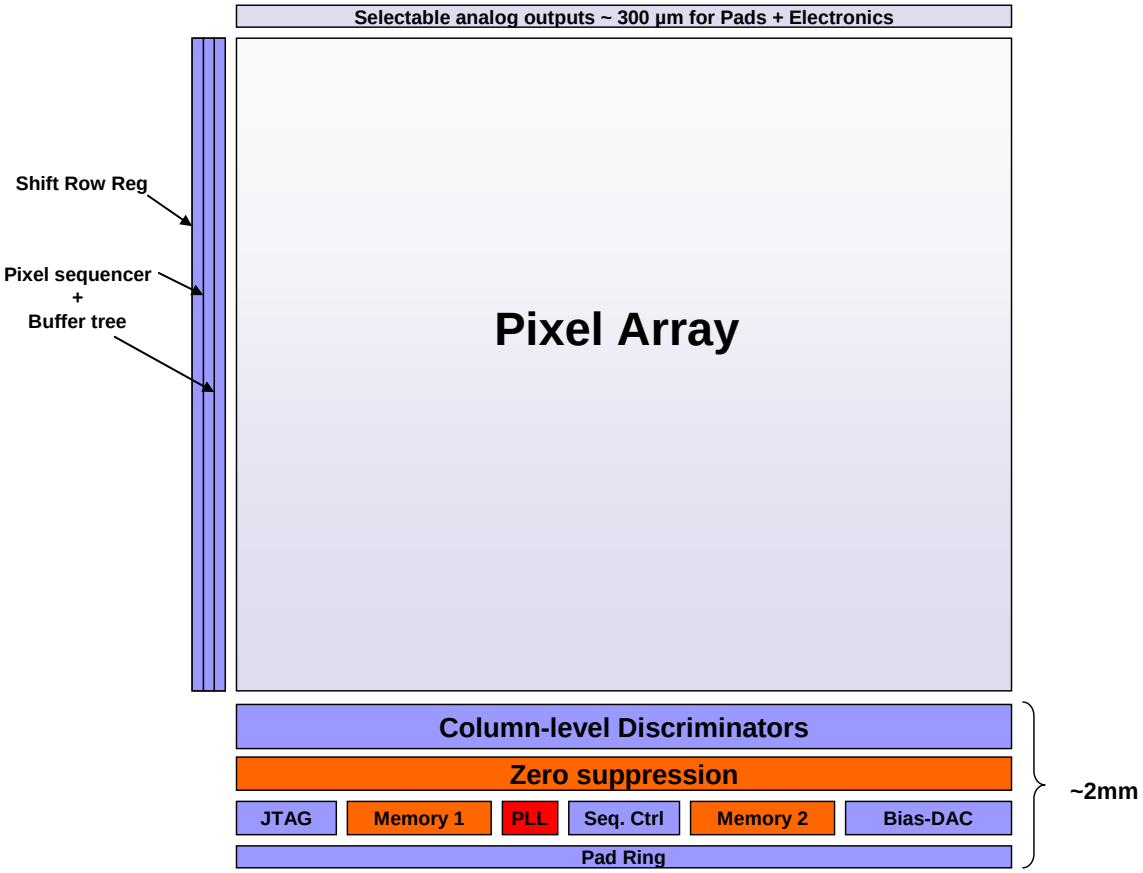

Figure 1 - Ultimate sensor functional blocks

The SUZE system allows for on sensor zero suppression and the reduction of the number and speed of the outputs, but complicates the testing that is required since only a small percentage of pixels can be sampled before the overflow point of SUZE is reached. A more detailed diagram of the SUZE function is shown below.

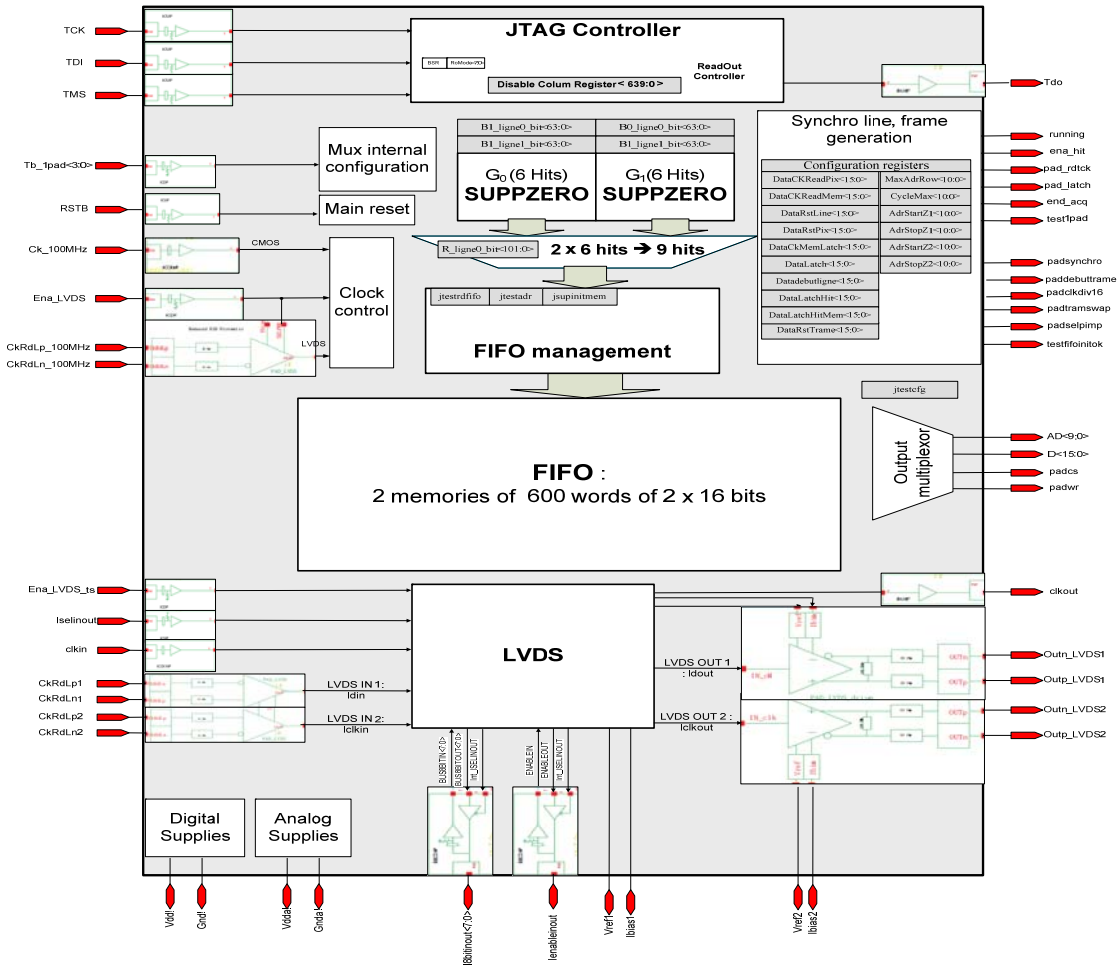

Figure 2 - SUZE architecture. Note that overflow can be initiated by >9 hits/line or by > 600 words of 2 x 16 bits in the total event hit memory in this configuration.

The design shown appears to be a ping pong arrangement where one FIFO is being filled while the other one is read out on a frame by frame basis. One can see that the SUZE architecture as it is currently designed can reach overflow in two ways. If any row exceeds 9 hits, overflow for that row is reached. Furthermore, in order to save space in the silicon (it is assumed) there is an additional limitation in the number of hits that can be stored in the hit format in the event FIFO. That limit as given at IPHC in April 2008 is encoded 500 hits for the current design but may rise to over 1000 hits for future designs. This feature significantly complicates testing since the desire for production testing is to provide a stimulus at the sensor pixel (such as an LED flash) and to check that the signal is handled correctly in the sensor through the whole readout chain. This must be done for every pixel in the sensor with some quality cuts to be sure that we are attaching usable sensors to ladders. To achieve this goal, LBNL will need to request additional functionality in the form of a special testing mode from IHPC.

Special Testing Mode(s)

In order to test all pixels and not to run into SUZE overflow we will need to test the sensor in blocks of clusters that do not generate a SUZE overflow condition. In order to

accomplish this we will need to integrate a column and row mask into the Ultimate sensor design. For the sake of discussion, if we take a 500 hit event FIFO limitation and a ~ 1M pixel sensor, we must take at ~ 2K frames with different mask settings for each frame in order to read out each pixel. If we are to do this with different threshold settings as well, the JTAG setting accesses become the time limiting factor. This drives the need for a more automated testing mode rather than a simple JTAG accessed set of column and row masks.

We would like to propose a special test sequence mode that can be initiated via JTAG settings and a START token that will automatically use the column and row masks to generate a window of active pixels that will encode to less than the SUZE limit. There are many possible implementations that can accomplish this task. A simple one that has limited functionality is described below.

The special test mode would generate an active window of 500 pixels by appropriate masking of row and column. This window would automatically move to the location of the next block of untested pixels in the next frame readout in a pattern that covers the active area of 1024 x 1088 pixels. Readout would continue in this way until this testing mode is ended. A diagram of the proposed function of the special test mode is shown below.

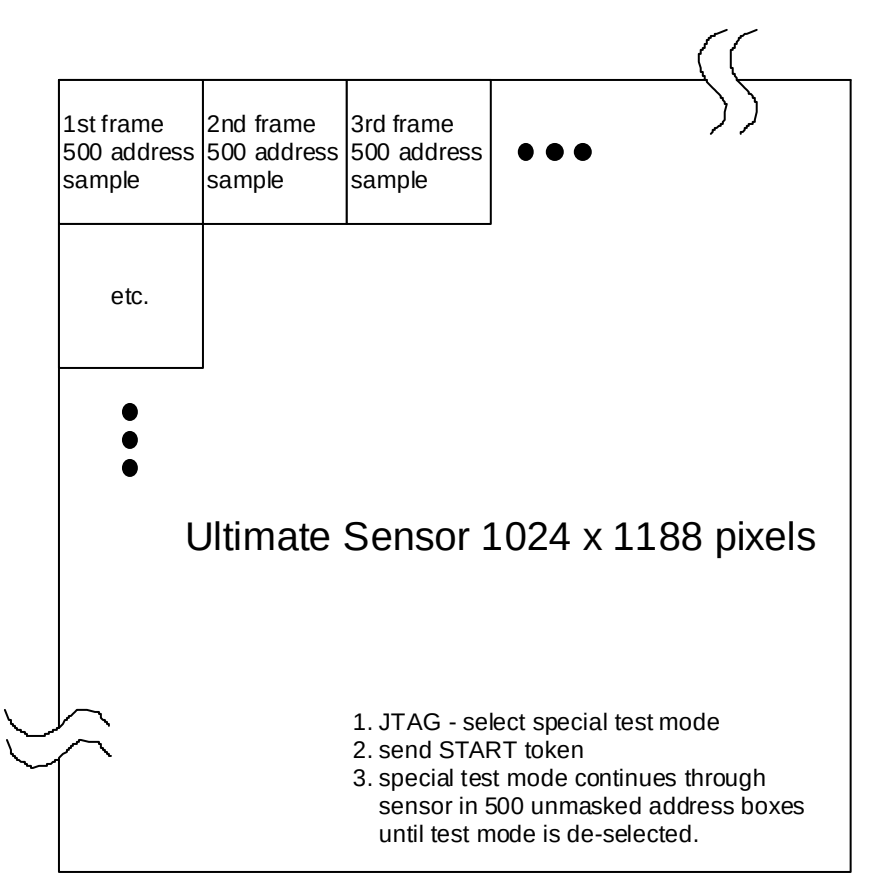

Figure 3 – The masking of rows and columns on adjacent frame readouts to give a window of active pixel addresses that would be tested through the SUZE system in each frame in a simple example.

Other slightly more complex testing modes can be envisioned that would allow for enhanced capabilities while preserving the basic requirements of an automated mode that allows for automatic testing of all pixels.

Testing Plan

We envision two modes of testing for this sensor. Design validation and performance evaluation is the first mode. Production testing after design criteria have been met is the second mode.

Mode 1 –
Purpose:
Design validation and performance evaluation. We expect that such parameters as contribute to the overall sensor signal/noise and all sensor functional parameters to be tested. These tests will most likely be performed on individual sensors mounted to full function testing boards. In this case, the testing input and output points that would allow for the testing and analysis of the separate functional parts of the sensors should be defined and integrated by the chip designer. The internal sensor interfaces that allow for the measure of sensor performance characteristics should similarly be defined by the chip designer since the designer alone knows the parts of the internal design and communications in the sensor that have the greatest contribution to the performance and the points that will aid the most in any troubleshooting that may be needed.

Required sensor capabilities:

1. TBD
2.

Mode 2 –
Purpose:
To perform production testing on the Ultimate sensors and verify the digital function of sensors and the aliveness and response of all channels of each sensor through the whole readout path.

Required sensor capabilities:

1. Programmable output pattern test mode (at least 64 bits) that can be set to repeat.
2. Column and row disable mask sequence for testing that can be initiated as a special testing mode. This testing mode would segment the sensor such that SUZE did not go into overflow. This is described above.

Testing Plan –
The requirement for the programmable output mode is to allow us to calibrate the latencies and timing to allow for data transfer between the sensor and the RDO system at the high system readout frequencies. The requirement for the special testing mode is to allow us to test the whole sensor response through the SUZE without running into the overflow limit. We intend to have two large scale sensor testing points during the assembly of the Pixel detector. We will first probe test these sensors after dicing and

thinning to 50 um. We will then perform the gluing, wire binding and other assembly steps leading to testing of the finished ladders. During these tests we will follow the testing plan shown in preliminary form at http://rnc.lbl.gov/hft/hardware/docs/Phase1/m22_phase1_ultimate_sensor_testing.pdf.