

Appendix ??: Integration of the SSD into the HFT

Version 1.0

Introduction

The STAR Silicon Strip Detector¹ (SSD) constitutes the fourth layer of the HFT. It is installed between last layer of the IST and the TPC, the SSD will enhance the tracking capabilities of the STAR experiment by measuring accurately the two dimensional hit position and energy loss of charged particles. It aims specifically at improving the extrapolation of TPC tracks to the IST. As a result, the tracking efficiency is significantly improved. The SSD resides at a distance of 230 mm from the beam axis and covers a pseudorapidity range of $|\eta| < 1.2$. It has a total silicon surface of about 1 m².

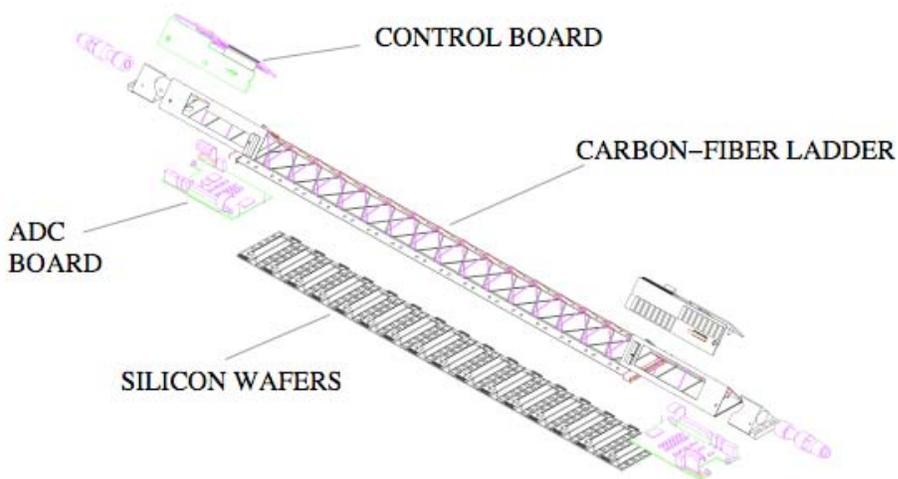


Figure 1. An SSD ladder showing separately its components.

The design of the SSD has two clamshells. Each clamshell supports 10 carbon fiber ladders. Each of these ladders, see [Figure 1](#), supports 16 wafers using double-sided silicon strip technology (768 strips per side). These wafers are connected to the front-end electronics (6 ALICE 128C chips per side) by means of the Tape Automated Bonded (TAB) technology². The ladders are tilted with respect to their long axis, allowing the overlap of the detectors in the transverse plane for better hermiticity and alignment. A bus cable transports the analog signals along the ladder to a 10-bit ADC board, which is installed at each end. After digitization, the signals are sent to Readout Boards, which are linked to the DAQ system through Giga-link optics fibers.

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The whole system is remotely controlled to monitor powers and temperature and also to calibrate and tune the front-end electronics. The cooling system uses airflow through the ladder, which is enclosed in a Mylar sheet. The total radiation length of each ladder is approximately 1%.

Current Readout

The current readout chain can be viewed in [Figure 2](#). There, 10 ADC boards are daisy chained to one readout board. As each of the 20 ladders has two ADCs, then a total of four RDO boards can digitize the full detector.

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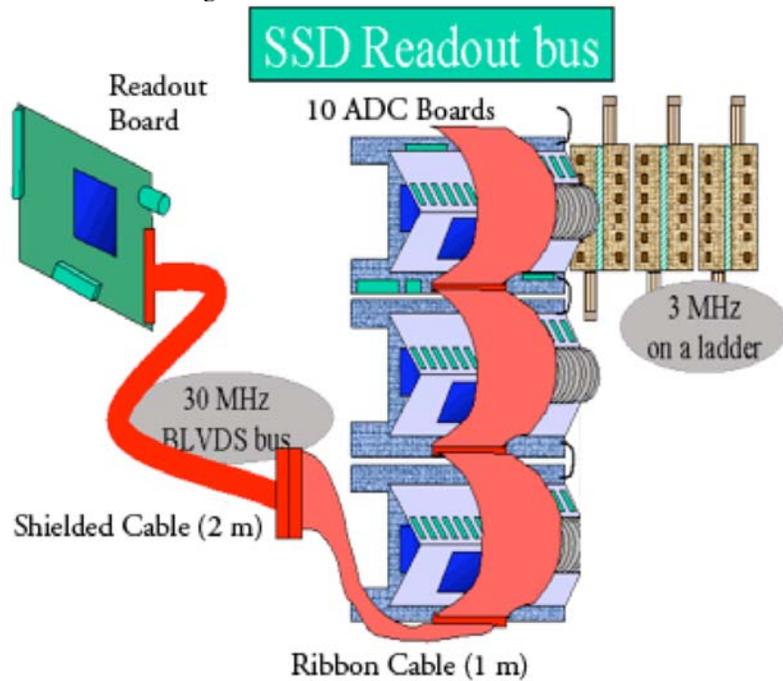


Figure 2. Module layout of the electronics.

The current FEE runs at 3 MHz. As there are 768 strips/wafer and 16 wafers/ADC Board, then it takes 4.1 ms to read out a ladder into the ADC Board. Each RDO, which runs at 30 MHz controls 10 ADC boards. Therefore, it takes a similar time, 4.1 ms, to read out each RDO. Due to a quick fix to match the TPC format, there is an extra 3 ms needed to readout extra 0s. Nevertheless, that SSD readout time is less than the TPC, so no special effort has been made to eliminate this superfluous data. When needed, this extra data transfer can be eliminated.

Future Readout

The existing ADC, which is Analog Devices' model AD 9200,³ can operate at 10 MSPS as its maximum speed is 20 MSPS. However, the fundamental limitation to increasing

the readout speed to match DAQ1000 is the custom made Alice128 ASIC.⁴ This device has a maximum speed of 10 MHz. In principle, the ladder should work at 10 MHz. Nevertheless, this maximum speed must be demonstrated in full ladder test.

When the SSD operated at 10 MHz, it would readout out all of the strips in 1.23 ms. This speed is the fastest that a ladder's worth of data can be digitized using the current ladder. If this were done, then 3 ladder sides could be daisy chained together and connected to one RDO board. The total time to read out each board would then be a similar 1.23 ms. To implement this change, we would need to have a total of 14 RDO boards – 10 more than we are using now. We would also need a similar number of receivers in the DAQ Room.

Cooling

The SSD is cooled by room temperature air, which greatly reduces the material budget. Air-cooling has been shown that it can keep the SSD as a proper operating temperature. However, experience has shown that with the existing SVT, there is a tangle of cables. When the pole tip of the STAR magnet is closed, it is very difficult to maintain an adequate supply of air. Therefore, when the Pixel detector, IST and SSD are integrated in one structure, great care will be taken to provide adequate cooling that can be maintained when STAR is operating.

¹ L. Arnold et al., *The STAR Silicon Strip Detector (SSD)*, Nucl. Instrum. Meth. A 499, 652 (2003).

² S. Bouvier, *TAB: a packaging technology used for silicon strip detector to front end electronics interconnection*, Proceedings of the workshop on electronics for LHC experiments, Rome, Sept. 1998.

³ <http://www.analog.com/en/prod/0..AD9200.00.html>

⁴ L. Hebrand et al., *Design and test of a CMOS low-power mixed-analog/digital ASIC for radiation detector readout front ends*, ASIC Conference 1998. Proceedings of the Eleventh Annual IEEE International, (1998), 89.