



Intermediate Silicon Tracker (IST)

Technical implementation,
Cost, R&D plan, Schedule

Bernd Surrow

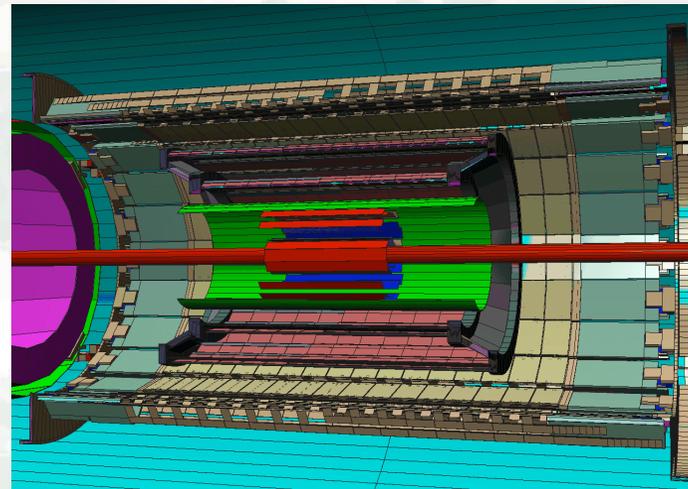


Outline

- Technical realization

- Layout

- Requirements



- R&D plan

- Cost estimate

- Schedule



IST group

□ Institution list

- Argonne National Laboratory
- Brookhaven National Laboratory
- Lawrence Berkeley National Laboratory
- Massachusetts Institute of Technology

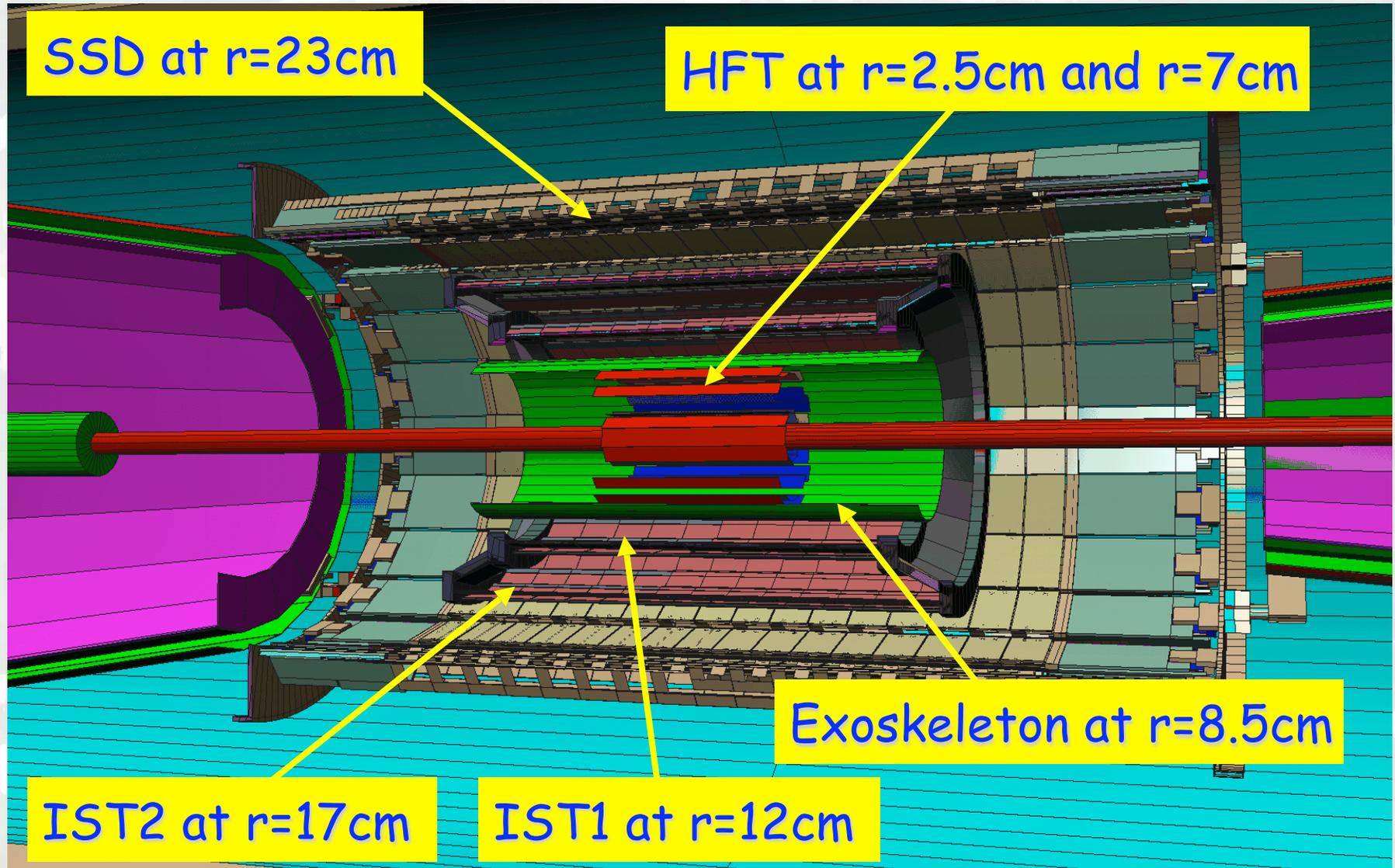


Requirements

- **Location:** Between HFT and SSD covering $-1 < \eta < +1$
- **Material budget:** $<4.5\% X_0$ and $<1.5\% X_0$ per layer, $<10\%$ ($1 < \eta < 2$)
- **Occupancy:** $<10\%$ for central Au+Au events at 200GeV CME
- **Tracking efficiency / purity:** Meet physics requirements of efficient D^0 reconstruction
($D^0 \rightarrow K+\pi$)
- **Rate capability:** Handle RHICII peak luminosities for Au+Au and p+p
- **Sampling speed:** Resolve individual beam bunches (107ns - bunch crossing time)

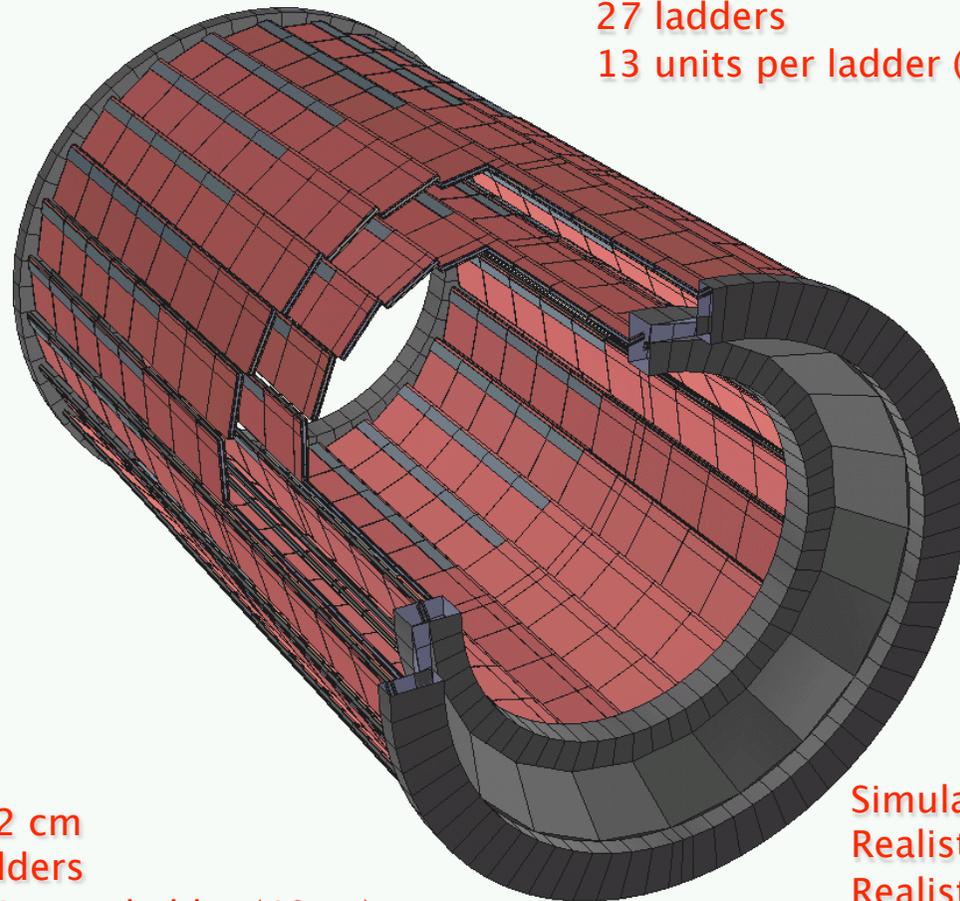


Layout





Layout



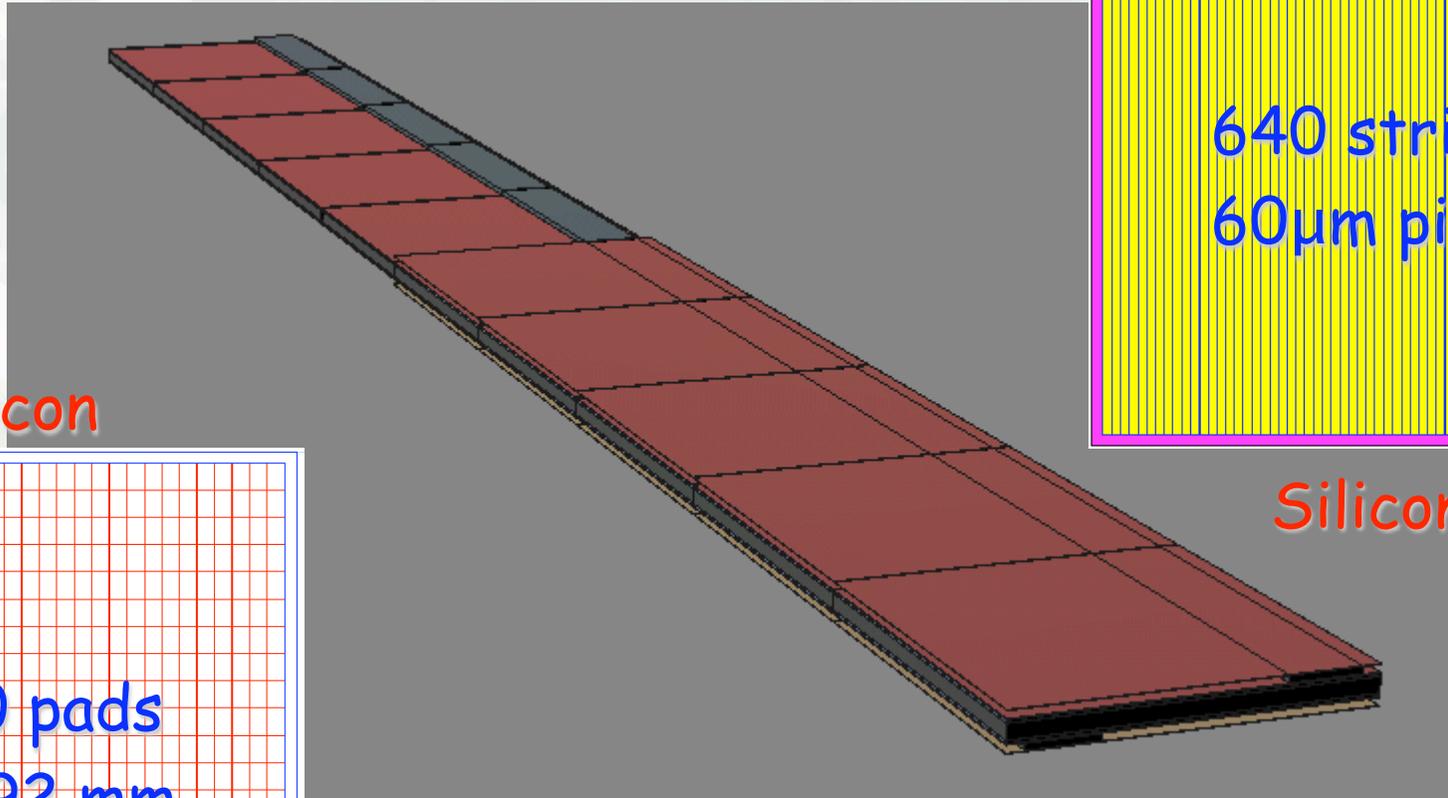
IST2
R = 17 cm
27 ladders
13 units per ladder (52cm)

IST1
R = 12 cm
19 ladders
10 units per ladder (40cm)

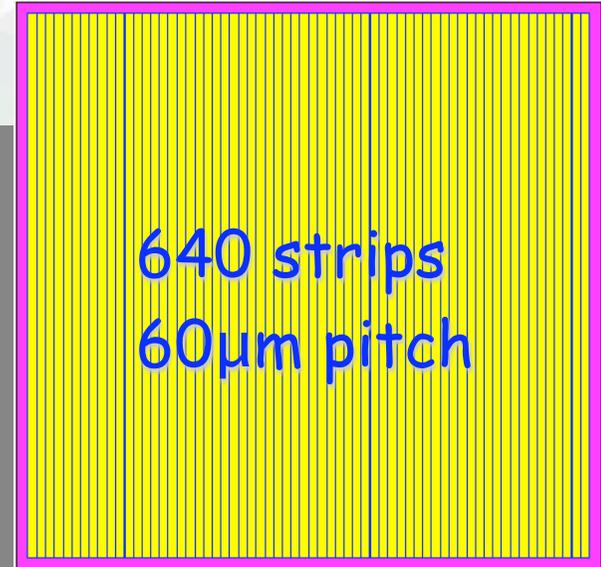
Simulations
Realistic ladders
Realistic support
Realistic cables
No utilities yet



Layout

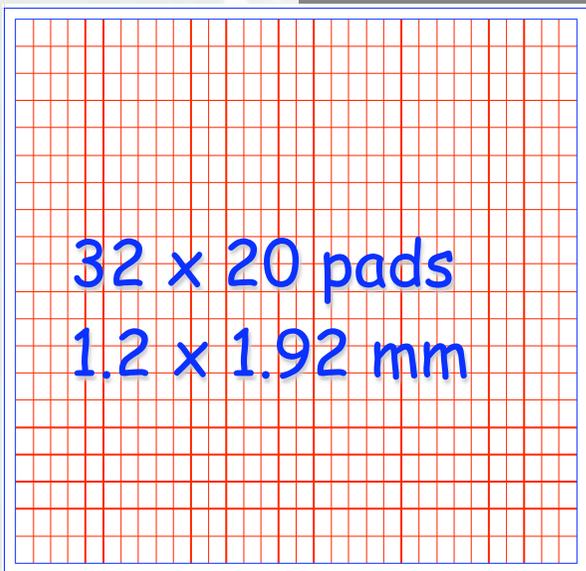


Silicon



640 strips
60 μ m pitch

Silicon Strip



32 x 20 pads
1.2 x 1.92 mm

For the readout the pad sensors are identical to the strip sensors: 640 channels



Technical realization

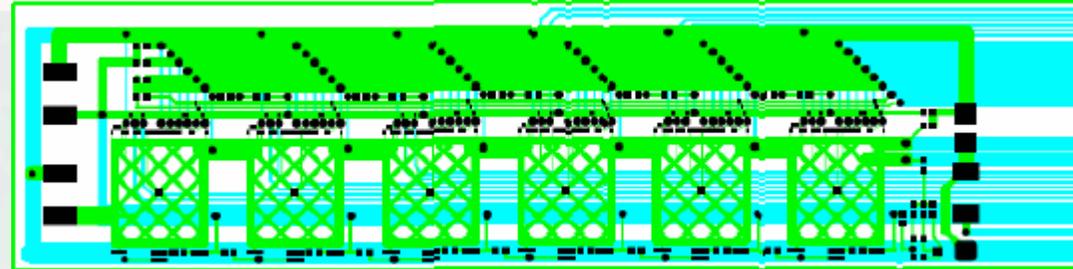
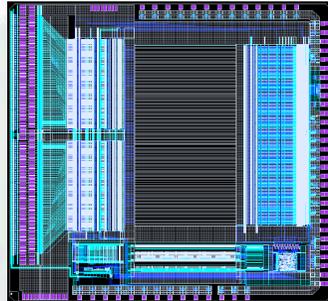
- IST technology choice
 - Conservative approach to minimize risk
 - Build upon **existing expertise**
 - Silicon sensors (Strip/Pads) from **commercial vendor (Hamamatsu)**
 - Proven to be a **reliable technology** at numerous applications
 - MIT-LNS silicon labs (Successful PHOBOS silicon system)
 - **Off-the-shelf readout chip**: APV25-S1 for CMS (Silicon) and COMPASS (GEM)
 - Basis for a cost-effective solution



Technical realization

IST module details

APV25-S1



Average X_0 :
~1.5% ($\eta \sim 0$)



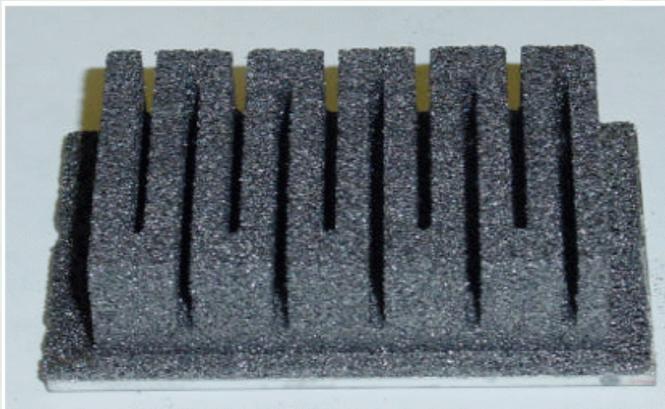
100 μ m Kapton Hybrid

Silicon Sensor

Thermal conducting carbon foam

Silicon Sensor

100 μ m Kapton Hybrid

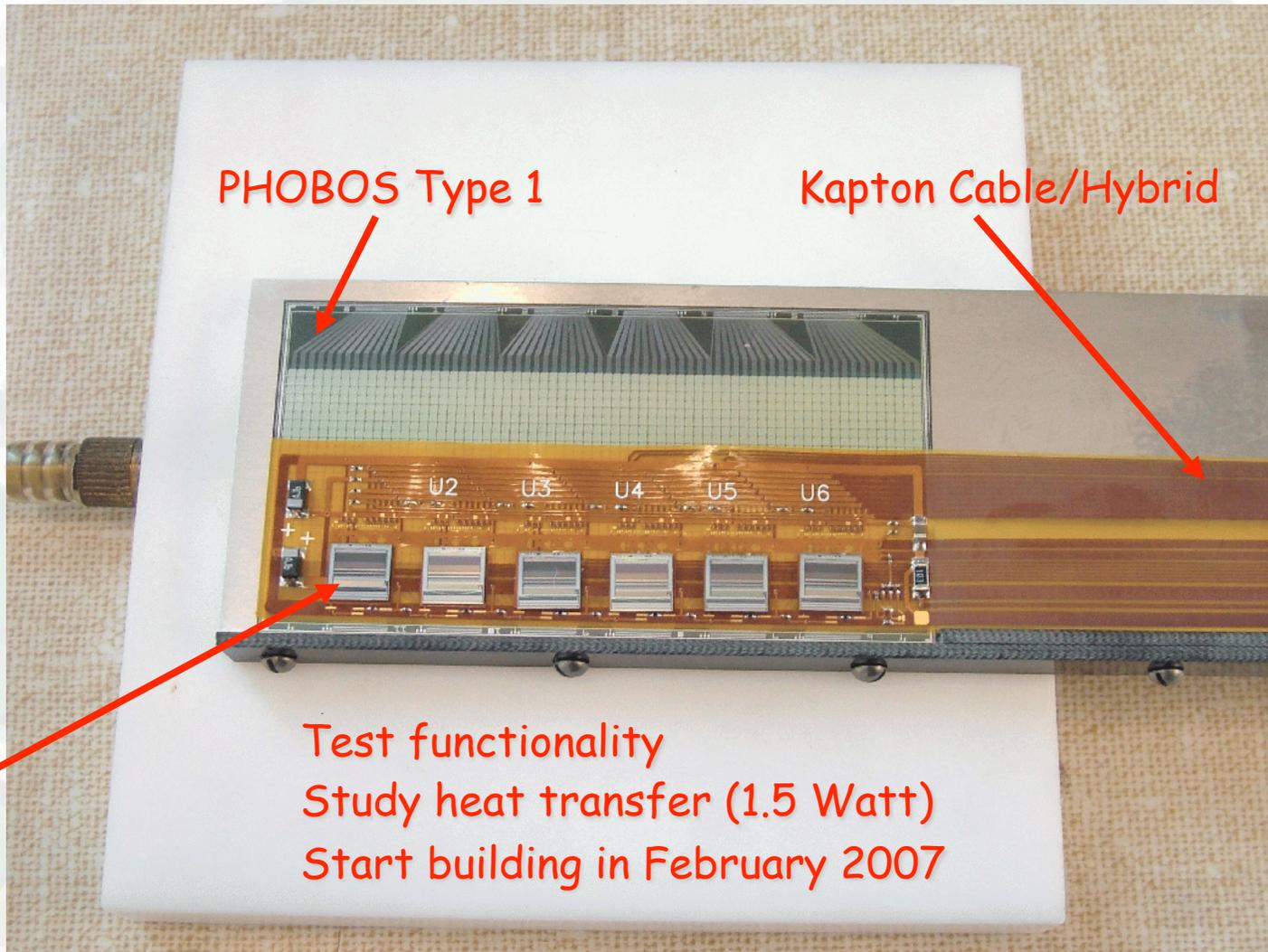


Investigating
air cooling



Technical realization

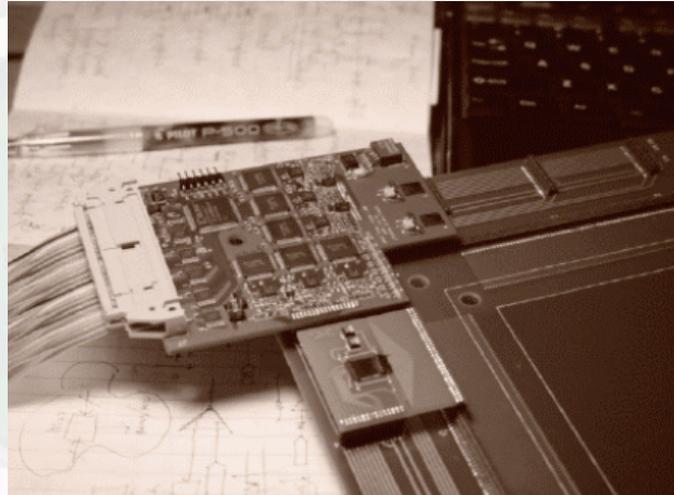
□ IST prototype



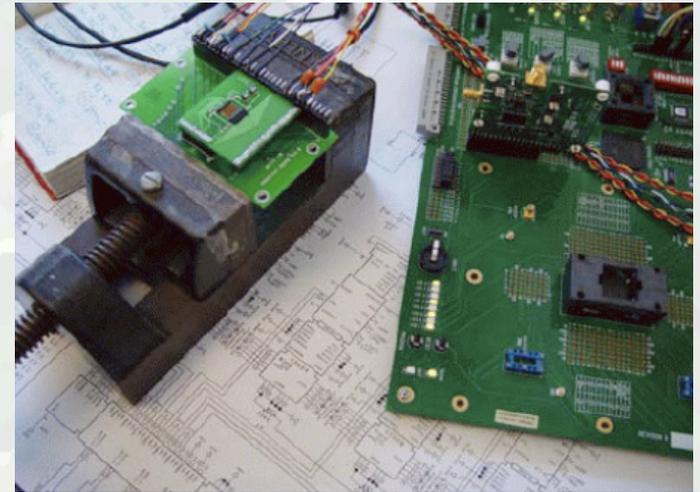


Technical realization

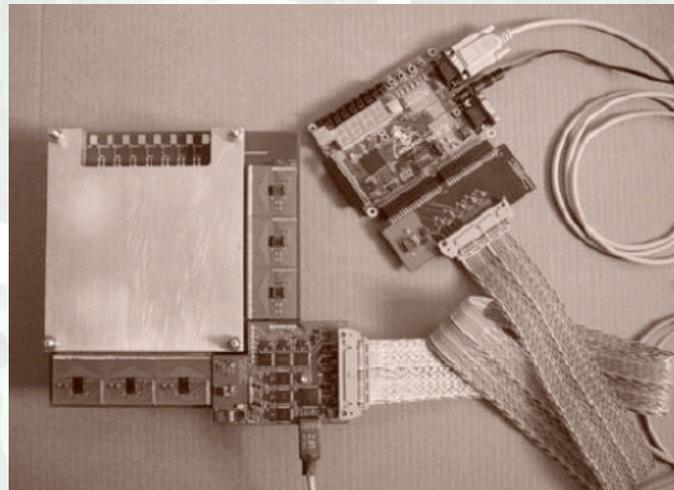
□ IST readout system



Readout Controller



APV25-S1 Module



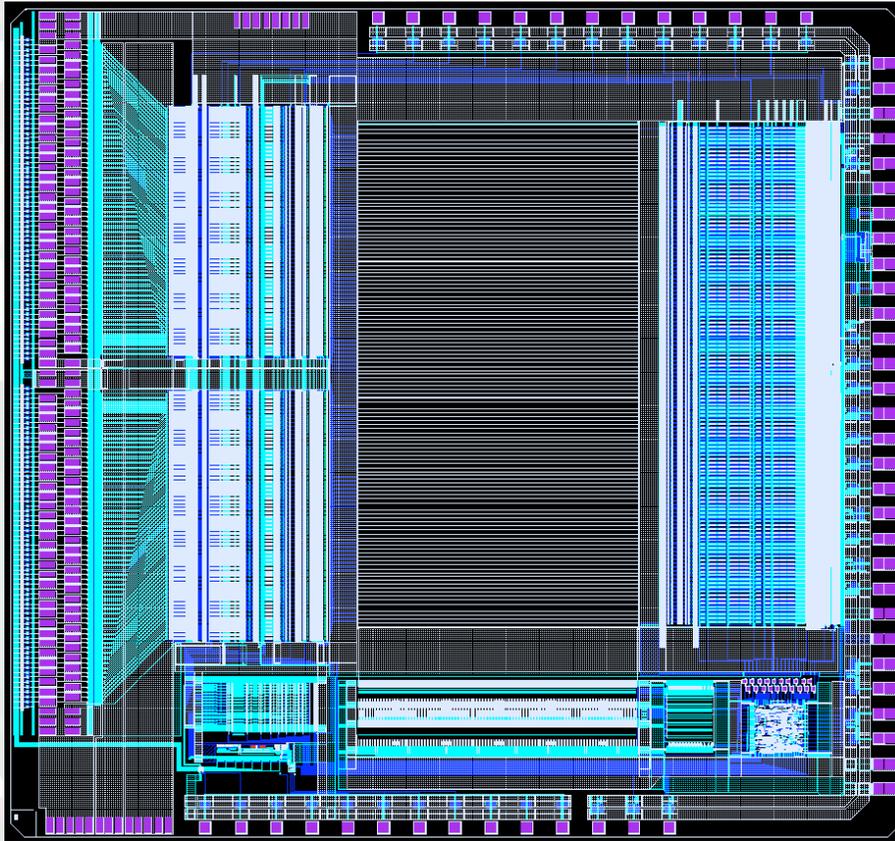
Readout Prototype

To be used in IST
and FGT (1 readout
system)!



Technical realization

□ APV25-S1 readout chip



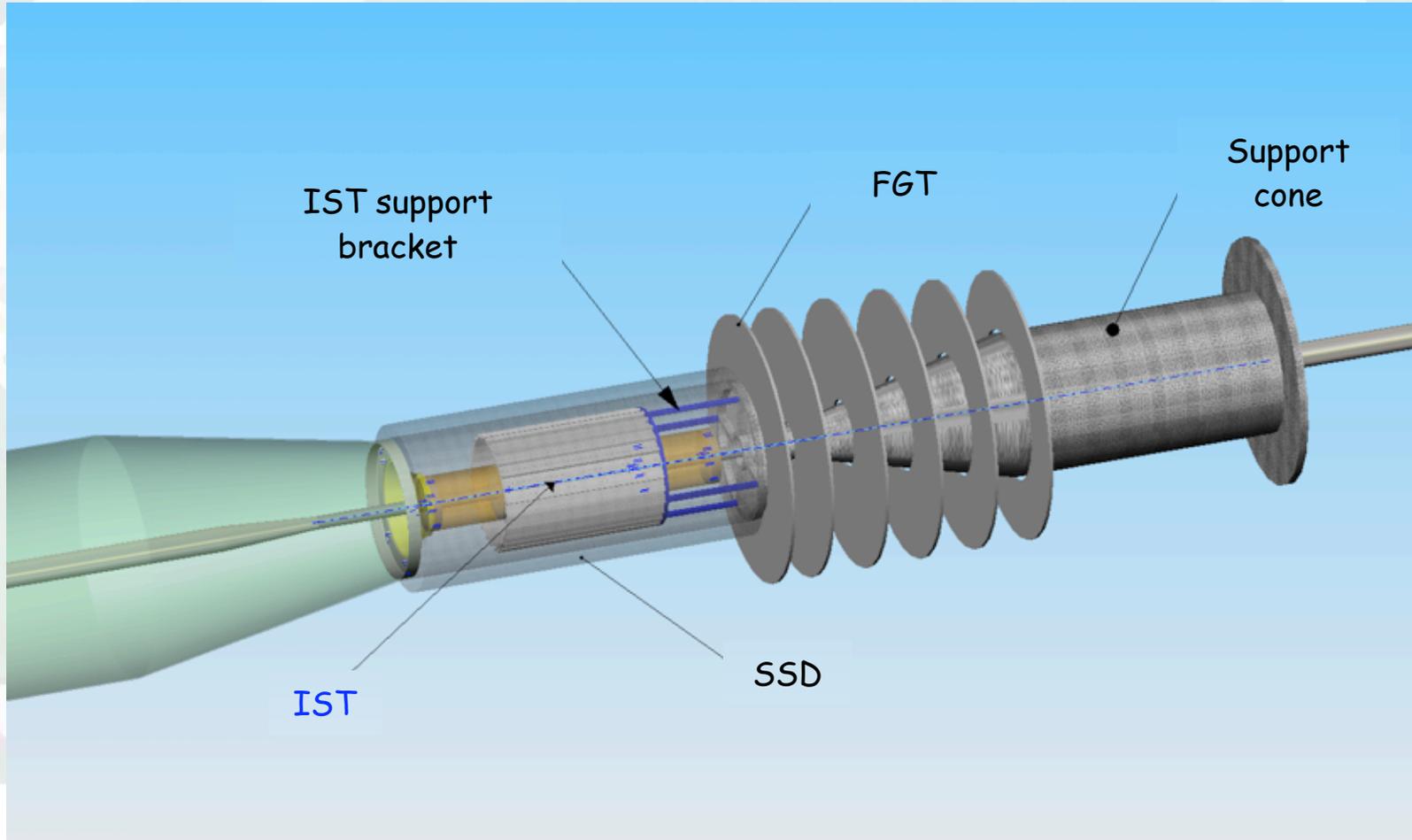
- Developed for CMS
(75000 in CMS tracker)
- 128 channels
- 40 MHz sampling rate
- 4 μ s analogue pipeline
- 11:1 Signal / Noise
- 0.25Watt/chip
- 0.25 μ m CMOS
- Radiation hard

To be used in IST and FGT (1 readout system)!



Technical realization

□ Mechanical design - Support structure





R&D plan

□ R&D items - 2007

○ The following R&D activities are foreseen in 2007

- Prototype and test of IST hybrid chip readout system
- Optimization of IST silicon strip / pad prototype sensors
- Feasibility study on the usage of light-weight carbon foam material to design IST ladders
- Feasibility study on the usage of air cooling using prototype
- Stability of carbon foam material

○ Requested funds: \$120k

- R&D engineering reserach: \$75k
- Readout components (APV25-S1 chip, cables, hybrids): \$15k
- Carbon foam material and air cooling: \$30k



R&D plan

□ R&D items - 2008

○ The following R&D activities are foreseen in 2008

- Build IST prototype ladder
- Investigate performance of IST prototype ladder inside STAR under beam conditions
- Feasibility study on a zero-suppression system

○ Requested funds: \$336k

- R&D engineering research: \$100k
- Sensor prototypes (Strip/Pads): \$68k+\$77k = \$145k
- Zero suppression system (Mercury cell system): \$66k
- Test beam prototypes: \$25k



Cost estimate

- Assumptions on cost estimate
 - Estimate is based on **baseline design**
 - The **readout system** is based on the **APV25-S1** chip which is already part of a prototype readout system (**PHOBOS expertise** at LNS on chip readout systems)
 - Current estimate relies heavily on the **PHOBOS experience** at LNS gained during the **silicon detector design and construction**



Cost estimate

□ Material

Item	IST1		IST2		Remarks
	Amount	k\$	Amount	k\$	
Strip sensors	263	167	471	297	
Pad sensors	263	736	471	1319	
APV25-S1 chips	2625	93	4713	165	
Carbon foam ladders	26	72	36	132	
Flex cable/hybrid	105	30	218	62	
Control Units	26	43	36	91	
Ribbon cables	26	4	36	6	
LV power supplies	4	39	6	59	
HV power supplies	4	19	6	29	
Subtotal layers	1203		2160		
DAQ				130	
Air cooling				98	
Mechanics				420	
Misc. items				140	
Sub total				788	
Total				4151	
Grand total				4525	

Spares:

- IST1 (19 ladders + 2 spares)
- IST2 (27 ladders + 2 spares)
- 25% spares: Sensors, readout chips, carbon foam ladders, flex cables/hybrids, control units and ribbon cables

Contingency:

- 20% on catalogue items and 40% on non-standard items

Allocation:

- 9% of Total



Cost estimate

- Mechanical engineering
 - MIT-Bates mechanical engineering division: MIT
- Electronics engineering
 - ANL and MIT-Bates electronics engineering division: ANL / MIT
- Silicon lab
 - LNS Silicon laboratory (PHOBOS production facility): MIT
- Assembly and integration (BNL Physics Department silicon lab): BNL / MIT
- Computing / Software: LBL / MIT
- DAQ integration: ANL / MIT



Cost estimate

□ Labor

Institute (6.5)	MIT (4.5)	BNL (2)
Mechanical FTE (3.5) (Engineer / Technician)	1.5 (\$300k) / 1 (\$100k)	0.5 (\$100k) / 0.5 (\$50k)
Electrical FTE (3) (Engineer / Technician)	1 (\$200k) / 1 (\$100k)	0.5 (\$100k) / 0.5 (\$50k)
Total:	\$500k / \$200k	\$200k / \$100k

(1 FTE: 1 Full-Time Employee per year including overhead)

Total: \$1300k (With 30% contingency)

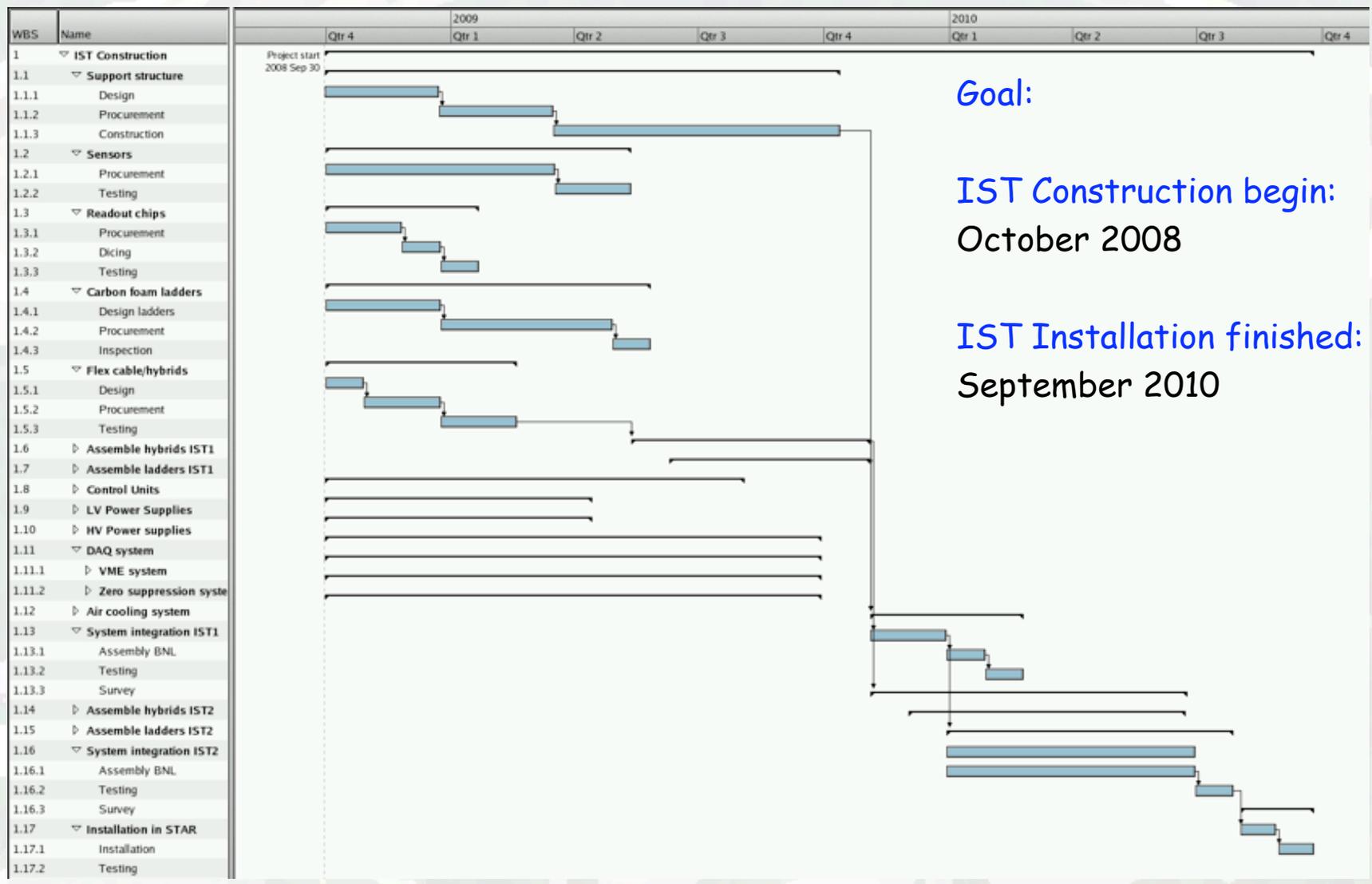
Total IST project cost: Material (\$4525k) + Labor (\$1300k) = \$5825k

(Estimated contributed labor (Not subtracted): 0.5 FTE (Technician))



Schedule

IST work flow - WBS



Goal:

IST Construction begin:
October 2008

IST Installation finished:
September 2010