# Adapting CMOS Sensors to STAR Vertex Detectors

**Marc Winter** (IReS/IPHC-Strasbourg)

▷ **More information on IPHC Web site:** **http://wwwires.in2p3.fr/ires/web2/rubrique.php3?id_rubrique=63**

## OUTLINE

- **Team composition and Activities**
- **Remarks on experimental trends ⟼ Limits of existing devices for flavour tagging**
- **The solution of CMOS sensors:**
  ↪ **Principle of operation – Advantages & Concerns – R&D directions – Typical performances**
- **Performances relevant for STAR achieved since 2003 (MIMOSA-5)**
- **Remaining steps for the MimoSTAR IV Detector**
- **Requirements and Plans for the Ultimate Detector**
- **Summary**

- **Team Composition: 13 staff (10 engineers, 3 physicists), 2 temporary, 7 PhD**
  - ◇ **Micro-circuit designers:** C.Colledani, M.Dahoumane (Doc.), A.Dorokhov (Post-doc), W.Dulinski, F.Guilloux, S.Heini (Doc.), A.Himmi, Ch.Hu, M.Koziel (Doc.), O.Robert, M.Szelezniak (Doc.), I.Valin
  - ◇ **Micro-circuit test engineers:** G.Claus, M.Goffe, K.Jaaskelainen, M.Pellicioli
  - ◇ **Physicists:** J.Baudot, A.Besson, M.Deveaux (Doc.), D.Grandjean (Doc.), A.Shabetaï (Doc.), M.Winter

- **Activities:**
  - ◇ **Development of CMOS sensors for:**
    - ○ vertex detectors: STAR upgrade (RHIC), CBM (GSI), ILC, EUDET telescope (FP6)
    - ○ imaging devices: HPD, electron microscopes, comfocal fluorescence microscopes, etc.

  ↪ R&D of CMOS sensors = National project of IN2P3 (IReS/IPHC, IPNL, LPSC, LPCC)

  .....

  - ◇ **Studies of vertex detector geometries for:** ILC, CBM
  - ◇ **Studies on physics potential of ILC:** Measurement of Higgs couplings to fermions and bosons
  - ◇ **Coordination of activities:**
    - ○ Conception of ILC vertex detector (Europe)
    - ○ Generic R&D of CMOS sensors at IN2P3
    - ○ CMOS sensor telescope for the EUDET project

# WHAT TRIGGERS THE R&D ON

# CMOS SENSORS ?

# General Trend in Vertexing Requirements

- **Flavour tagging takes growing importance in understanding the dynamics underlying heavy ion and particle physics phenomena $\longmapsto$ b, c, $\tau$ tagging with High Efficiency & Purity !**

  $\hookrightarrow$ **Aim for an ultra-light, very granular, poly-layer Vertex Detector installed very close to the interaction point**

  $\hookrightarrow$ **Demanding running conditions (occupancy, radiation) !!!**

- **Existing technologies are not adequate:**

  ⁕ **CCD (SLD): granular and thin BUT too slow and radiation soft**

  ⁕ **Hybrid Pixel Sensors (Tevatron, LHC): fast and radiation hard BUT not granular and thin enough**

  $\hookrightarrow$ **CMOS sensors are expected to provide a good trade-off between granularity, material budget, radiation tolerance and speed**

# PRINCIPLE OF OPERATION

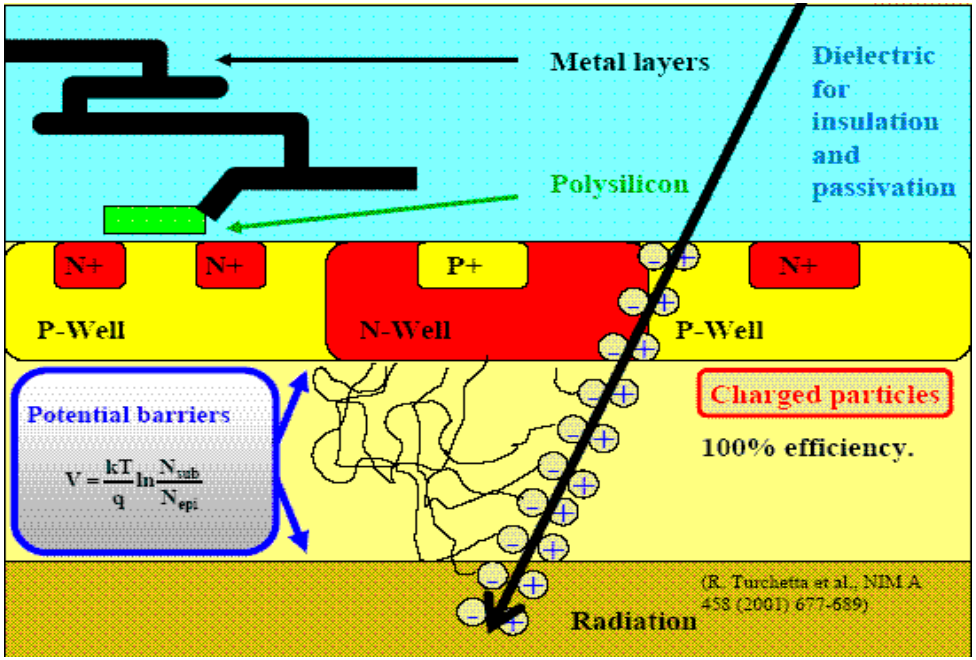
# AND SPECIFIC FEATURES

# OF CMOS SENSORS

# Main Features and Advantages of CMOS Sensors

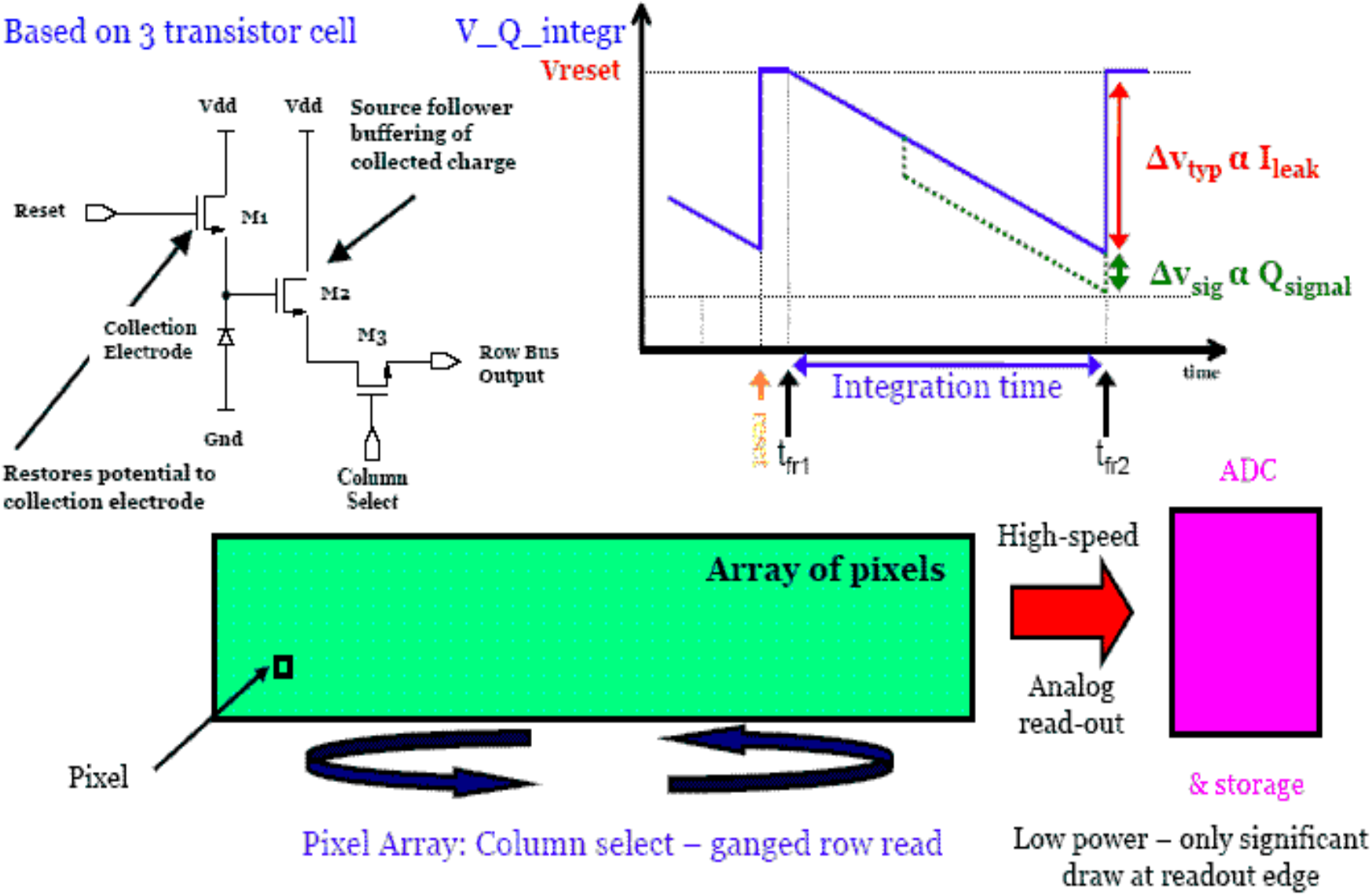
- p-type low-resistivity Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):

    $Q \sim 80$ e-h / $\mu m \mapsto$ signal $\lesssim 1000\ e^-$
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode with help of reflection on boundaries with p-well and substrate (high doping)



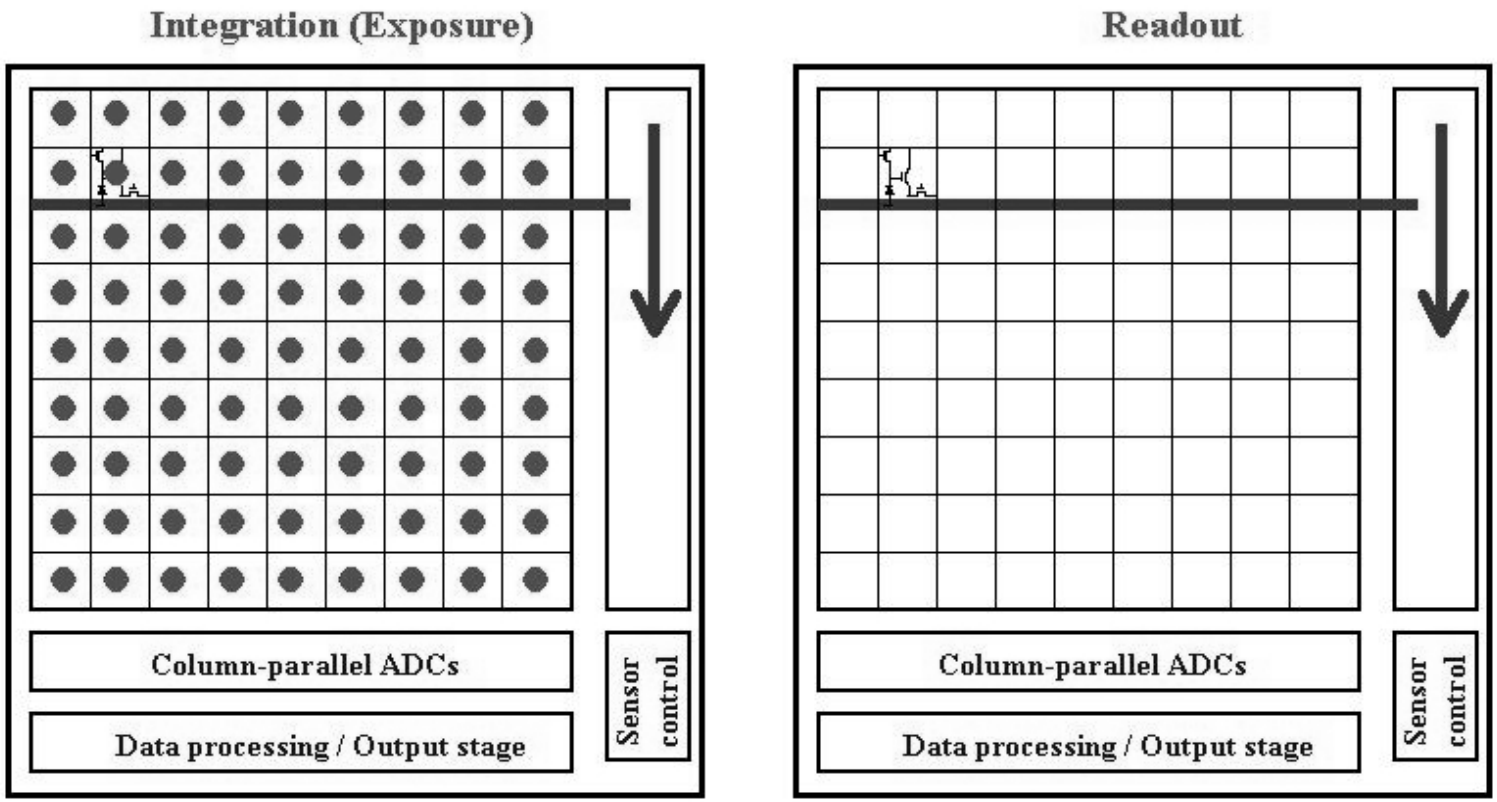

- Specific advantages of CMOS sensors:
  - ◇ Signal processing $\mu$circuits integrated on sensor substrate (system-on-chip) $\mapsto$ compact, flexible
  - ◇ Sensitive volume ($\sim$ epitaxial layer) is $\sim$ 10–15 $\mu m$ thick $\longrightarrow$ thinning to $\lesssim$ 30 $\mu m$ permitted
  - ◇ Standard, massive production, fabrication technology $\longrightarrow$ cheap, fast turn-over
  - ◇ As granular and thin as CCDs, BUT faster and more radiation tolerant

# Basic Read-Out Architecture



# Basic Read-Out Architectures

- **Two different ways of reading out the sensor:**
  - ◇ **Rolling Shutter mode (see below): array is read out row after row**
    - ↪ **each row is slightly shifted in time w.r.t. previous ones**
  - ◇ **Snap-shot mode (rather suited to imaging): all rows read out at once**
    - ↪ **dead time before/during pulsing all rows and during read-out**



# Main R&D Directions

- **High read-out speed, low noise, low power dissipation, highly integrated signal processing architecture:**
  - analog part (charge collection, pre-amp, CDS, ...) inside pixel
  - mixed (ADC) and digital (sparsification) micro-circuits integrated aside of active surface

- **Optimal fabrication process:**
  - epitaxial layer thickness
  - number of metal layers
  - yield
  - (dark current)
  - cost
  - life time of process

- **Radiation Tolerance:**
  - dark current
  - doping profile
  - (latch-up)

- **Industrial thinning procedure:**
  - minimal thickness
  - yield
  - individual chips rather than wafers

# M.I.P. TRACKING PERFORMANCES:

## PIXEL & CLUSTER CHARACTERISTICS,

## DETECTION EFFICIENCY

- **5 – 6 different fabrication processes explored with 15 MIMOSA proto. $\mapsto$ feature size (epitaxy)**
  - ⁕ **AMS: 0.6 $\mu m$ (14 $\mu m$), 0.35 $\mu m$ ( 0 !!!), 0.35 $\mu m$ OPTO ($\gtrsim$ 10 $\mu m$),**
  - ⁕ **AMI (former MIETEC): 0.35 $\mu m$ (4 $\mu m$),**
  - ⁕ **IBM: 0.25 $\mu m$ (2 $\mu m$),**
  - ⁕ **TSMC: 0.25 $\mu m$ ($\lesssim$ 7 $\mu m$)**

- **Most sensors characterised with particle beams (CERN, DESY)**

  $\hookrightarrow$ **tracking performances well assessed**

- **Outcome of $\gtrsim$ 6 years of R&D is very convincing:**
  - ◇ **Excellent m.i.p. detection efficiency and single point resolution well established**
  - ◇ **Radiation tolerance investigated partly: good performances obtained**
  - ◇ **Thinning well advanced: very satisfactory outcome**
  - ◇ **Fast integrated signal processing concentrates the efforts: analog part $\sim$ OK**

    $\hookrightarrow$ **mainly mixed (ADC) and digital micro-circuits**

# Exploration/Characterisation of Fabrication Processes

- **Why exploring fabrication processes ?**

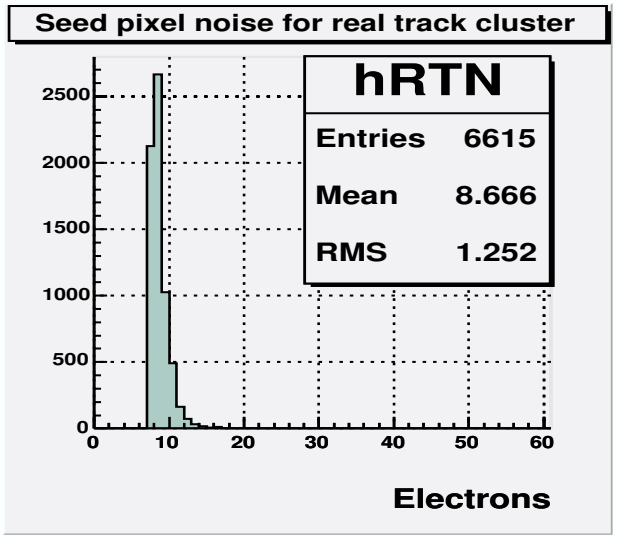
  ↪ **determine epitaxy thickness, $I_{leak}$(T, rad. dose), rad. tolerance, noise, ...**

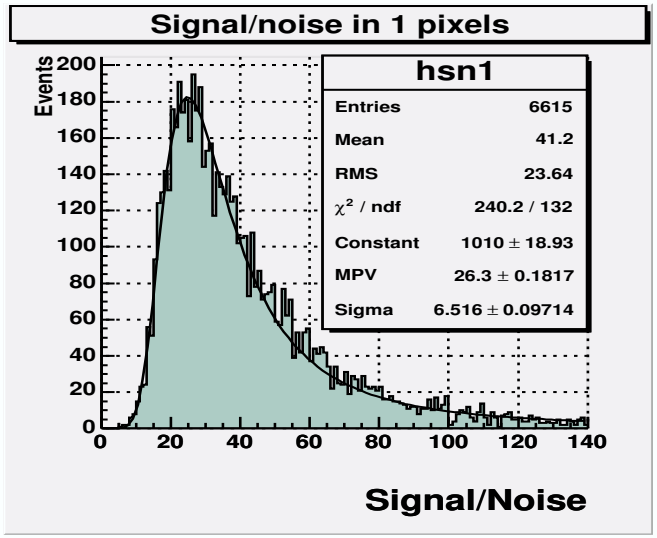
- **AMS-0.35 OPTO process first tested in 2004 (MIMOSA-9):**

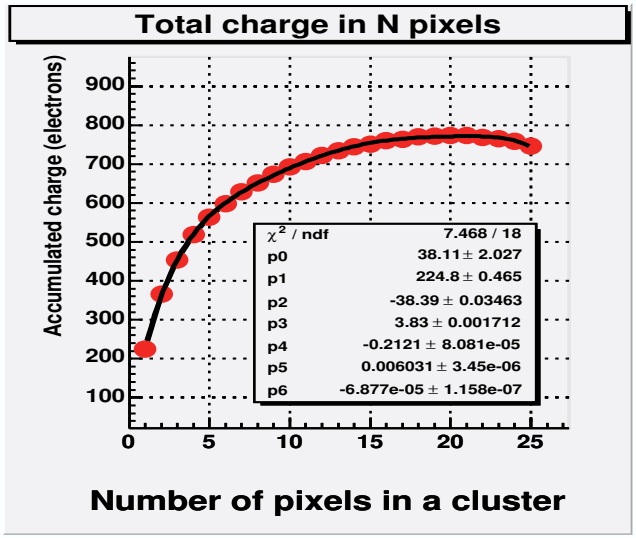
  ◇ **pitch: 20, 30, 40 $\mu m$** ◇ **diode size: 3.4x4.3, 5x5, 6x6 $\mu m^2$**

- **Excellent m.i.p. detection performances (assessed with 120 GeV/c $\pi^-$ at CERN-SPS):**

  ◇ **S/N $\sim$ 20-30 (MPV) $\longrightarrow$ $\epsilon_{\mathbf{det}}$ $\sim$ 99–99.9 %** ◇ **$\sigma_{sp}$= 1.5 $\mu m$ (20$\mu m$ pitch) $\longrightarrow$ 5 $\mu m$ (40$\mu m$ pitch)**



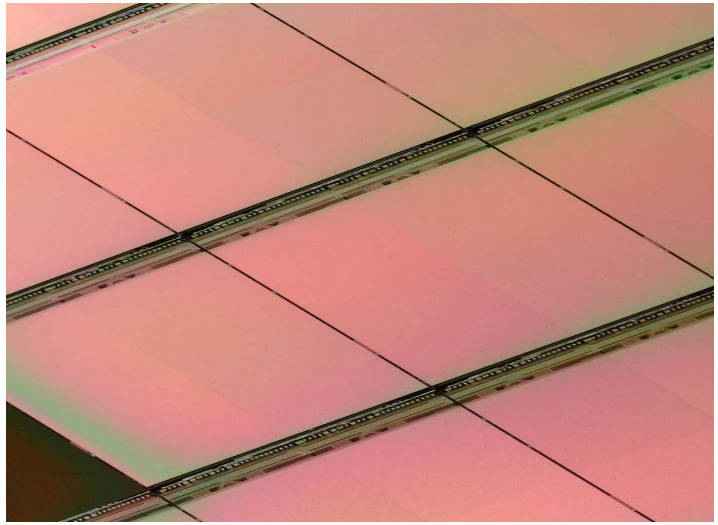



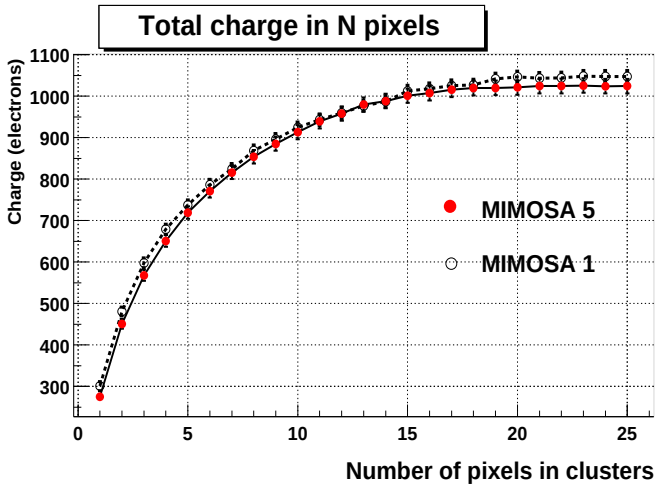



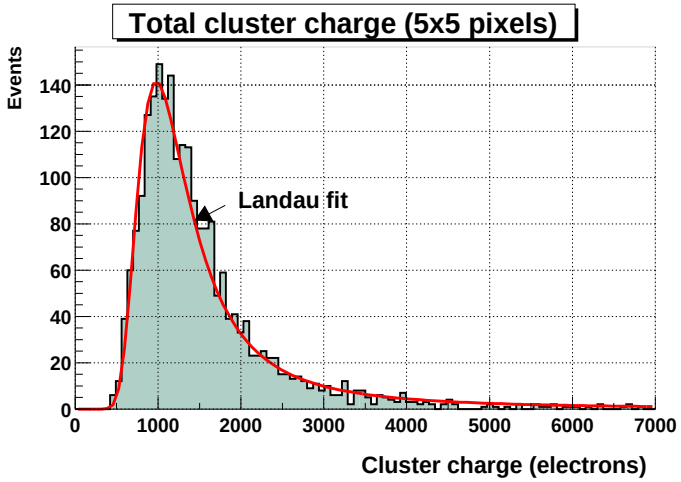

▷ **AMS-0.35$\mu m$ OPTO: most attractive process tested up to now ↦ baseline for further sensor R&D**

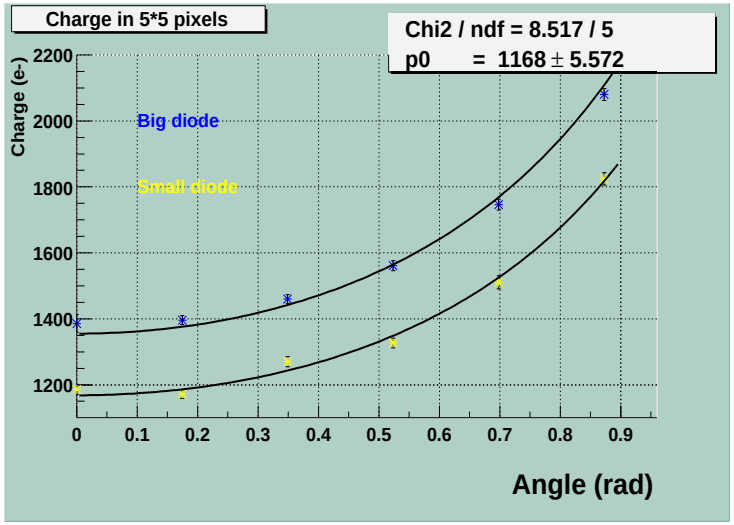
# Performances of a Reticle Size Sensor

- MIMOSA-5: 19.4 x 17.4 mm$^2$ wide chips made of $\sim$ 1 million pixels
  $\hookrightarrow$ AMS-0.6 $\mu m$ technology (like small MIMOSA-1 prototype)
- Electrical tests $\mapsto$ yield $\lesssim$ 40 %
- Uniformity of performances (tests with 120 GeV/c $\pi^-$):
  - $\diamond$ $\mathbf{Q^{M5}_{clus} \cong Q^{M1}_{clus} \mapsto \epsilon_{det} \sim 99\%}$
  - $\diamond$ $\sigma_{sp} \lesssim 2\mu m$
  - $\diamond$ average pixel gain uniformity: $\pm 0.3\%$






- Yield of sensors with integrated signal processing ?
- Consequences on stitching possibilities ?

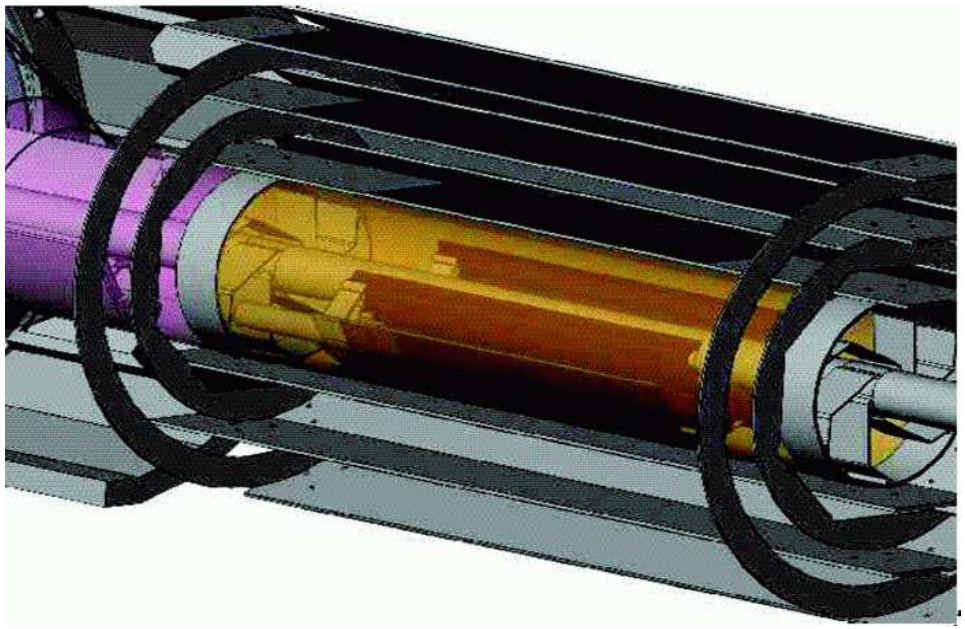
# ADAPTING MIMOSA SENSORS TO

# STAR VERTEX DETECTOR UPGRADE

# Main Requirements for MimoSTAR IV Detector

- **Objective: equip 2 cylindrical layers at radii $\sim$ 15 mm & 50 mm $\mapsto$ $\sim$ 1000 cm$^2$**

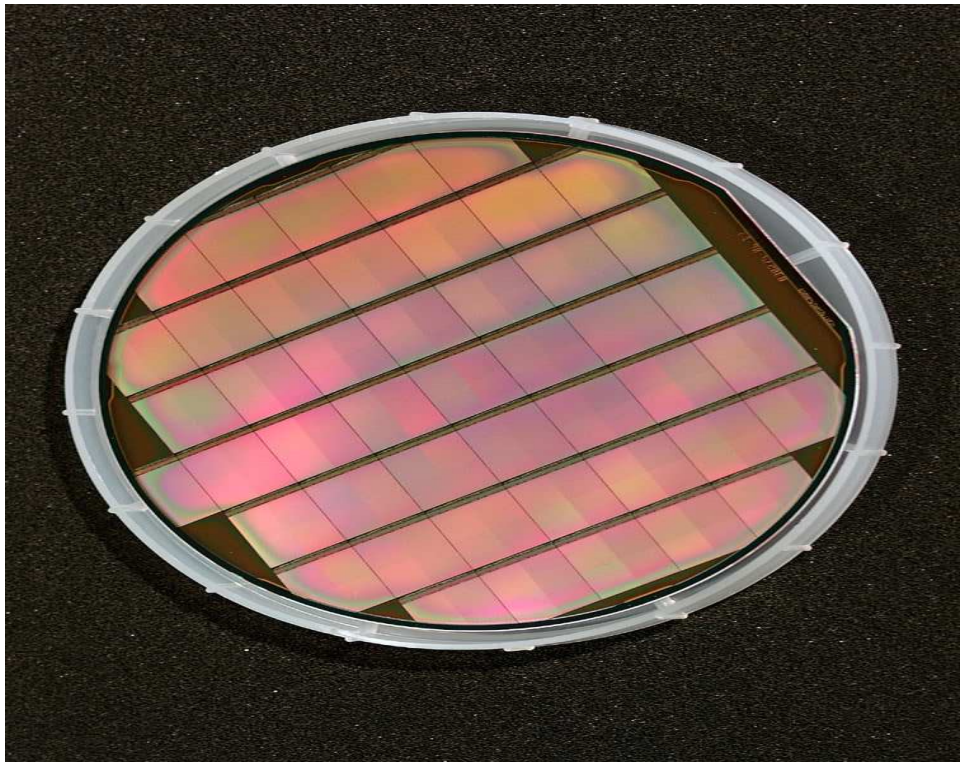
- **Requirements for sensors equipping the 6 + 18 ladders:**
  - **Detection efficiency $\gtrsim$ 98 %**
  - **Single point resolution $<$ 10 $\mu m$**
  - **Thickness $<$ 80 $\mu m$**
  - **Read-out time $<$ 5 ms**
  - **Power dissipation $\lesssim$ 100 mW/cm$^2$**
  - **Radiation tolerance:**
    - ◇ **few 10$^{11}$ $\pi^{\pm}$/cm$^2$/yr**
    - ◇ **5 - 10 kRad/yr**
  - **Operating Temperature $\lesssim$ 30$^0$C (air cooling only)**
    - $\hookrightarrow$ **can be challenging after irradiation !!!!**



- **MIMOSA-5 (fabricated in 2002) was not far from these requirements**

# Comparison of MIMOSA-5 Perfo. to Upgrade Requirements

- ⊗ Detection efficiency $>$ 99 %
- ⊗ Single point resolution $<$ 2 $\mu m$ (17 $\mu m$ pitch)
- ⊗ Power dissipation $\sim$ 10 mW/cm$^2$
- ⊖ Read-out time: 25 ms
- ⊖ Thickness after industrial thinning: 120 – 130 $\mu m$
- ⊖ Yield: $\lesssim$ 40 %
- ⊖ Operating temperature:
  - $\lesssim$ 20$^0$C before irradiation
  - $\lesssim$ 0$^0$C after irradiation !!!!
    (100 kRad, few 10$^{11}$ n$_{eq}$/cm$^2$)



▷▷▷ **Main requests of improvement:**

**Operating temperature after irradiation** – Thinning – Read-out speed – Yield

# Objectives of the 2004 – 2005 Development

- **Reduce read-out time from 25 ms to 4 ms but keep power consumption $<$ 100 mW/cm$^2$**

- **Validate industrial thinning $<$ 80 $\mu m$ (instead of 120 $\mu m$)**

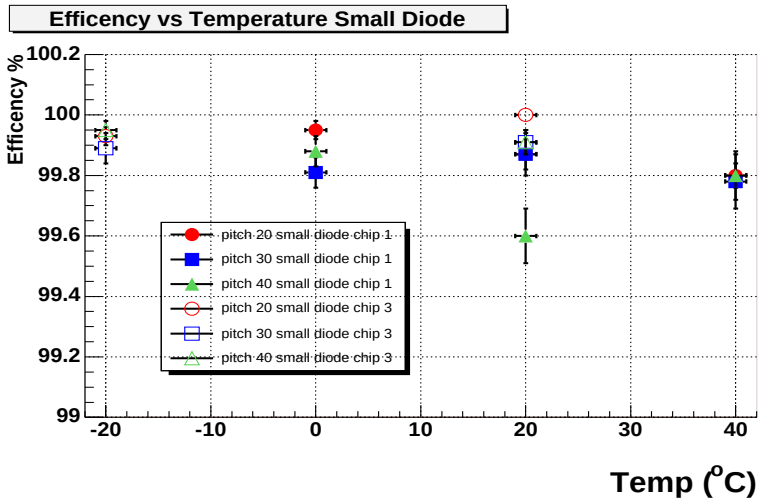
- **Improve radiation tolerance at T $\sim$ 30 – 40$^0$C**
  - **Improve pixel architecture to reduce sensitivity to leakage current increase after irradiation**
  - **Find a fabrication process featuring:**
    - **reduced leakage current $\mapsto$ squeeze the electronic noise**
    - **epitaxial layer with satisfactory thickness $\mapsto$ enhance signal charge**

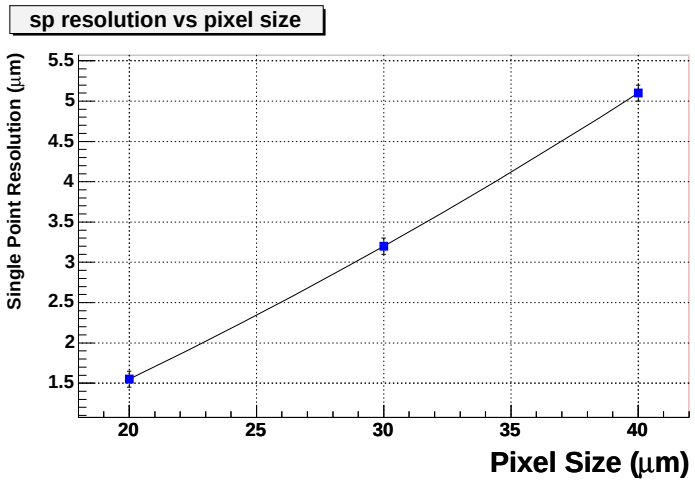
- **Adjust pixel pitch to read-out speed, power consumption and single point resolution :**
  - **17 $\mu m$ $\mapsto$ 30 $\mu m$ improves read-out spead and reduces consumption**
  - **check that detection efficiency, single point and double hit resolutions remain OK**

- **Watch fabrication yield**

# Results of the 2004/2005 R&D (1/3)

- 5 MIMOSA prototypes (M-9, M-10, M-11, M-14, M-15) designed, fabricated and tested in 2004/2005
- Extensive study of AMS-0.35 $\mu m$ OPTO process characteristics ( ... may be available for 10 yrs ...):
  - epitaxial layer $\sim$ 11 – 12 $\mu m$ $\mapsto$ signal $\sim$ 800 electrons
  - leakage current 10 - 100 times smaller than standard
  - pitch varied from 20 to 40 $\mu m$




$\hookrightarrow$ $\epsilon_{det} \gtrsim$ 99.8 % up to +40°C – $\sigma_{sp} \sim$ 3 $\mu m$ for 30 $\mu m$ pitch

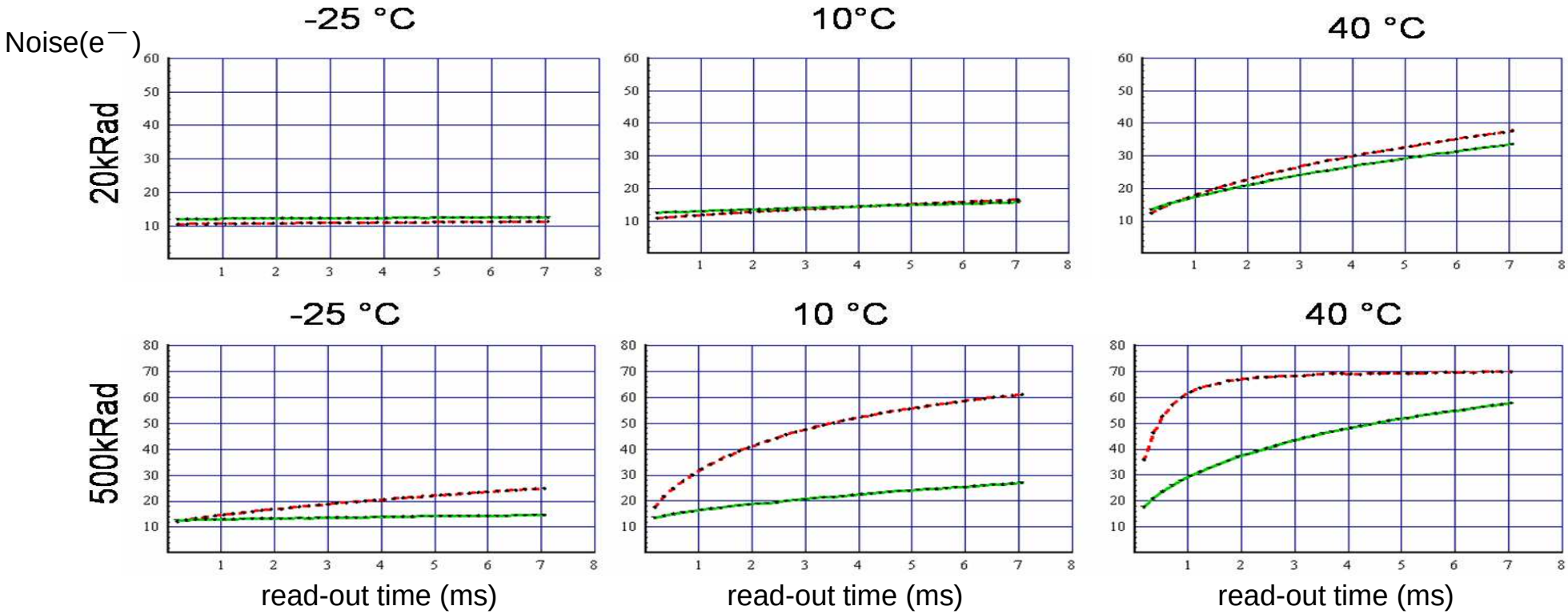
- Several tens of MIMOSA-5 chips thinned to 50 $\mu m$
  - $\hookrightarrow$ mounted sucessfuly on prototype ladders (LBL) and operated

# Results of the 2004/2005 R&D (2/3)

## Tolerance to non-ionising radiation (measured at T = 0°C):

| Fluence | 0 | $3 \cdot 10^{11}$ $n_{eq}/cm^2$ |
|---|---|---|
| S/N | 21.8 ± 0.2 | 17.6 ± 0.3 |
| $\epsilon_{det}$ | 99.88 ± 0.02 % | 99.56 ± 0.13 % |

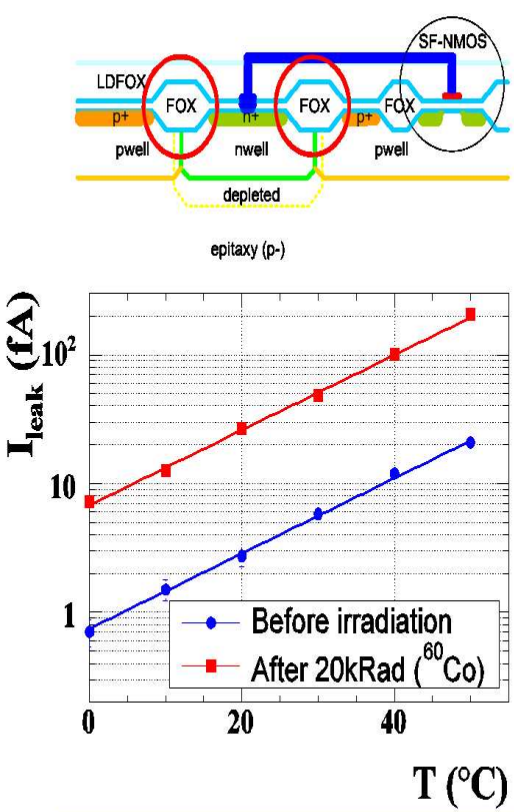
## Tolerance to ionising radiation (10 keV X-Rays):

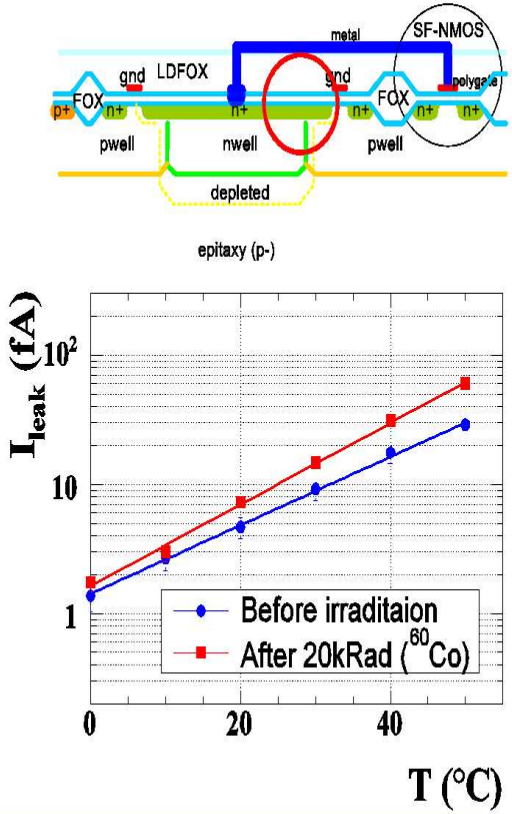


# Improving Tolerance to Ionising Radiation

- **Pixel designs avoiding thick oxide around N-well and including guard-ring**

## Studies on radiation hardness (ionising): MIMOSA9

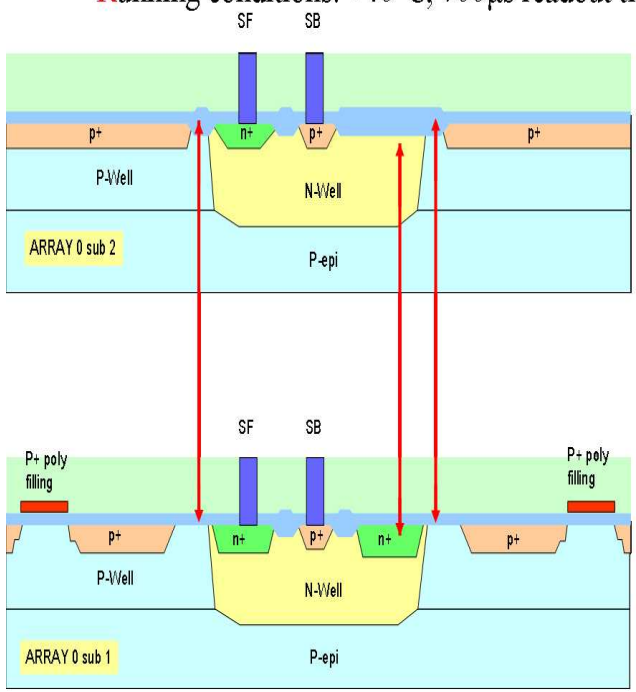



Increase of leakage current depends on the diode layout.
Probable reason: Presence of thick oxide (FOX) near the diode.

## Beamtest on MIMOSA11

Running conditions: +40°C, 700µs readout time

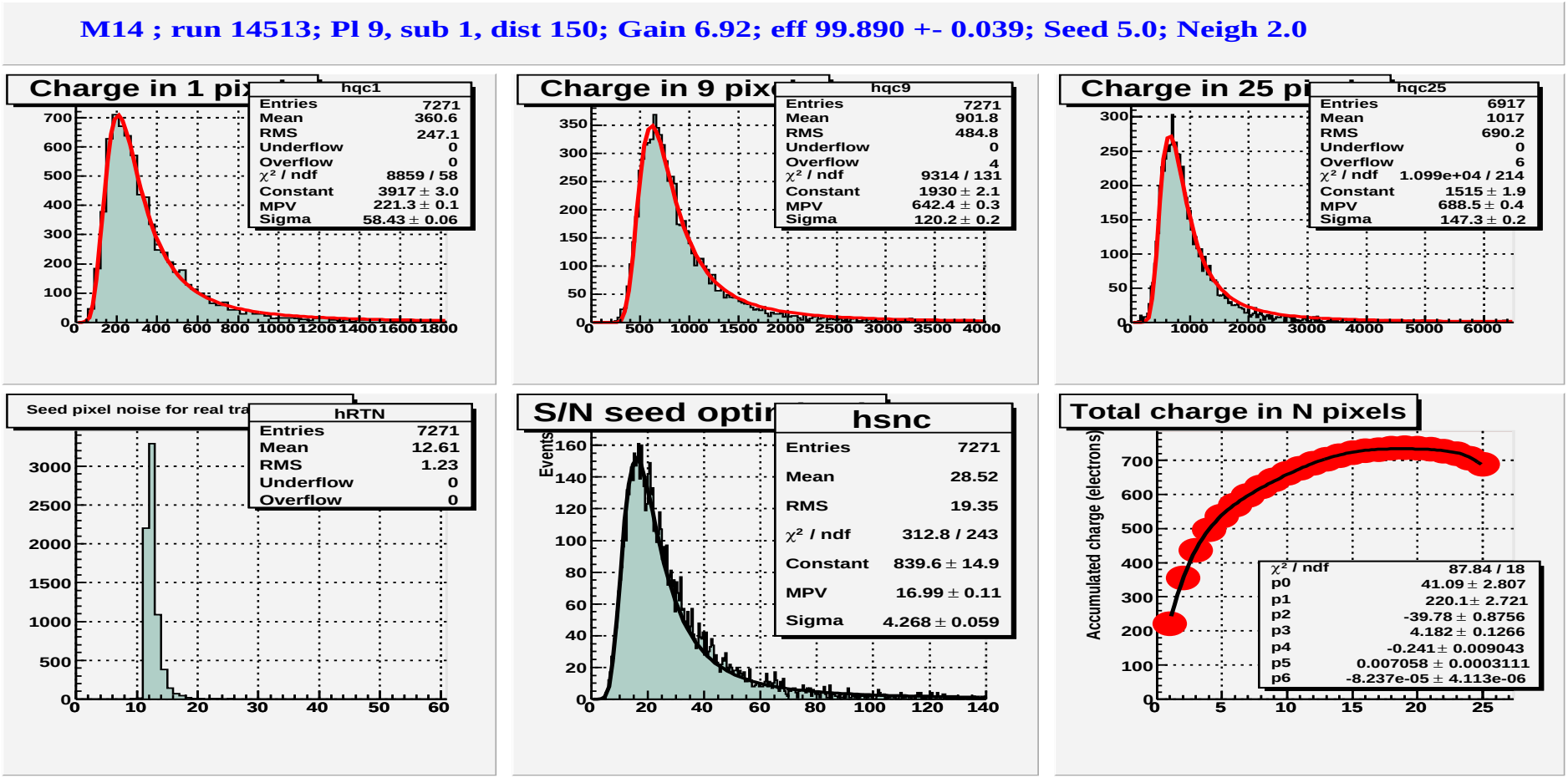



| | New | After 20kRad |
|---|---|---|
| **Standard pixel (A0 Sub 2)** | | |
| S/N (MPV): | 23.9 | 10.3 |
| Det Eff [%]: | 99.9 | 97.7 |
| Noise [e$^-$]: | 10.7 | 23.5 |
| **Hardened pixel (A0 Sub 1)** | | |
| S/N (MPV): | 14.9 | 15.1 |
| Det Eff [%]: | 99.5 | 99.6 |
| Noise [e$^-$]: | 16.1 | 16.1 |

Radiation hardened pixel remains stable after irradiation.
Obvious reason: Leakage current increases after irradiation slower than for the standard pixel.
S/N of the radiation hard pixel is not yet optimized (See MIMOSA15).

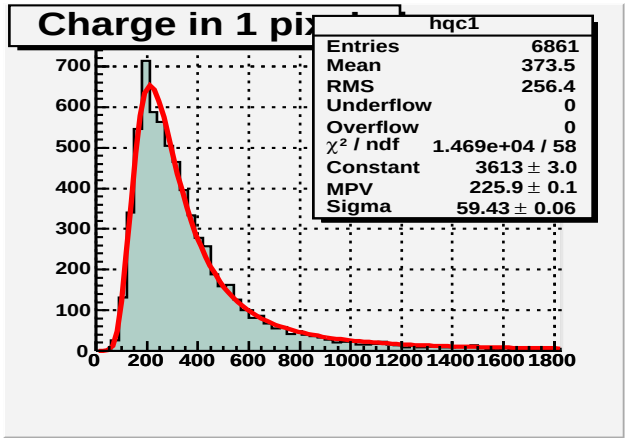
# MIMO★-2 Characteristics & Test Results

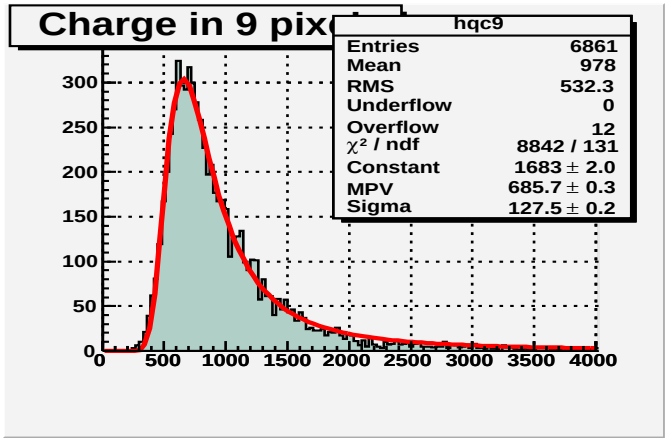
- **Fab. in AMS 0.35 $\mu m$ OPTO technology in Spring 2005 $\mapsto$ tested at DESY (5 GeV e$^-$) in Septembre**
  - ◇ **2 matrices of 64 x 128 pixels (30 $\mu m$ pitch) treated in // $\mapsto$ active area of 4 x 4 mm$^2$**
    - $\hookrightarrow$ **1 matrix with rad. hard pixels (already tested with MIMOSA-11)**
  - ◇ **JTAG architecture for steering**
  - ◇ **frame r.o. time: 0.8, 1.6, 4.0 ms (pixel r.o. frequency: 10, 4, 2 MHz)**

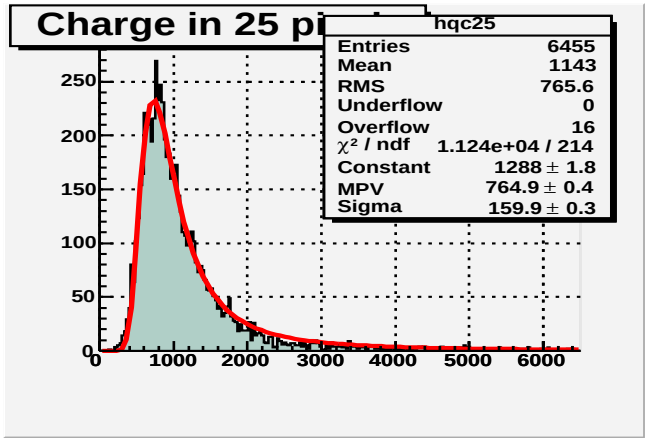


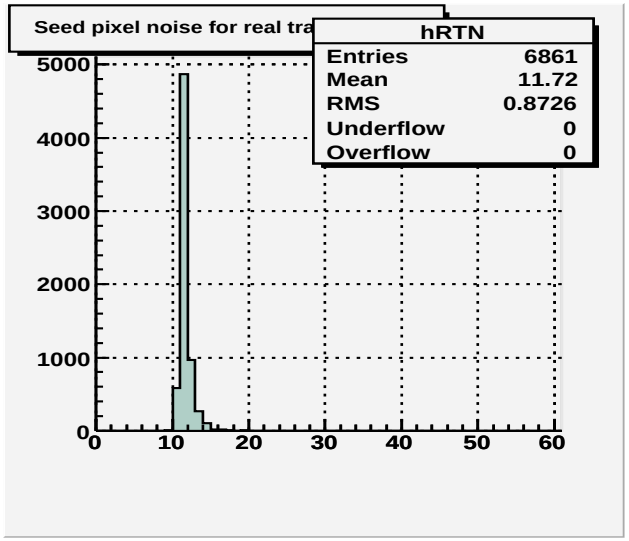
# MIMO★-2 Beam Test Results: 10 MHz and 20°C

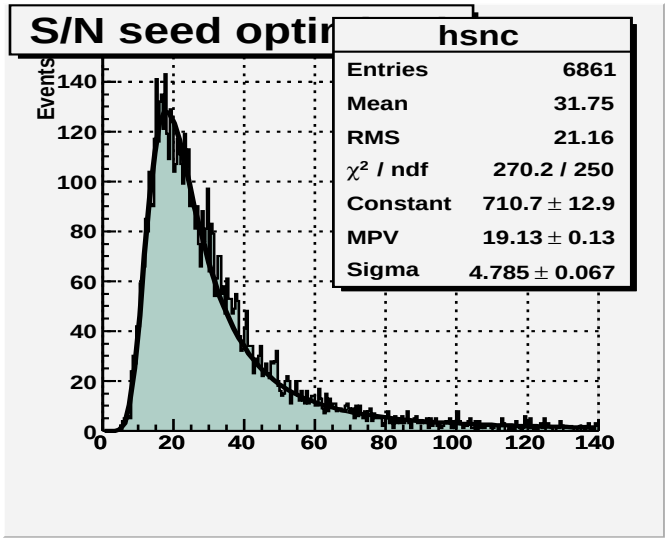
**M14 ; run 14512; Pl 9, sub 1, dist 150; Gain 8.00; eff 99.985 +- 0.015; Seed 5.0; Neigh 2.0**

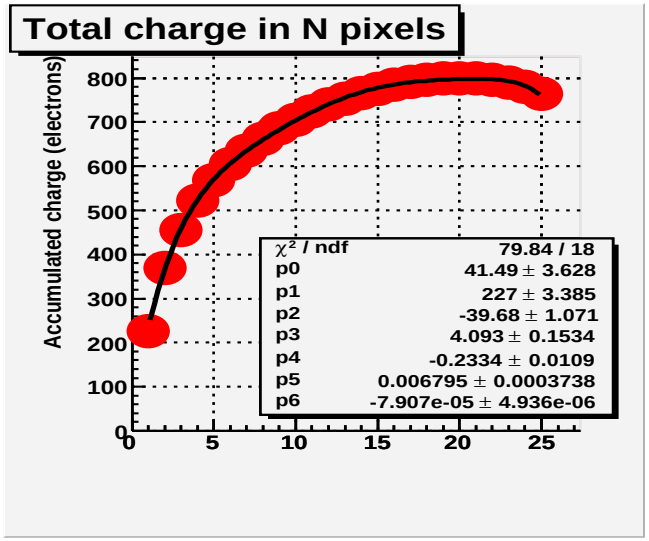


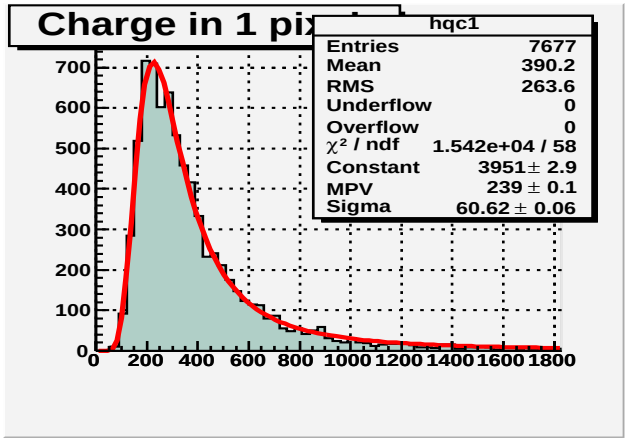



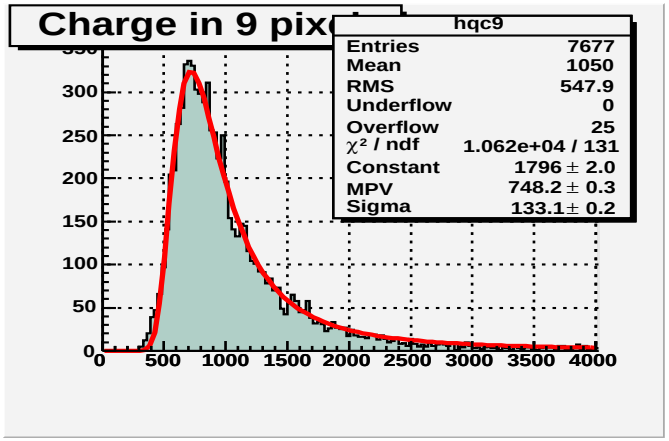



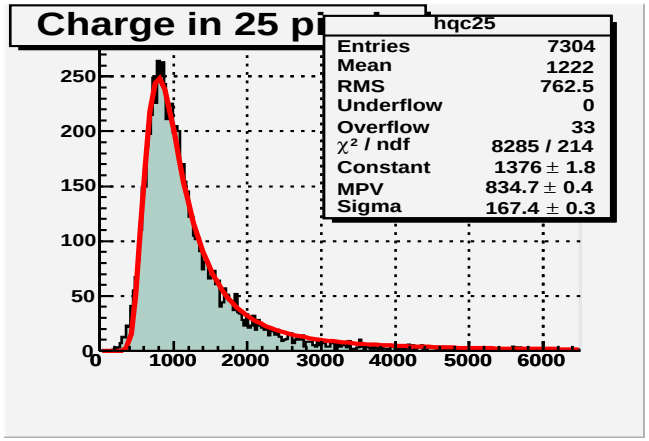



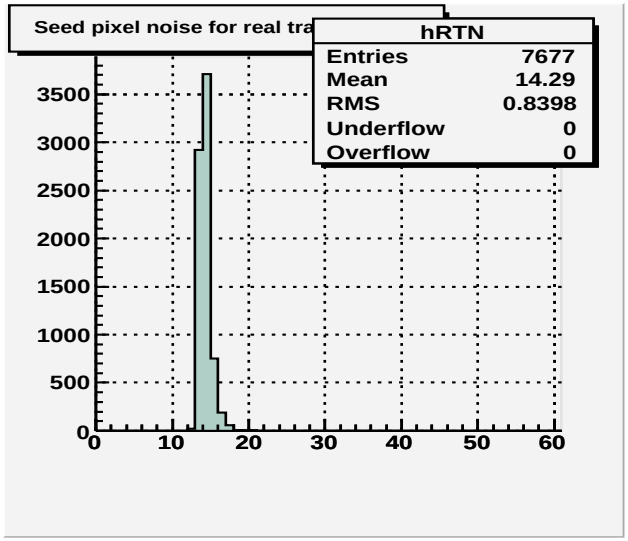
# MIMO★-2 Beam Test Results: 10 MHz and 40°C

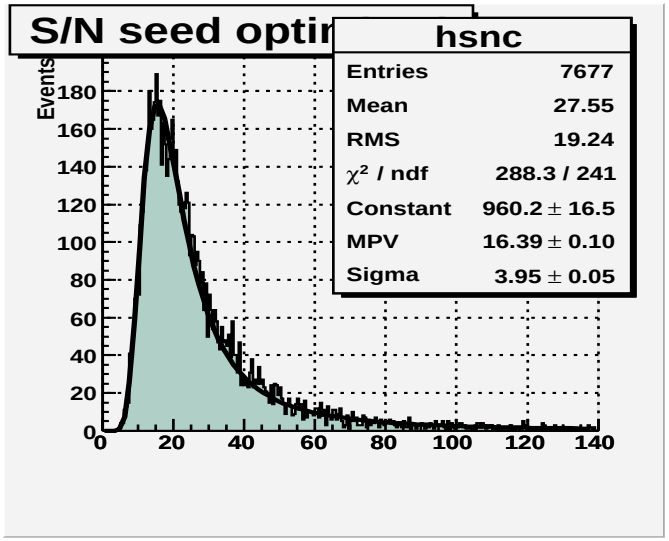
**M14 ; run 14508; Pl 9, sub 1, dist 150; Gain 8.24; eff 99.974 +- 0.018; Seed 5.0; Neigh 2.0**

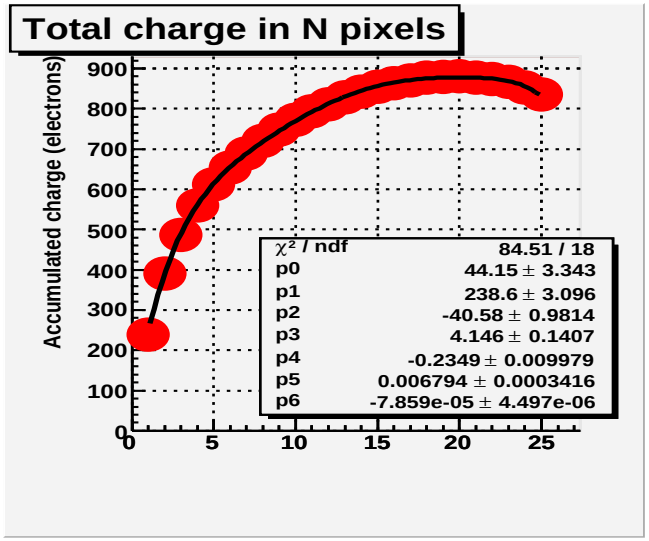


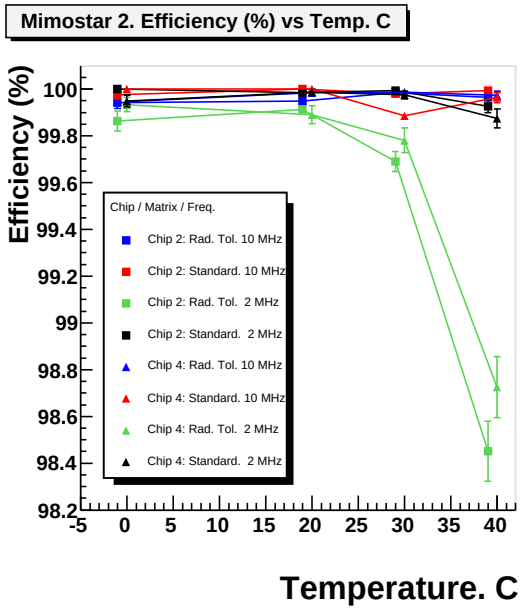



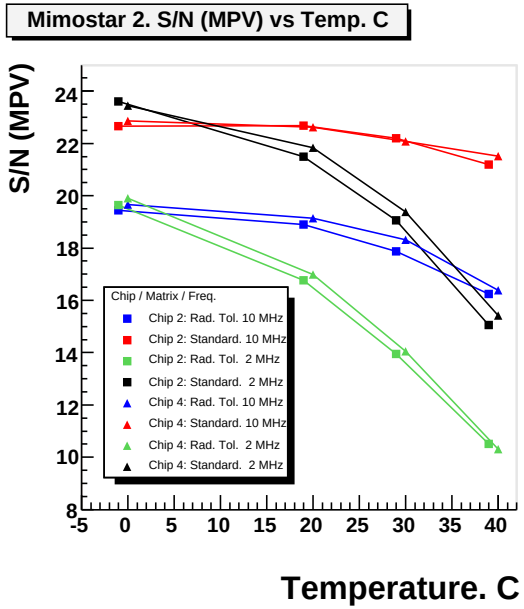



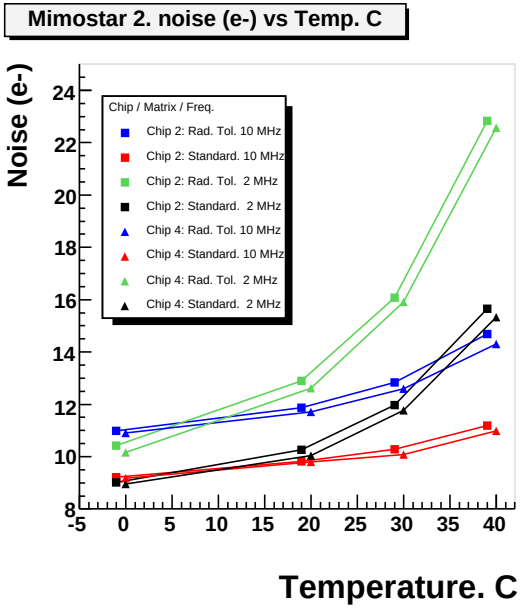
# Summary of MIMO★-2 DESY Beam Test Results

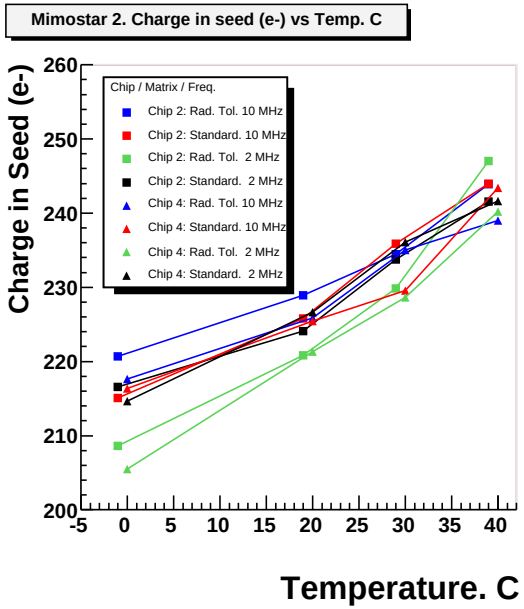
- JTAG design fully validated
- Main results at T = 25°C and $t_{r.o.}$ = 0.8 & 4 ms:
  - ∴ N ∼ 11 - 14 $e^-$ ENC
  - ∴ S/N ∼ 15 - 21 (MPV)
  - ∴ $\epsilon_{det} \gtrsim$ 99.8 %
  - ∴ $\sigma_{sp} \sim 3\ \mu m$ (from MIMOSA-9)
  - ∴ power dissipation ∼ 40 mW/cm$^2$




- CONCLUSION:
  - ◇ Architecture of sensor for MimoSTAR IV running conditions (T, radiation) validated
    - ↪ sensors in real environment end '06
  - ◇ Design of final prototype can start
    - ↪ ∴ fabrication $\gtrsim$ Summer '06
    - ∴ chips available for mounting ∼ end '06



# SUMMARY OF WORK ACHIEVED

# AND PLANS FOR THE MimoSTAR IV Chip

## Achieved performances:

- **Granularity:** 30 $\mu m$ ✓
- **Fab. process & S/N** $\mapsto$ $\epsilon_{\mathbf{det}} \gtrsim$ 99.5 % ✓
- **Read-out speed:** O(1 ms) ✓
- **Power dissipation:** few 10 mW / cm$^2$ ✓
- **Radiation tolerance:**
  - ※ ionising radiation at T = +40$^\circ$C : up to $\sim$ 1 MRad (t$_{int.}$ $<$ 1 ms ) ✓
  - ※ non-ionising radiation: up to $\sim$ 10$^{12}$n$_{eq}$/cm$^2$ ✓ check at T$_{room}$ still missing
- **Material budget:** industrial thinning of diced chips to 50 $\mu m$ ✓ yield still missing

## Remaining topics to address:

- **Radiation tolerance:**
  - ※ ionising radiation : check latch-up sensitivity (planned in the coming weeks)
  - ※ non-ionising radiation: check T$_{room}$ behaviour
- **Macroscopic detector** including all design features
  - $\hookrightarrow$ fabrication (and thinning) yield assessment & check of performance uniformity

# Plans for 2006 - 2007 $\mapsto$MimoSTAR IV Detector

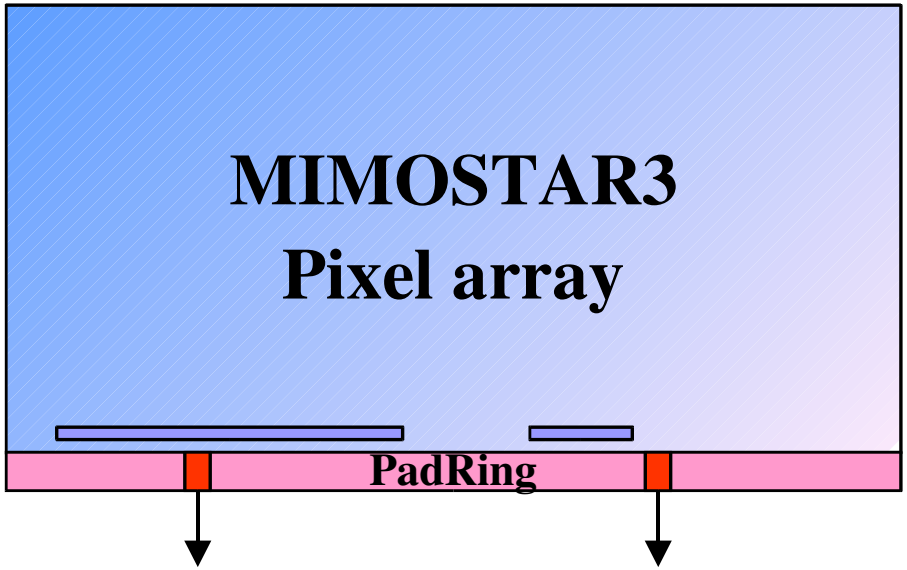
- **2006 $\mapsto$ Operate MIMO★-2 mounted on ladders in real experimental conditions:**
  - integrate chip operation in central STAR DAQ
  - estimate chip sensitivity to surrounding background

- **2006 $\mapsto$ Design, manufacture and test macroscopic chip demonstrator :**
  - assess final architecture operation
  - complete tests performed with MIMO★-2
  - assess fabrication yield
  - investigate whether "20 $\mu m$" epitaxial layer is more adequate than "14 $\mu m$"

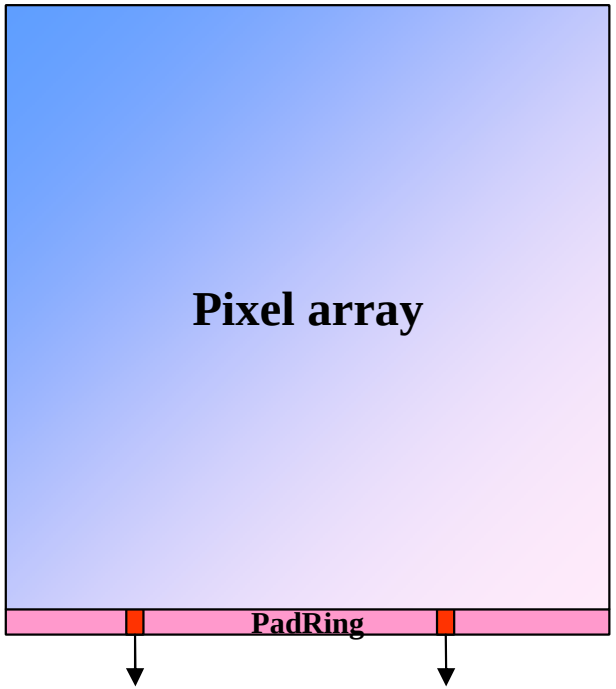
- **2007 $\mapsto$ Design, fabricate and test final sensors :**
  - equip $\sim$ 100 ladders of vertex detector (10 sensors per ladder)

# MIMO★-3: Characteristics & Time Line

- **Prominent characteristics:**
  - ※ AMS 0.35 $\mu m$ OPTO process ($\sim$ 12 $\mu m$ epitaxy)
  - ※ 640 x 320 pixels (30 $\mu m$ pitch)
    - $\hookrightarrow$ active surface: 19.2 x 9.6 mm$^2$
  - ※ 10 sub-arrays of 64 x 320 pixels treated in // at 10 MHz
    - $\hookrightarrow$ r.o. time $\sim$ 2 ms (2 output nodes at 50 MHz)




- **Production schedule:**
  - ※ Design under way, extrapolating from MIMO★-2
    - $\hookrightarrow$ Submission (engineering run) by end of June '06
      - $\hookrightarrow$ Wafer tests: Sept. '06
        - $\hookrightarrow$ Dicing & thinning: Oct. – Nov. '06
          - $\hookrightarrow$ Individual sensor tests: end '06 $\mapsto$ early '07




- **Prominent characteristics:**
  - ⁕ AMS 0.35 $\mu m$ OPTO process ($\gtrsim$ 12 $\mu m$ epitaxy)
  - ⁕ 640 x 640 pixels (30 $\mu m$ pitch)
    - ↪ active surface: 19.2 x 19.2 mm$^2$
  - ⁕ 10 sub-arrays of 64 x 640 pixels treated in // at 10 MHz
    - ↪ r.o. time $\sim$ 4 ms (2 output nodes at 50 MHz)

- **Production schedule:**
  - ⁕ Design by end '06 till Spring '07, extrapolating from MIMO★-3
    - ↪ Submission (production run) early April '07
      - ↪ Wafer tests: July – Aug. '07
        - ↪ Dicing & thinning: Sept.– Oct. '07
          - ↪ Individual sensor tests: Autumn '07 ↦ early '08

# PLANS FOR ULTIMATE CHIP

- **Change in time structure of event recording:**
  - ✳ event recorded only in case of trigger ($\sim$ 2 $\mu s$ latency)
  - ✳ TPC information recording requires $\sim$ 1 ms
  - ✳ event rate of interest is high $\mapsto$ trigger fires within a few $\mu s$
  - $\hookrightarrow$ running condition sequence: period ($\lesssim$ 10 $\mu s$ long) during which a trigger arrives with $\sim$ 2 $\mu s$ delay w.r.t. event of interest, followed by $\sim$ 1 ms long period without trigger

- **Luminosity increase:**
  - ✳ event rate increase $\mapsto$ risk of pile-up
  - ✳ radiation dose increase $\mapsto$ ◇ $\sim 10^{12} \pi^{\pm}$/cm$^2$/yr ◇ few 10 kRad/yr

oooooooooooooooooooooooooooooo

- **Natural solution = 2 step sensor architecture $\mapsto$ decoupled signal sensing and data transfer:**
  - ✳ continuous charge integration with 100 - 200 $\mu s$ integration time and in-pixel storage
    - $\hookrightarrow$ cope with event rate and leakage current due to radiation dose
  - ✳ signal transfer and processing restricted to triggered frames (charge encoded on 1 or 2 bits)
    - $\hookrightarrow$ contain power dissipation and data flow

$\mapsto$ **Main effort will be invested in low power dissipation architectures**

- **Main concern: keep power dissipation compatible with air flow cooling ($\lesssim$ 100 mW/cm$^2$)**
  - activity of sensor will be very restricted during TPC read-out time
  - data transfer and treatment will be relatively slow (several 100 $\mu s$) and restricted to minimal functionnalities

- **Sensor architectures under study $\mapsto$ pending questions:**
  - CDS either inside each pixel or integrated on side band and activated by trigger only
  - 2 memories inside each pixel sufficient ? which type ?
  - should triggered signal be discriminated ? 1 ou 2 thresholds ?
  - how many bits for signal charge encoding ? digital pixel resolution sufficient ?

- **Some answers already extractable from existing MIMOSA prototypes:**
  - fast column // architecture $\mapsto$ MIMOSA-8
  - various in-pixel amplification schemes $\mapsto$ MIMOSA-9, MIMOSA-15
  - etc.

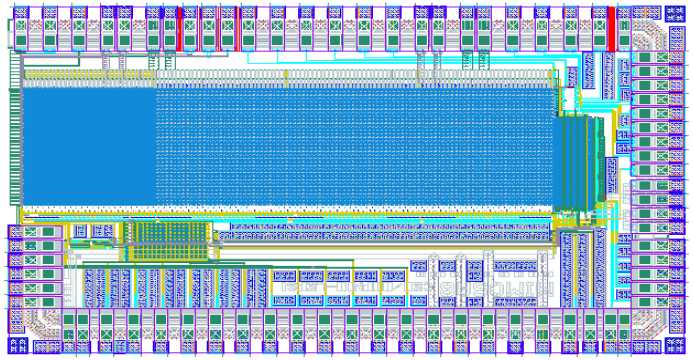
- **Several other design features of interest will be implemented on MIMO★-3 reticle**

- **Input expected from MIMO★-2/-3 tests in situ**

# High Read-Out Speed Architecture

## MIMOSA-8:

- TSMC 0.25 $\mu m$ digital fab. process (8 $\mu m$ epitaxy)
- 32 // columns of 128 pixels (pitch: 25 $\mu m$)
- 4 sub-arrays featuring AC and DC coupled on-pixel voltage amplif.
- on-pixel CDS
- discriminator at end of each column



## Tests with $^{55}$Fe source:

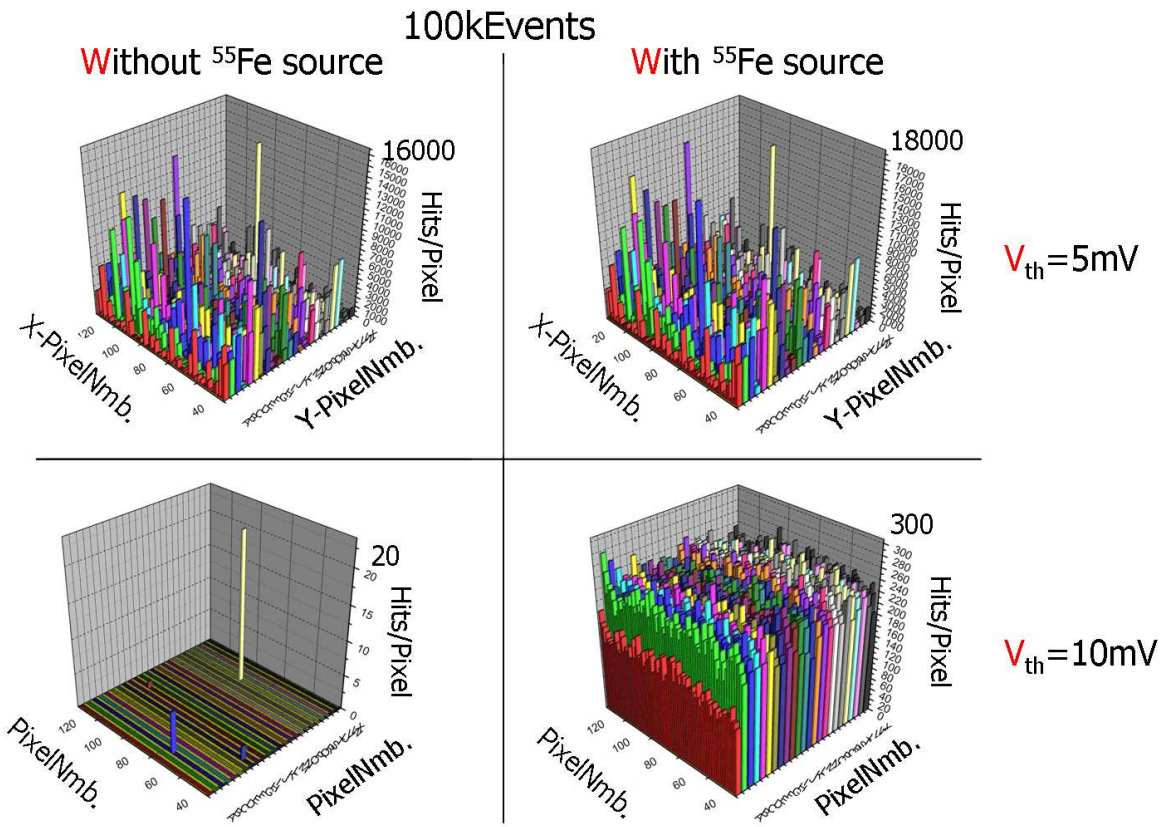
◇ conversion factor: 50 – 110 $\mu V$/e$^-$,

◇ pixel noise (including CDS): $\sim$ 13 – 18 e$^-$ ENC !

◇ little pixel-to-pixel dispersion ($<$ 10 e$^-$ ENC)!

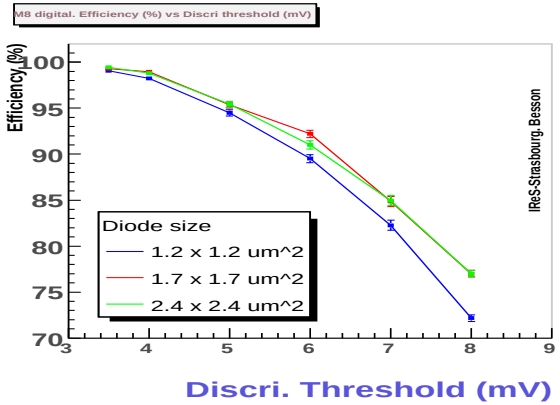
◇ discriminator operational:

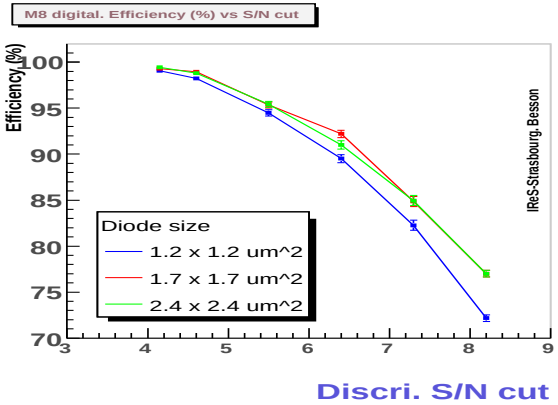
$\hookrightarrow$ discriminated $^{55}$Fe X-Ray clusters observed !

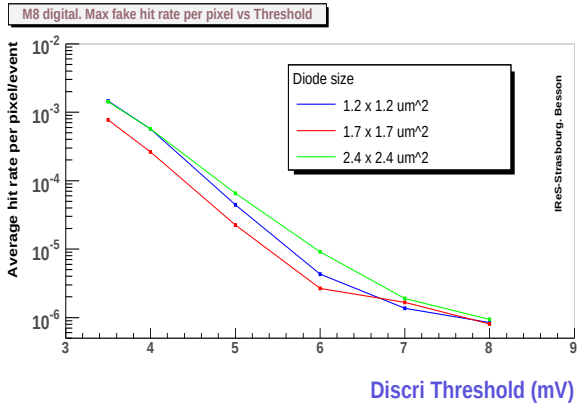


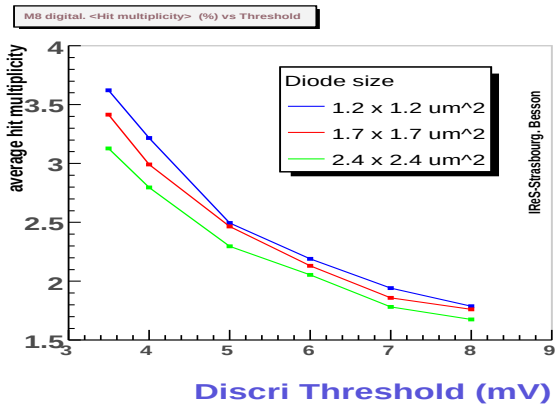
# Fast Col. // Chip with Discri Output: Beam Test Results

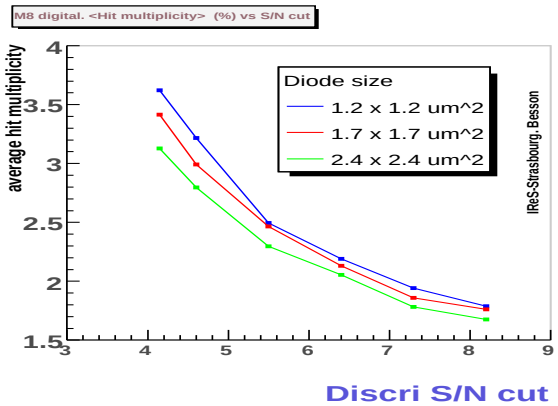
- **MIMOSA-8 tests with 5 GeV/c $e^-$ beam at DESY in September 2005**
- **Excellent m.i.p. detection performances despite modest thickness of epitaxial layer**
  - ◇ **det. eff. ∼ 99.3 % for fake rate of ∼ 0.1 %**
  - ◇ **discriminated cluster multiplicity ∼ 3–4**

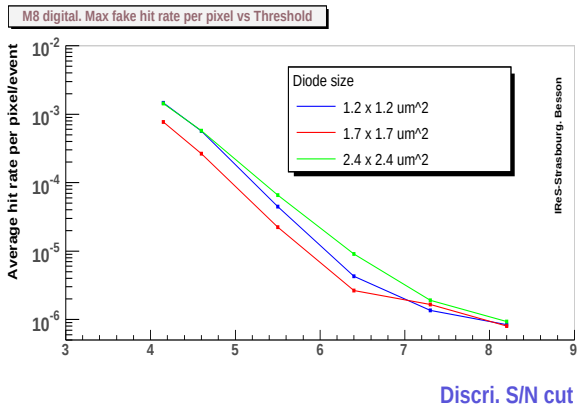



▷▷▷ **Architecture validated for next steps: techno., rad. tol. pixel at $T_{room}$, ADC, zero supp., etc.**

- **TSMC-0.25: $\lesssim$ 7 $\mu m$ epitaxy thickness $\mapsto$ signal $\sim$ 450 e$^-$**

  **AMS-0.35 OPTO: $\lesssim$ 11 – 12 $\mu m$ epitaxy thickness $\mapsto$ signal $\sim$ 700 – 800 e$^-$**

  $\hookrightarrow$ **translate MIMOSA-8 in AMS-0.35 OPTO in order to improve S/N ($\mapsto \epsilon_{det}$ vs fake hits)**

- **First step $\mapsto$ MIMOSA-15 (fabricated in Summer 2005):**
  - ⁕ **pixel with integrated C.D.S. design of MIMOSA-8**
  - ⁕ **2 diode sizes: 1.7 x 1.7 $\mu m^2$ and 2.4 x 2.4 $\mu m^2$**

- **Tests with $^{55}$Fe:**
  - ⁕ **CVC $\sim$ 50 $\mu V/e^-$**
  - ⁕ **Noise $\lesssim$ 10 e$^-$ ENC**
  - ⁕ **Q$_{seed}$ $\sim$ 10 % of Q$_{tot}$ (instead of $\sim$ 25 %)**
  - ⁕ **Q$_{3X3}$ $\sim$ 30 % of Q$_{tot}$ (instead of $\gtrsim$ 80 %)**

  $\hookrightarrow$ **CVC and noise very close to MIMOSA-8** $\mapsto$ **ready for translation of complete MIMOSA-8 chip**

  $\hookrightarrow$ **BUT less signal charge collected** $\mapsto$ **increase sensing diode size**

$\triangleright\triangleright\triangleright$ **Next step: full translation within MIMO★-3 engineering run**

# SUMMARY

## MimoSTAR IV Chip: design almost finalised

- Sensor design completed and tested at small scale: MIMO★-2
  - ↪ will be operated inside STAR in 2006
- Will be tested on large scale (MIMO★-3) in 2006 (engineering run):
  - ◇ 640 x 320 pixels (30 $\mu m$ pitch) $\mapsto$ 2 x 1 cm$^2$
  - ◇ 2 ms read-out time
  - ◇ thinned to 50 $\mu m$
- Final sensor (MIMO★-4) will be fabricated in Spring 2007
  - ◇ 640 x 640 pixels (30 $\mu m$ pitch) $\mapsto$ 2 x 2 cm$^2$
  - ◇ 4 ms read-out time
  - ◇ thinned to 50 $\mu m$
  - ↪ Ready for mounting end 2007

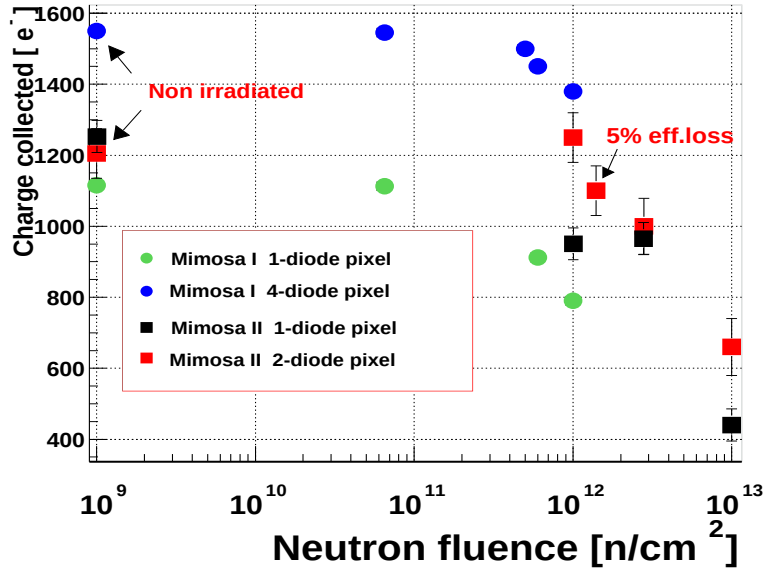
## Ultimate Chip: several $\sim$ satisfactory architecture alternatives under study

- Existing MIMOSA prototypes (M-8, M-9, M-11, M-15) feature already most essential functionnalities
- Next important steps:
  - ◇ MIMO★-3 engineering run
  - ◇ MIMO★-2 operation inside STAR
  - ↪ Design $\sim$ finalised end 2007 $\mapsto$ Final production in Summer 2009

# BACK-UP SLIDES

# Radiation Tolerance: Non-Ionising Radiation

- Neutrons of O(1 MeV) at JINR (Dubna):
  irradiation of up to $10^{13}$ $n_{eq}/cm^2$
- Tests with 2 sensors (T = + 10°C)
  from different fabrication processes:
  - ◇ AMS-0.6 ($\lesssim$ 14 $\mu m$ epitaxy)
  - ◇ AMI-0.35 ($\sim$ 4 $\mu m$ epitaxy)
    - ↪ charge loss for $\lesssim 10^{12}$ $n_{eq}/cm^2$
      & modest increase of $I_{leak}$ & noise ($\lesssim$ 10 %)




- AMS-0.35 OPTO ($\sim$ 11 $\mu m$ epitaxy)
  ↪ S/N (MPV) vs fluence and T:

  ↦ fluences of $\gtrsim 10^{12}$ $n_{eq}/cm^2$ affordable,
  better performances with T $<$ 0°C
  ($\epsilon_{det}$ $\gtrsim$ 99.5 $\pm$ 0.1 %)

| Fluence | T = -20°C | T = 0°C |
|---|---|---|
| 0 | 28.4 $\pm$ 0.2 | 26.3 $\pm$ 0.2 |
| $10^{11}$ $n_{eq}/cm^2$ | 25.3 $\pm$ 0.2 | 24.5 $\pm$ 0.4 |
| $10^{12}$ $n_{eq}/cm^2$ | 18.7 $\pm$ 0.2 | – |

▷▷▷ Results show that fluences $>>$ $1 \cdot 10^{12}$ $n_{eq}/cm^2$ can be accomodated

- **Reduce mean free path of signal $e^-$ :**
  - ⁜ Reduce pixel pitch (optimise w.r.t. r.o. speed)
  - ⁜ Pixel architecture with improved charge collection: MIMOSA-15
    - ↪ irradiations with 1 MeV neutrons under way at Dubna
  - ⁜ Optimise operation temperature
  - ⁜ Investigate annealing possibilities

- **Improve S/N performance :**
  - ⁜ Optimise pixel and r.o. architecture
  - ⁜ Investigate thick epitaxy techno. $\mapsto$ AMS 0.35 OPTO offers "20 $\mu m$" epitaxy option (multi-project ?)
  - ⁜ Optimise cluster reconstruction algorithms

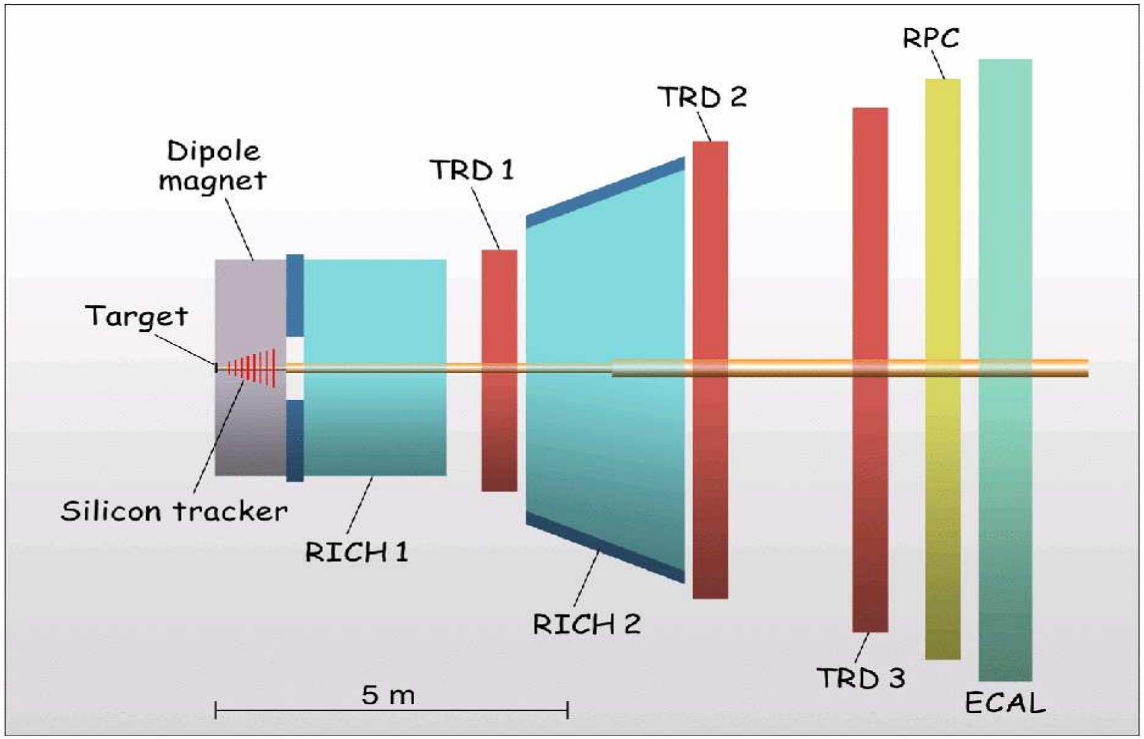
- **Equip each detector layer with 2 layers of sensors**
  - ↪ ○ 90 % detection efficiency per layer allows 99 % overall detection efficiency
  - ○ double layer $\mapsto$ track mini-segments from loosely selected clusters $\mapsto$ improved detection efficiency
  - ⁜ Thinning sensors to ultimate thickness ($\sim$ 30 $\mu m$) is particularly valuable
  - ⁜ Design mechanical support allowing double sensor layer per detector layer

# APPLICATIONS TO OTHER VERTEX DETECTORS

# Application to CBM Vertex Detector ($<$ 2015 ?)

- **Cold Baryonic Matter (fixed target) experiment at FAIR/GSI:**

  **Open charm production in heavy ion collisions as a probe for quark-gluon plasma formation (similar physics issue as for STAR)**




- **2 or 3 planes of pixels for D meson decay vertex reconstruction (1000 - 2000 cm$^2$)**

  $\therefore$ **single pt resolution** $\lesssim$ **5** $\mu m$

  $\therefore$ **sensor thickness** $\lesssim$ **50** $\mu m$

  $\therefore \sim$ **10$^{13}$n$_{eq}$/cm$^2$/yr** $\mapsto$ **10$^{15}$n$_{eq}$/cm$^2$/yr !!!!!**

  $\therefore \sim$ **1-10 MRad/yr !!!!**

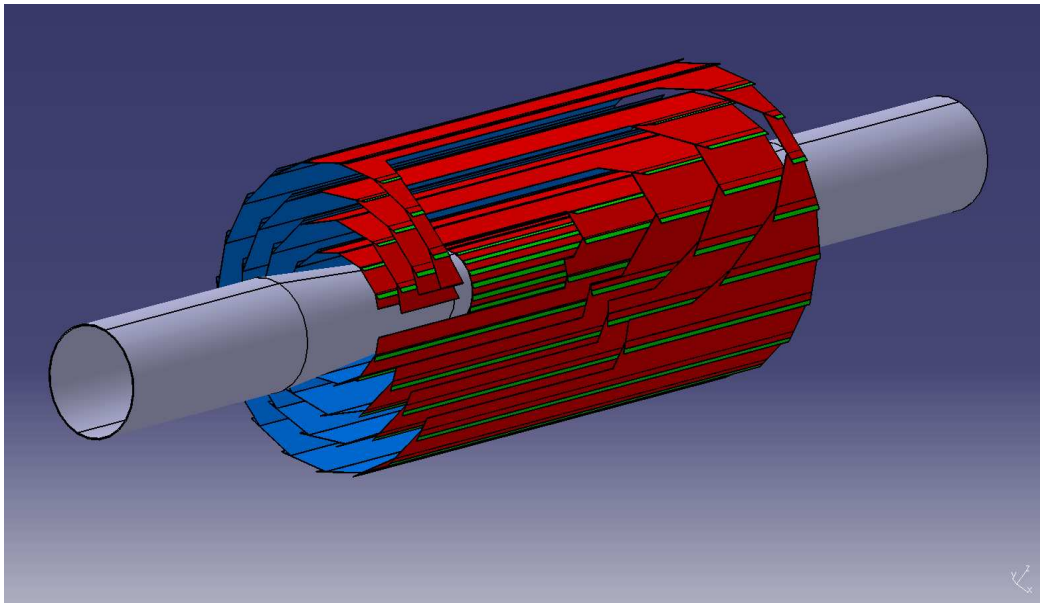
  $\therefore \lesssim$ **10$^{10}$ particles / s** $\mapsto$ **read-out time** $\lesssim$ **10** $\mu s$ **!!!!!**

$\hookrightarrow$ **Intense R&D effort on FAST and RADIATION HARD CMOS sensors**

# Application to the ILC Vertex Detector

- Geometry: 5 cylindrical layers (R=15 – 60 mm), $||cos\theta|| \leq$ 0.90 – 0.96
- $\sigma_{\mathbf{IP}} = \mathbf{a} \oplus \mathbf{b/p} \cdot \mathbf{sin^{3/2}}\theta$, with a $<$ 5 $\mu m$ and b $<$ 10 $\mu m$
- Read-out time: ¶ 25 $\mu s$ in L0 ¶ 50 $\mu s$ in L1 $\therefore$ $\lesssim$ 200 $\mu s$ in L2, L3, L4

| Layer | Radius (mm) | Pitch ($\mu m$) | $t_{r.o.}$ ($\mu s$) | $N_{lad}$ | $N_{pix}$ ($10^6$) | $P^{inst}_{diss}$ (W) | $P^{mean}_{diss}$ (W) |
|---|---|---|---|---|---|---|---|
| L0 | 15 | 20 | 25 | 20 | 25 | $<$100 | $<$5 |
| L1 | 25 | 25 | 50 | 26 | 65 | $<$130 | $<$7 |
| L2 | 37 | 30 | $<$200 | 24 | 75 | $<$100 | $<$5 |
| L3 | 48 | 35 | $<$200 | 32 | 70 | $<$110 | $<$6 |
| L4 | 60 | 40 | $<$200 | 40 | 70 | $<$125 | $<$6 |
| Total | | | | 142 | 305 | $<$565 | $<$29 |



- Ultra thin layers: $\sim$ 0.1 % $X_0$/layer (?)
- Very low $P^{mean}_{diss}$: $<<$ 100 W ($\mapsto$ minimise cooling)
- Rad. tolerance (3 yrs): $\lesssim$ 3·$10^{10}$ $n_{eq}$/cm$^2$ – $\lesssim$ 6·$10^{12}$ $e_{10MeV}$/cm$^2$ (150 kRad, 2·$10^{11}$ $n_{eq}$/cm$^2$)

# Application to ILC: Various FE Architectures

▷ **Fast col. // architecture (like MIMOSA-8), allowing to process signal (CDS, ADC, sparsification) during BX:**

↪ **complex, close to technology limits ↦ much design & test effort needed (but quite universal output)**

▶ **Alternative ↦ 2 phase $\mu$circuit architecture exploiting beam time structure, reducing data flux:**

**1) charge stored (eventually sampled) inside pixel during train crossing: O(1) ms**

**2) signal transfered and processed inbetween trains: O(100) ms**

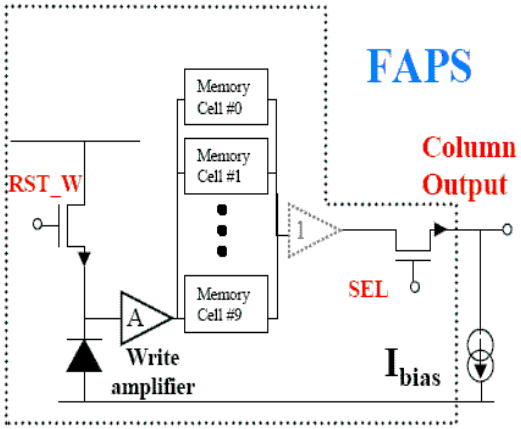
▶ **Different strategies of storage during train crossings:**

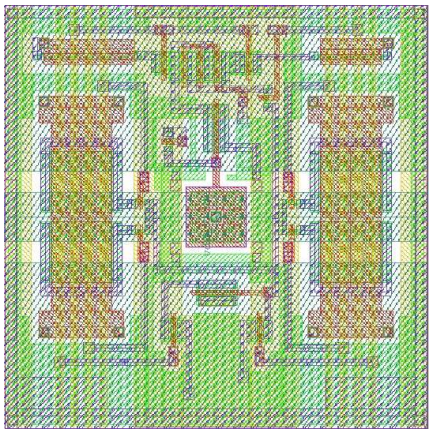
$\therefore$ **20 – 25 $\mu m$ large pixels with $\gtrsim$ 20 capacitors**

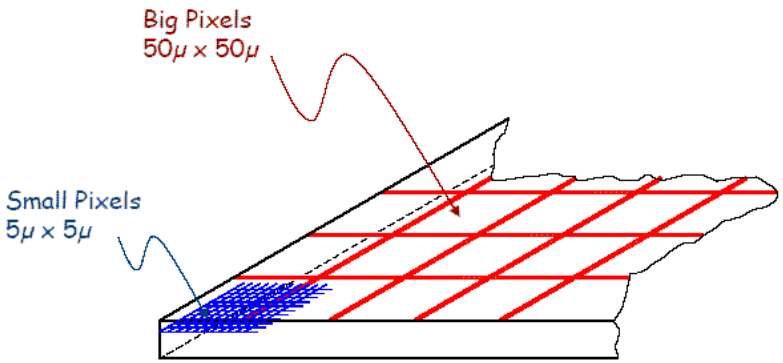
↪ **$\lesssim$ 50 $\mu s$ long snapshots/capacitor**

$\therefore$ **$\lesssim$ 5 $\mu m$ large pixels with 1 capa.(hit position)**

**and 50 $\mu m$ large pixels for hit zone selection**






▷ **Difficulty: are small capacitors precise enough ?**

▷ **Difficulty: can cluster size be $\lesssim$ 3 pixels ?**

# Application to BELLE Vx Detector Upgrade ($\sim$ 2008)

- **Improve vertex detector performance (strips $\mapsto$ pixels)**
  - $\therefore$ **to accommodate luminosity increase: $\sim$ 1.5·10$^{34}$ $\mapsto\sim$ 5·10$^{35}$ cm$^{-2}$·s$^{-1}$**
  - $\therefore$ **to improve impact parameter resolution**

  $\hookrightarrow$ **Equip inner most layer with single or double layer of pixels:**

  **R $\sim$ 8 mm $\mapsto$ surface $\sim$ 100 – 200 cm$^2$**

- **Major Difficulty: Beam background $\sim$ O(10) MRad/yr & Operation at room temperature**

  $\hookrightarrow$ **Short integration time mandatory**

- **Signal of interest selected by external trigger ($\sim$ 10 kHz)**

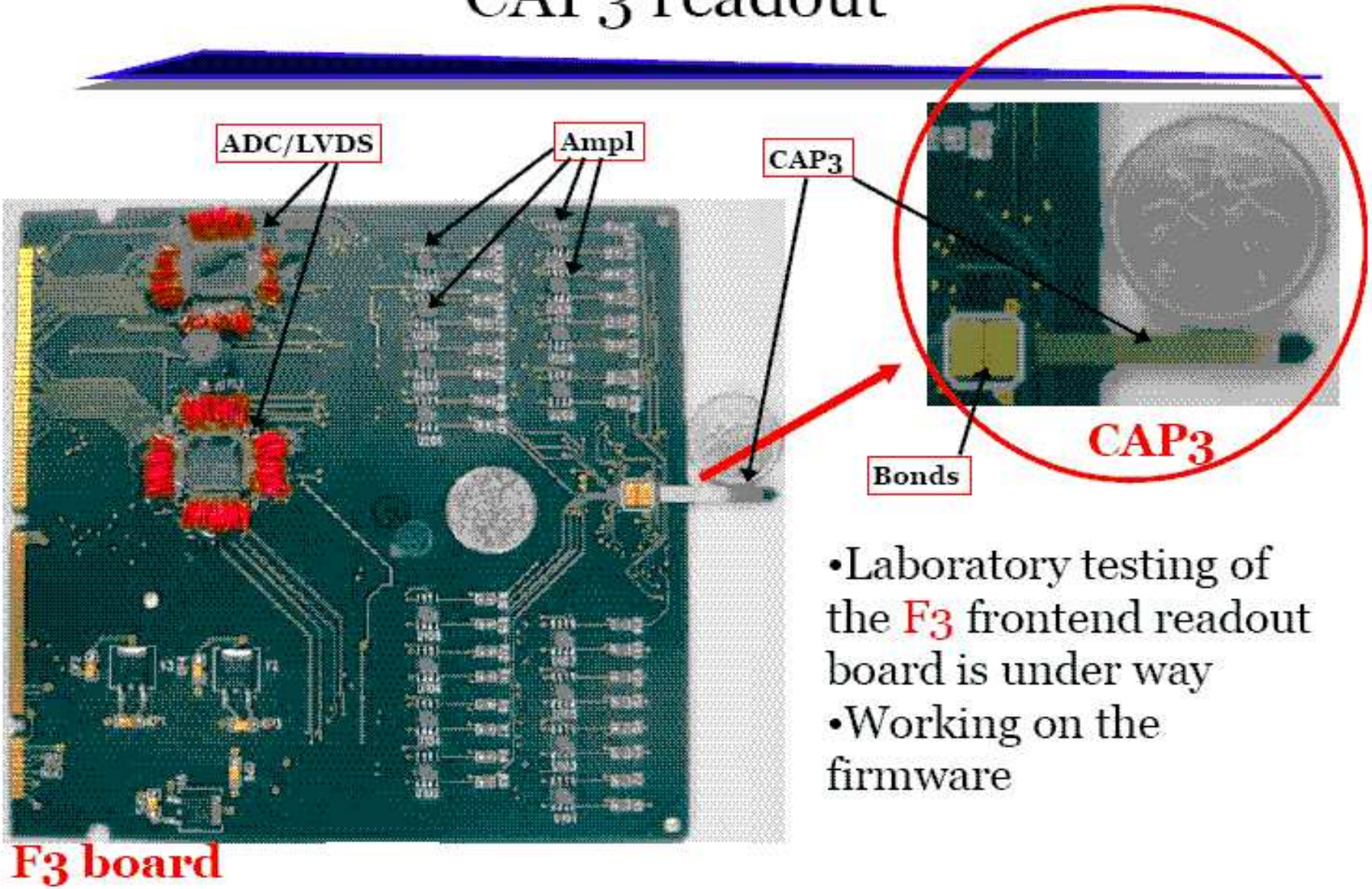
- **Chip architecture with charge sensing decoupled from read-out:**

  $\hookrightarrow$ **5 pairs of memory cells inside each pixel, each cell sampling the charge integrated over 10$\mu s$**

- **Already three prototypes designed: CAP-1 and -2 tested $\mapsto$ CAP-3 (mature prototype) being tested**

# CAP-3: Prototype for (Super)BELLE

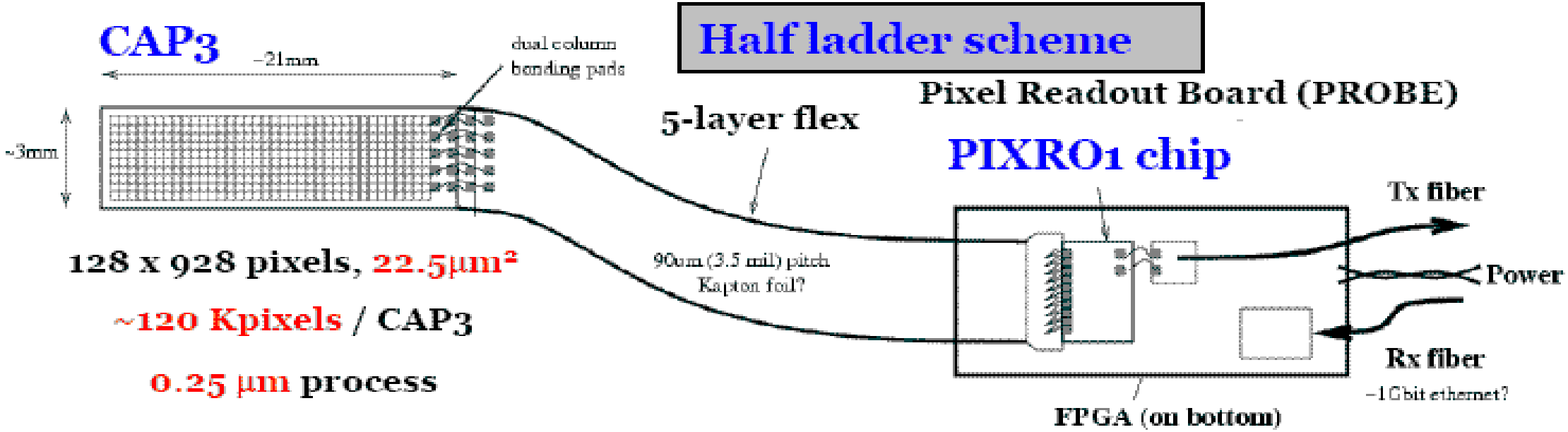
## CAP3 readout




- Laboratory testing of the F3 frontend readout board is under way
- Working on the firmware

# Integration of CAP in (Super)BELLE

## Half ladder scheme

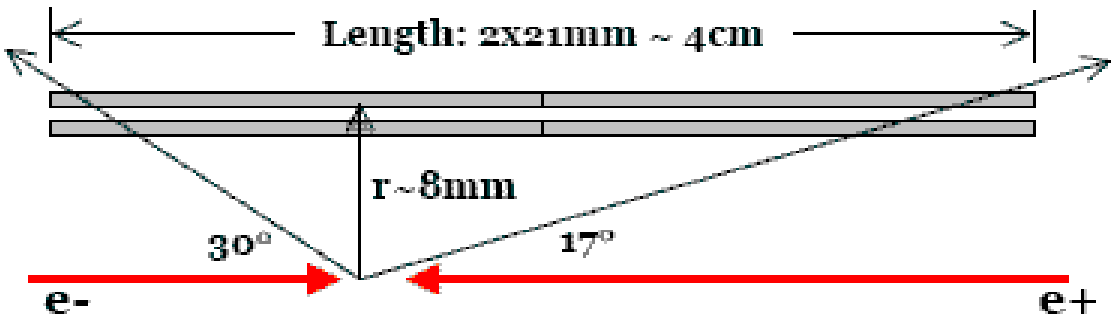



128 x 928 pixels, 22.5μm²

~120 Kpixels / CAP3

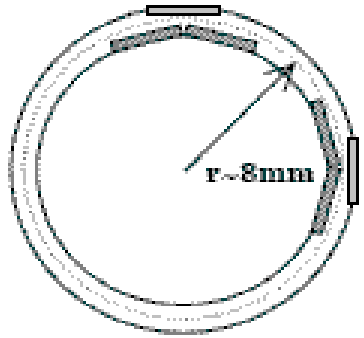
0.25 μm process

## Side view




## End view

Double layer, offset structure




# of Detector / layer ~ 32