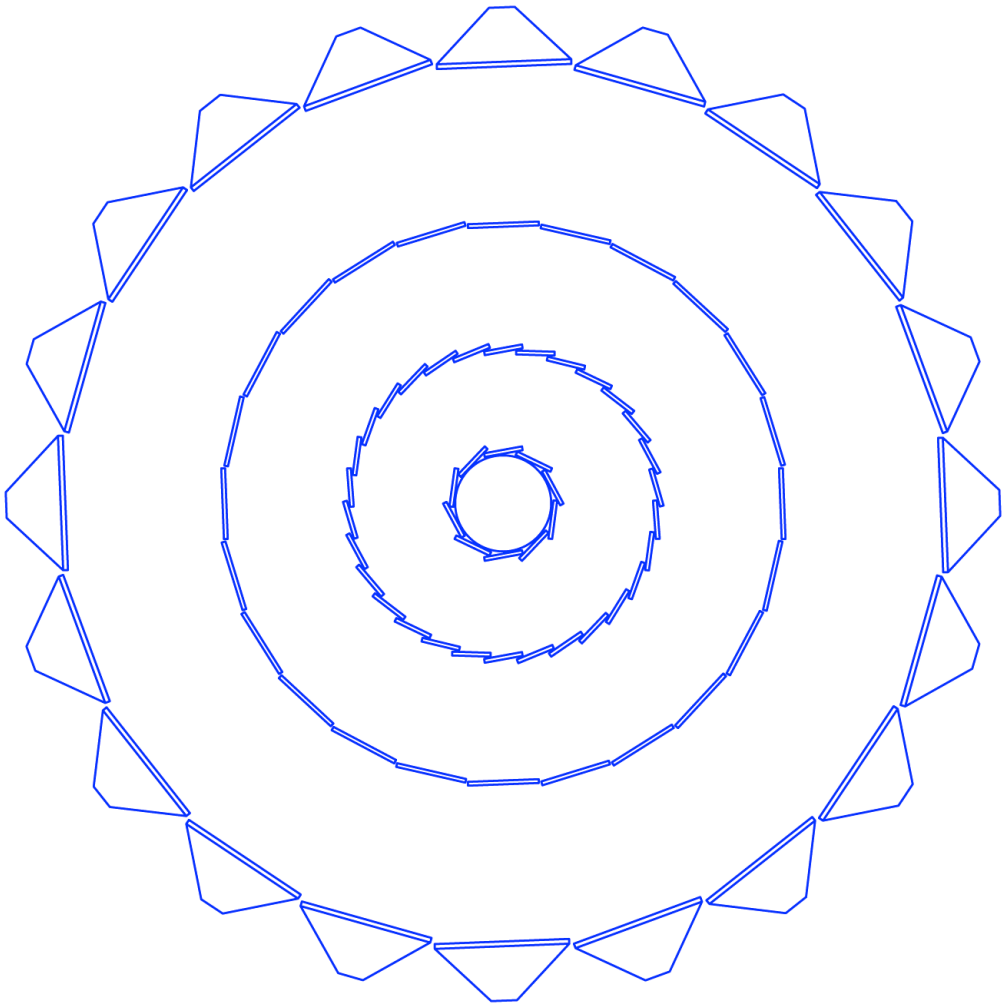
The STAR Heavy Flavor Tracker

Technical Design Report



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1. Introduction

The Heavy Flavor Tracker (HFT) is a state-of-the-art micro-vertex detector utilizing active pixel sensors and silicon strip technology. The HFT will significantly extend the physics reach of the STAR experiment for precision measurements of the yields and spectra of particles containing heavy quarks. This will be accomplished through topological identification of mesons and baryons containing charm quarks, such as D^o and Λ_c, by the reconstruction of their displaced decay vertices with a precision of approximately 30 μm in p+p, d+A, and A+A collisions. The combined measurements of directly identified charm hadrons and of the total non-photonic electrons will enable the measurement of bottom production at RHIC, including the bottom production cross section, the nuclear modification factor and the collectivity of the decay electrons.

The HFT consists of 4 layers of silicon detectors grouped into three subsystems with different technologies, guaranteeing increasing resolution when tracking from the TPC towards the vertex of the collision. The Silicon Strip Detector (SSD) is an existing detector in double-sided strip technology. It forms the outermost layer of the HFT. The Intermediate Silicon Tracker (IST), consisting of a layer of single-sided strip-pixel detectors, is located inside the SSD. Two layers of silicon pixel detector (PXL) are inside the IST. The pixel detectors have the resolution necessary for a precision measurement of the displaced vertex. With the HFT, the Time-of-Flight detector, the TPC, and the Barrel Electromagnetic Calorimeter STAR will study the physics of mid-rapidity charm and bottom production.

The pixel detector will use CMOS Active Pixel Sensors (APS), an innovative technology never used before in a collider experiment. The APS sensors are 50 μm thick with the first layer at a distance of only 2.5 cm from the interaction point. This opens up a new realm of possibilities for physics measurements. In particular, a thin detector (0.37% of a radiation length per layer) in STAR makes it possible to do the direct topological reconstruction of open charm hadrons down to very low transverse momentum by the identification of the charged daughters of the hadronic decay.

2. Physics Motivation

Heavy quark measurements are a key component of the heavy ion program at RHIC as it moves from the discovery phase to the systematic characterization of the dense medium created in heavy ion collisions. The primary motivation for the HFT is to extend STAR's capability to study heavy flavor production in p+p, p+A, and A+A collisions by the measurement of displaced vertices and the direct topological identification of open charm hadrons. The yield and distribution of bottom hadrons will be estimated from charm production and non-photonic electron measurements and also via the impact parameter reconstruction of their decay electrons. The primary physics topics to be addressed by the HFT include heavy flavor energy loss, flow, and a test of partonic thermalization at RHIC. These measurements have been identified as necessary goals for the RHIC program in the Nuclear Physics Long Range Plan and in the RHIC mid-term scientific plan.

From a precise measurement of the spectra and the production ratios of the majority of charm hadron states, we will be able to extrapolate to the total yield for charm quark production. Furthermore, the open charm production rate is high enough at RHIC that the coalescence process becomes relevant for charmonium production. Knowledge of the total production cross-section for charm quarks is also essential as a baseline for J/ψ measurements.

In the following we will briefly review the status of HFT simulations with respect to key measurements that STAR will be able to perform in the first three years of HFT operation.

2.1. Charm Flow

At RHIC partonic collectivity has been well established via the measurements of hadrons containing light quarks (u, d, and s). Recent v_2 results from multi-strange hadrons, ϕ mesons and Ω baryons, further confirm this important discovery.[1] Charm quarks are abundantly produced at RHIC energies. Due to their large mass and small interaction cross-section, the strength of elliptic flow of heavy flavor hadrons may be a good indicator of thermalization occurring at the partonic level. All quarks in heavy flavor hadrons flowing with the same pattern as the quarks in the light flavor hadrons, would indicate frequent interactions between all quarks. Thus, thermalization of light quarks is likely to have been reached through partonic re-scattering.

Since flow is a hydrodynamic phenomenon, the low p_T region is most relevant for studies of collectivity. Generally, data and hydro predictions agree up to about 1.5 GeV/c p_T, beyond which point data deviate from the hydro prediction. In Figure 1 we present the precision of a v_2 measurement for D^0 that can be achieved **within the first year** of Au+Au data taking with the HFT by analyzing 500 million minimum-bias events. The red and green lines represent the results from model calculations[2] based on a coalescence assumption.[3] The red line assumes that charm quarks have the same flow strength as the light quarks, whereas the green line assumes that charm quarks do not flow. The error bars of the data points on the red and green lines represent the statistical errors the HFT measurement will have, assuming that the production follows either line. The blue (dotted) line shows the low p_T hydro prediction for the D^0 mass[4] and the purple line represents the charged hadron v_2 measured by STAR.[5]

Figure 1 clearly shows that the HFT will make a significant measurement that can determine from the low p_T end of the distribution, if charm quarks flow or not. It also clearly shows that the simple coalescence model from Reference [2] is not a good description of the data at high p_T. The model values saturate at high p_T, whereas the data decrease after 3 GeV/c. The model has no

predictive power at high p_T since it only assumes coalescence and does not include other effects, like parton energy loss. The model uses light quark momentum distributions and for the heavy quark either non-interacting distributions (no flow) or completely thermalized distributions with transverse expansion (flow). There is no realistic model on the market that would give quantitative guidance for v_2 values at low p_T and realistic predictions for v_2 at high p_T simultaneously,

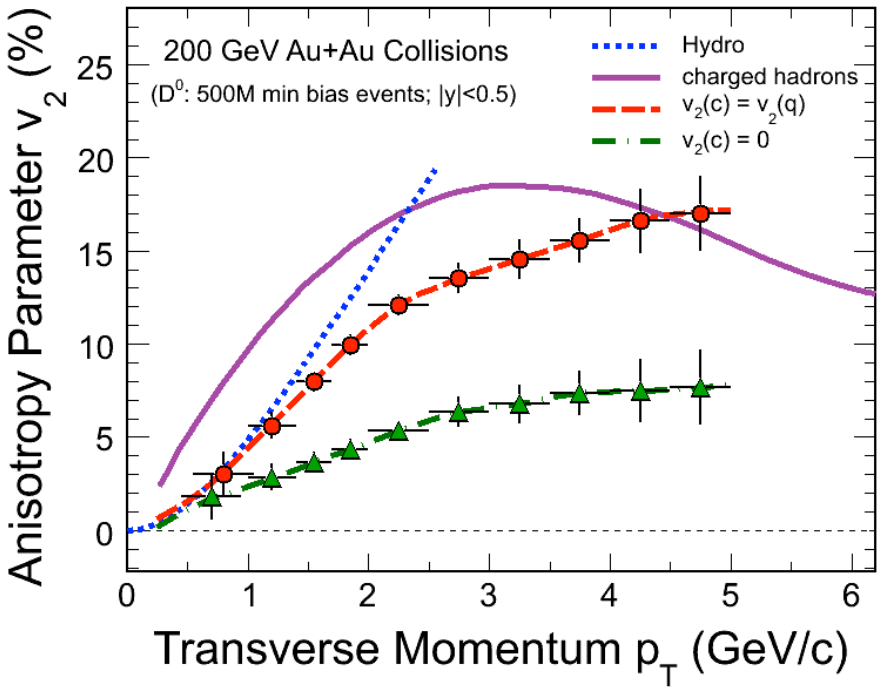

Figure 1: Elliptic flow (v_2) as a function of p_T in Au+Au collisions at 200 GeV. The red and the green curves show calculations from Ref. [2] for the limiting cases that the charm quark flows like the light quarks and that the charm quark does not flow in a coalescence model. The error bars of the data points represent the statistical errors the HFT measurements will achieve. The purple curve shows the measured v_2 value for charged hadrons.

It is also important to note that a measurement of v_2 of the non-photonic electrons from the semi-leptonic decay of charm hadrons cannot make a decisive contribution to the problem of thermalization. From kinematics we know that the parent p_T is not known to better than 3 GeV/c if only the electron p_T is measured. As argued above, only a measurement at low p_T (<2.5 GeV/c) will be able to settle this important question.

2.2. Heavy Quark Energy Loss

The discovery of a factor of 5 suppression of high p_T hadrons ($5 < p_T < 10$ GeV/c) produced in central Au+Au collisions at RHIC and the disappearance of the away-side jet has been interpreted as evidence for jet quenching.[6,7] This effect was predicted to occur due to radiative energy loss of high energy partons that propagate through a dense and strongly interacting medium.[8] The energy loss of heavy quarks is predicted to be significantly less compared to light quarks because of a suppression of gluon radiation at angles $\Theta < M_Q/E$, where M_Q is the heavy quark mass and E is the heavy quark energy. This kinematic effect is known as the "dead cone" effect.[9] However,

a recent measurement of the nuclear modification factor,[10] R_{AA}, for non-photonic electrons, the products of charm and bottom hadron decay, yielded the surprising result that heavy quarks may also be strongly suppressed in the medium. This clearly indicates that the energy loss mechanism is not yet understood. This fact has triggered new theoretical developments.[11,12] In order to make progress in understanding the nature of the energy loss mechanism, it is important to measure R_{AA} or R_{CP} for topologically reconstructed D mesons.

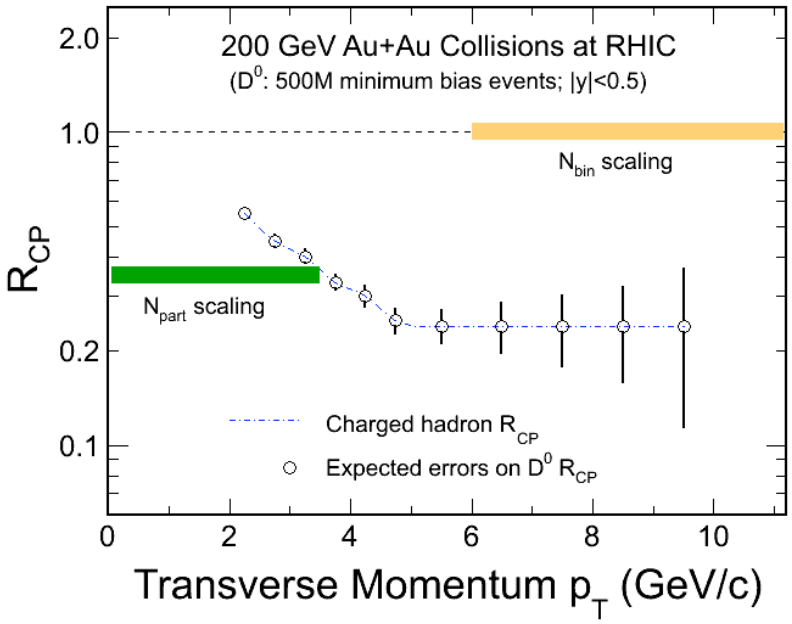

Figure 2: Expected errors for the R_{CP} measurement as a function of p_T.

Figure 2 shows the precision for R_{CP} that can be achieved with 500 M minimum-bias events in STAR with the HFT under the assumption that the suppression for heavy quarks is of the same size as the suppression for the light quarks. With the HFT STAR will be able to perform a precision measurement of R_{CP} of D mesons.

2.3. Λ_C-Baryons

In central Au+Au collisions at RHIC, a baryon to meson enhancement has been observed in the intermediate p_T region ($2 < p_T < 6$ GeV/c).[13,14] This is explained by a hadronization mechanism involving collective multi-parton coalescence rather than independent vacuum fragmentation.[3] The success of the coalescence approach implies deconfinement and the development of collectivity of the light quarks prior to hadronization. A similar pattern of baryon to meson enhancement is expected in the charm sector.[15] The Λ_C/D^0 ratio is the most promising candidate for such an observation. The Λ_c is the lightest charmed baryon and its mass is not far from that of the D^0 meson. Λ_C/D^0 enhancement is also believed to be a signature of a strongly coupled quark-gluon plasma.[16]

Figure 3 shows the expected statistical errors of the ratio of Λ_C to D^0 production for different assumptions about the production mechanism as a function of p_T. The discrimination should be made between estimated errors and the two scenarios of Λ_C /D^0 ratio, not between the two sets of estimated errors. The significance of this discrimination is in the range of 2 to 4 sigma in the case

of an enhanced ratio and about 4 to 6 sigma in the extreme case of no-enhancement. The error bars shown in Figure 3 can be achieved with a total statistics of 250 M central events and 2000 M minimum bias events. This will require 3 years of Au+Au running at 200 GeV.

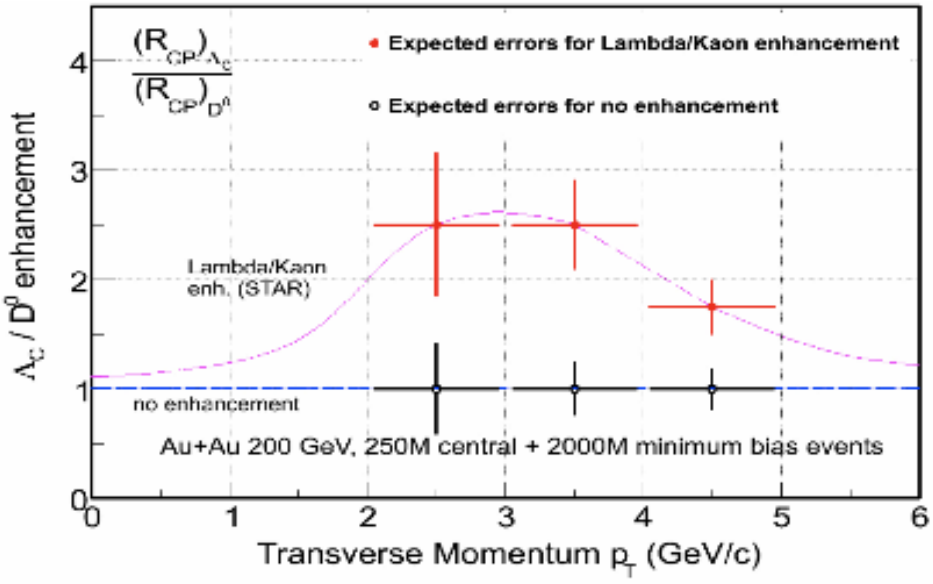

Figure 3: Expected statistical errors of the ratio of Λ_C to D^0 production for different assumptions about the production mechanism.

A Λ_c/D^0 enhancement could be an explanation[17] for the observation of the unexpectedly large suppression of high-p_T electrons from semi-leptonic charm and bottom decays.[18] The branching ratio of charm baryons and mesons into semi-leptonic decays is quite different. An enhanced baryon production will lead to apparent electron suppression. This again points out the necessity to topologically reconstruct charm hadrons and the limitations of the measurement of non-photonic electrons.

2.4. B-Mesons

B mesons can be identified with the methods developed for D mesons. At RHIC energies the dominant problem is the fact that the production rates are low. On the other hand, B mesons contribute to all measurements that are not based on topological reconstruction. In particular, the spectrum of non-photonic electrons is expected to have a substantial contribution from B decay. In fact, at transverse momenta above about 4 to 6 GeV/c of the decay electrons B decays are expected to dominate. Current measurements using non-photonic electrons as a measure of the abundance of charm and bottom hadrons indicate that the energy loss for heavy quarks is unexpectedly high and inconsistent with our current understanding of pQCD models. Based on the non-photonic electron data the theory of heavy quark energy loss is uncertain and may be completely wrong, especially with regards to bottom. The ability to separate and identify charm and bottom contributions is of crucial importance for such measurements.

The contributions from D and B decays can be determined through an unfolding procedure due to the fact that D and B mesons have different life times. Since the individual D states have greatly different life times, their relative abundance also needs to be known. However, if in heavy ion reactions the abundances are modified, precision unfolding becomes impossible.

Figure 4 shows the estimated precision for a measurement of R_{CP} of electrons from D (red) and B (blue) decay separately as a function of p_T, where we assume the respective R_{CP} (dotted curves) from a theoretical calculation of the T-matrix approach to heavy quark diffusion in the QGP.[19] For low p_T, R_{CP} and the expected errors are calculated from 500M Au+Au minimum bias events (open symbols). For high p_T a "high tower" trigger sampling 500 μb^{-1} luminosity (filled symbols) is used.

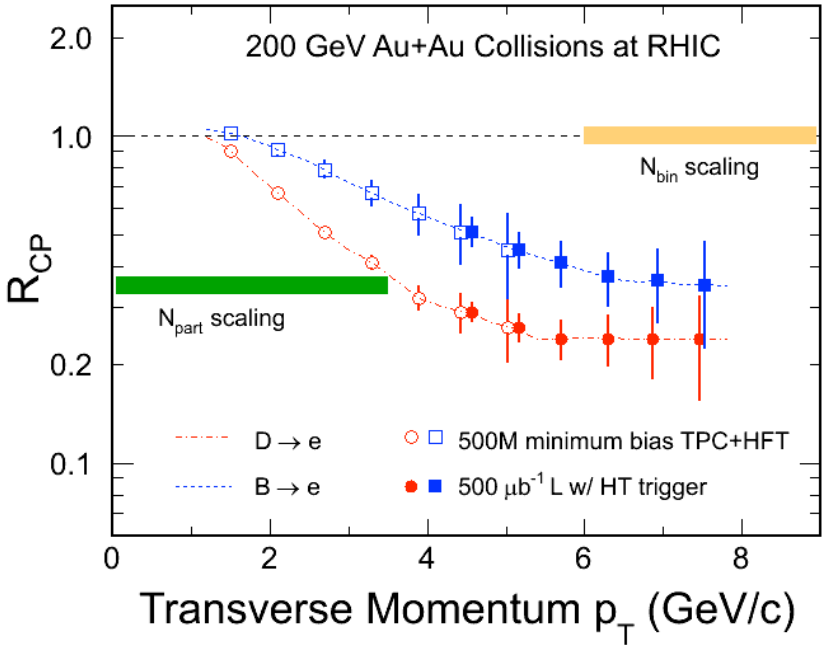

Figure 4: Nuclear modification factor R_{CP} of electrons from D meson and B meson decays. Expected errors are estimated for 500 M Au+Au minimum-bias events (open symbols) and 500 μb^{-1} sampled luminosity with a "high tower" trigger (filled symbols).

3. Technical Design

3.1. Requirements and Detector Design

The HFT will extend the STAR physics capabilities to the identification of short-lived particles containing heavy quarks through reconstruction and identification of the displaced vertex at mid-rapidity. STAR has 2π azimuthal coverage and to match this, the HFT is required to have 2π azimuthal coverage.

In order to identify short displaced vertices the HFT is required to have excellent pointing resolution of the order of 50 μm. A two-layer high-resolution vertex detector placed close to the interaction vertex can achieve good pointing resolution. In the high-multiplicity environment of heavy ion collisions, the HFT also needs to provide excellent tracking resolution in order to connect tracks identified in the TPC with the corresponding hits in the vertex detector. The resolution of the TPC is not good enough to assign hits in the vertex detector to identified particles with high efficiency. Thus the HFT needs to provide intermediate tracking in the region between the TPC and the vertex detector. We also require redundancy in the design.

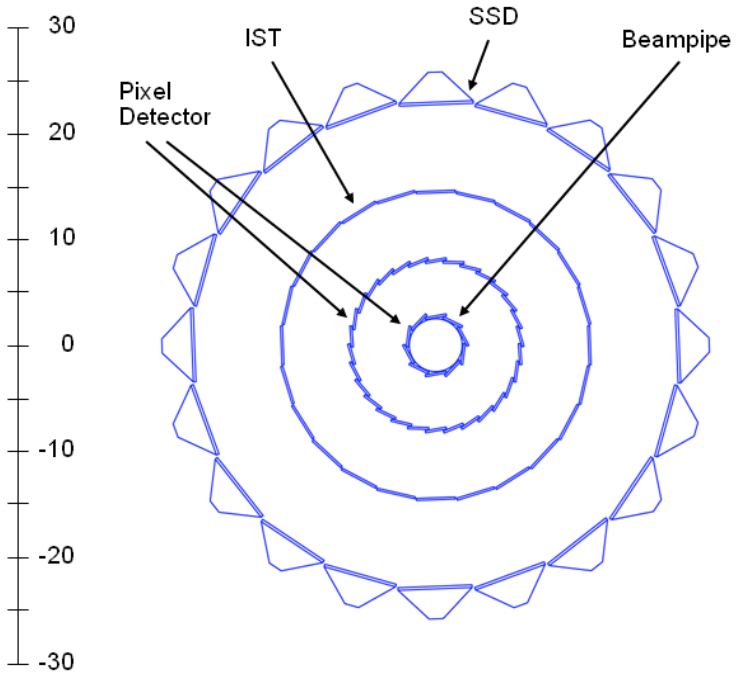

Figure 5: A schematic view of the Si detectors that surround the beam pipe. The SSD is an existing detector and it is the outmost detector shown in the diagram. The IST lies inside the SSD and the PXL lies closest to the beam pipe.

These requirements lead to the HFT design of 4 layers of silicon detectors distributed in radius between the interaction point and the TPC. Figure 5 shows the radial distribution of the four layers. The inner two layers, the PXL, lay at 2.5 and 8 cm, the IST lays at 14 cm and the SSD at 22 cm. A schematic view of the different HFT layers between the beam pipe and the inner field cage of the TPC is shown in Figure 6.

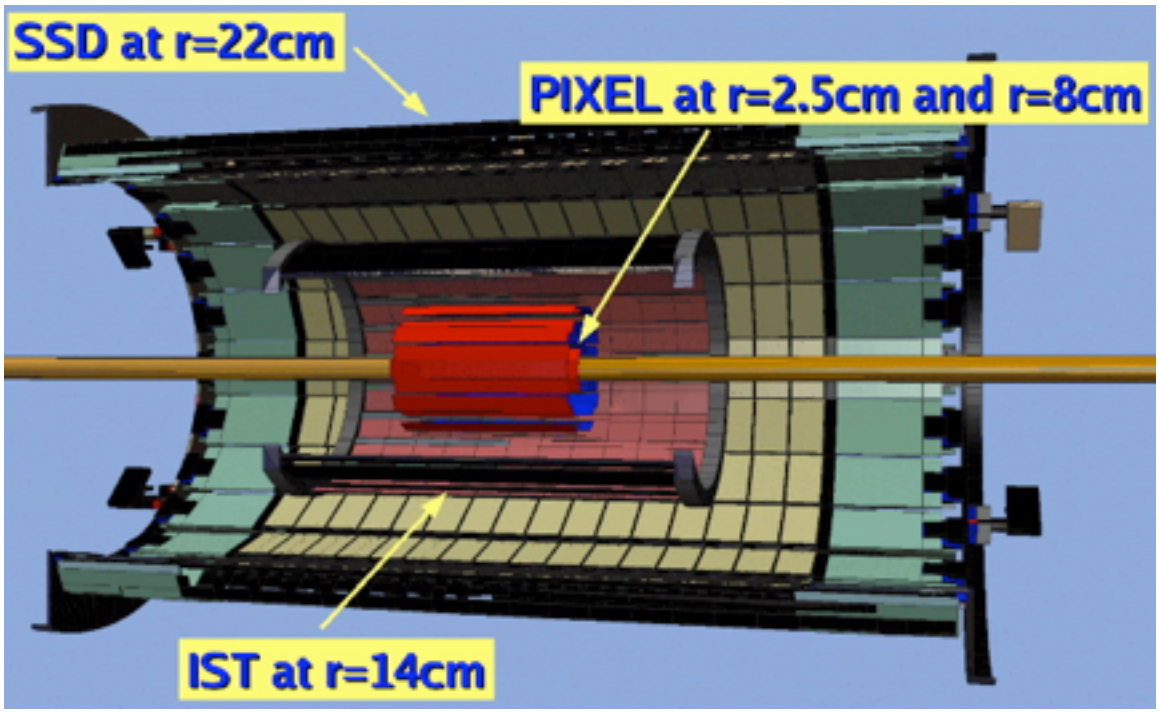

Figure 6: Schematic view of the different layers of the HFT.

The pointing resolution that can be achieved with a given system has two components, a contribution from detector resolution and a contribution from the effects of multiple scattering. Using low radiation length material, in particular between the interaction point and the second layer of the detector, can minimize multiple scattering. The HFT requirements are that the PXL and the beam pipe be as thin as technically possible and that the first detector layer be as close to the interaction point as technically feasible.

In order to meet those requirements, STAR needs a new beryllium beam pipe with a radius of 2 cm. The integrated radiation length from the interaction point to the outside of the PXL detector is smaller than 1 % of a radiation length.

Graded Resolution from the Outside - In		Resolution (σ)
TPC pointing at the SSD	(22 cm radius)	~ 1 mm
SSD pointing at IST	(14 cm radius)	~ 400 μm
IST pointing at PXL-2	(8 cm radius)	~ 400 μm
PXL-2 pointing at PXL-1	(2.5 cm radius)	~ 125 μm
PXL-1 pointing at the vertex		~ 40 μm

Table 1: Pointing resolution of the TPC and HFT detectors at intermediate points along the path of a 750 MeV kaon as it is tracked from the outside – in.

Table 1 gives an overview of the pointing resolution at intermediate points along the path of a 750 MeV kaon as it is traced back from the TPC to the vertex. Good resolution at the intermediate points is necessary to resolve ambiguous hits on the next layer of the tracking system with high efficiency.

Good pointing resolution can overall only be achieved if the individual detectors guarantee a long-term mechanical stability and reproducibility that is of the order of the resolution of the detector. The numbers used to guide the baseline design are:

- PXL 20 μm
- IST 300 μm
- SSD 300 μm

An important requirement is that the HFT be able to be read out with a frequency that is compatible with STAR DAQ, i.e. 1000 Hz. All sub-detectors are read out individually and their readout needs to fulfill this condition. The IST and the SSD are fast detectors and achieving this readout speed with appropriate electronics is trivial. The sensors of the PXL detector on the other hand have a slow readout time of the order of 100 μs. The individual pixels are always live and the sensors keep a memory of all tracks that pass through them during one readout cycle. This leads to pile-up of tracks that do not belong to the triggered event. Pile-up is unavoidable in this technique. With extensive simulations of the SSD, IST, and PXL detectors, we have shown that even at RHIC II luminosities the effects of pile-up are minimal if the readout time of the PXL sensors is smaller than 200 μs. This leads to the requirement that the readout time of the PXL sensors should be 200 μs or smaller.

The HFT needs to operate under RHIC II conditions and luminosities. The outer layers (IST and SSD) are required to operate for 10 years in this radiation field without degradation of performance in terms of efficiency. The PXL layers of the HFT are retractable and can be replaced in case of damage. The PXL layers need to operate for one year under the highest RHIC II luminosities without appreciable deterioration of the detection efficiency.

Calibration of a micro-vertex detector is very elaborate and time-consuming. The concept of replacing a detector within the short time span required for the HFT can only work, if the new detector is calibrated internally on the bench and if this calibration can be transferred to the inserted detector. This is a very important requirement for the PXL sub-detector.

The first layer of the HFT lies very close to the interaction vertex in a very high radiation field. We require that the innermost sensors can operate during an entire RHIC year at the highest RHIC II luminosities without a noticeable drop in efficiency. The location close to the beam is also prone to potentially catastrophic failure of the silicon in case of unintended and uncontrolled excursions of the beam from its nominal orbit. For the case of catastrophic failure or diminished efficiency due to high radiation, we want to be able to replace the PXL detector with a new, fully functioning copy of the detector and so it is a requirement that the PXL detector can be exchanged within one working day.

It is very important to understand the radiation environment the HFT will encounter. We have performed measurements of the radiation in the center of STAR that is generated from collisions and from background and the process of ramping the machine. The expected radiation dose in krad is given for the different detector radii for a 12 week run of Au+au at 200 GeV and for p+p at 500 GeV in Table 2. For the different radii we quote the radiation dose that is generated from collisions (Physics) and the total estimated rate. For the innermost radius, we also specify the dose expected from collisions and from production by colliding electromagnetic fields (UPC). The physics rate is calculated from interaction rates and cross sections. The estimated maximum doses are consistent with measurements performed by PHENIX in 2006.[20]

	Radius [cm]	200 GeV	200 GeV	500 GeV	500 GeV
		Au+Au Max	Au+Au Min	p+p Max	p+p Min
Physics	2.5	28	5.3	133	29
Physics+UPC	2.5	60	11	---	--
Total	**2.5**	**88**	**17**	**267**	**58**
Physics	14	1	0.2	4	1
Total	**14**	**2**	**0.3**	**9**	**2**
Physics	22	0.4	0.1	2	0.4
Total	**22**	**1**	**0.1**	**3**	**1**

Table 2: Radiation field in krad in the center of STAR extrapolated to RHIC II luminosities for different radial positions for 12 weeks of run time for the radii of PXL layer 1, the IST, and the SSD.

3.2. The Pixel Detector (PXL)

The PXL detector is a low mass detector that will be located very close to the beam pipe. It consists of two layers of silicon pixel detectors, one layer at 2.5 cm average radius and the other at 8.0 cm average radius. The PXL has a total of 40 ladders, 10 in the inner layer and 30 in the outer layer. Each ladder contains a row of 10 monolithic CMOS detector chips and each ladder has an active area of ~19.2 cm × ~1.92 cm. The CMOS chips contain a ~1000 × ~1000 array of 20.7 μm square pixels and will be thinned down to a thickness of 50 μm to minimize multiple coulomb scattering (MCS) in the detector. The effective thickness of each ladder is 0.37% of a radiation length. The relevant performance parameters for the pixel detector are shown in Table 3. Note that this table contains parameters that reflect an optimal performance of the detector. They are different from the CD-4 parameters.

Pointing resolution	(13 ⊕ 22GeV/p·c) μm
Layers	Layer 1 at 2.5 cm radius Layer 2 at 8 cm radius
Pixel size	20.7 μm × 20.7 μm
Hit resolution	10 μm rms
Position stability	6 μm (20 μm envelope)
Radiation thickness per layer	$X/X_0 = 0.37\%$
Number of pixels	~356 M
Integration time (affects pileup)	< 0.2 ms
Radiation tolerance	300 kRad
Rapid installation and replacement to cover radiation damage and other detector failure	Installation and reproducible positioning in less than 24 hours

Table 3: Performance parameters for the PXL detector.

3.2.1. Mechanical Design of the PXL Detector

The mechanical design is driven by the following design goals:

- Minimize multiple coulomb scattering, particularly at the inner layer
- Locate the inner layer as close to the interaction region as possible
- Allow rapid detector replacement
- Provide complete spatial mapping of the PXL from the beginning

The first two goals, multiple coulomb scattering and minimum radius, set the limit on pointing accuracy to the vertex. This defines the efficiency of D and B meson detection.

The third goal, rapid detector replacement, is motivated by the recognition of difficulties encountered in previous experiments with unexpected detector failures. This third goal is also motivated by the need to replace detectors that may be radiation damaged by operating so close to the beam.

The fourth goal, complete spatial mapping, is important to achieve physics results in a timely fashion. The plan is to know, at installation, where each pixel is located with respect to each other to within 20 microns and to maintain the positions while installed in STAR.

An overview of the pixel detector is shown in Figure 7. PXL consists of two concentric barrels of detector ladders, which are 20 cm long. The inner barrel has a radius of 2.5 cm and the outer barrel has an 8 cm radius. The barrels separate into two halves for assembly and removal. In the installed location both barrel halves are supported with their own three-point precision kinematic mounts located at one end. During installation, the support for the detector is provided by the hinge structures mounted on a railed carriage. Cooling is provided by air flowing in from one end between the two barrel surfaces and returning in the opposite direction over the outer barrel surface and along the inner barrel surface next to the beam pipe.

The design of the mechanical components is presented in the following sections. Related structural and cooling analysis is covered in the HFT CDR document.[21]

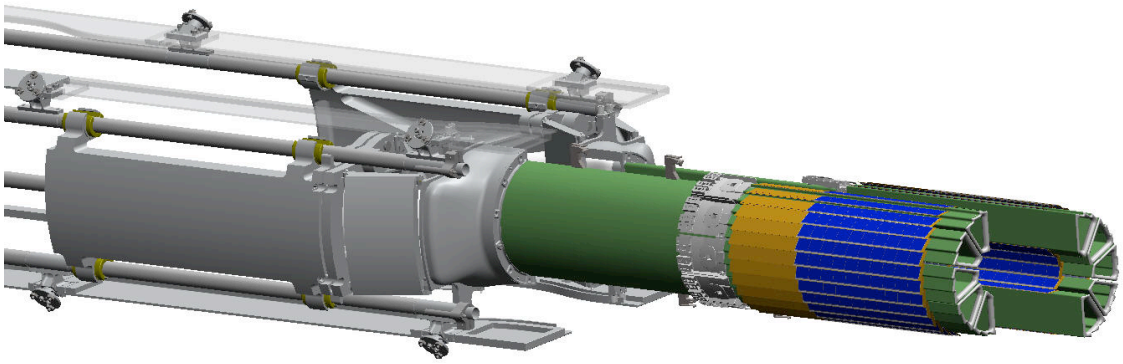

Figure 7: Overview of the PXL detector mechanics showing detector barrel, support structures and insertion parts.

Detector Ladder Design

The mechanical support for the detector chips is arranged in ladders. 10 chips in a row form a ladder. An exploded view of the mechanical components is shown in Figure 8. The thinned silicon chips are bonded to a flex aluminum Kapton cable which is in turn bonded to a thin carbon composite structure. All electrical connections from the chips to the cable are done with a single row of wire bonds along one edge of the ladder. The carbon composite sheet, which is quite thin, will only be of sufficient thickness for handling the chips and for heat conduction. Stiffness and support of the ladder are provided by the support beam. Parts are aligned and held in place with vacuum chuck tooling for bonding. Fifty micron soft, pressure sensitive acrylic adhesive 200MP by 3M is used to make the bonds. A method has been developed[1] which uses a 4 bar pressure vacuum bag and the pressure of an autoclave to remove bond voids and to stabilize the bond. The low elastic modulus of the adhesive is an important component in the design as it greatly reduces bi-metal type deformations stemming from differential expansion caused by thermal changes and humidity changes. This is discussed in more detail in the HFT CDR document.[21]

Mechanical prototypes of the ladder and support structure have been built and tested showing that they meet both structural stability and thermal requirements.

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[1] http://sseos.lbl.gov/hft/hardware/docs/film_adhesive_progress_report.pdf

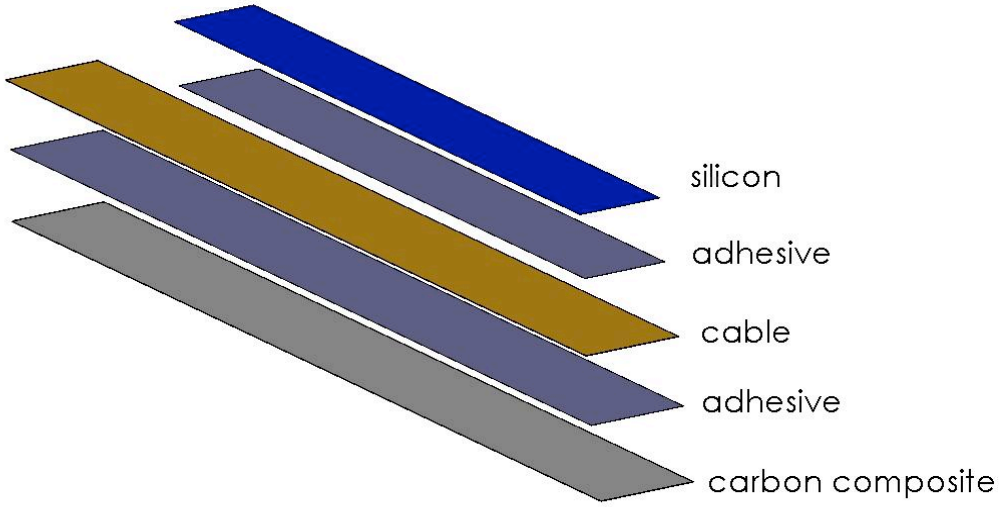

Figure 8: Exploded view of the ladder showing components. The silicon is composed of 10 square chips. It is shown here as a continuous piece of silicon, the way it has been modeled for analysis.

Ladder Support System

A critical part of the ladder support is the thin carbon composite beam which carries one inner ladder and three outer ladders as shown in Figure 9. The beam, which is an adaptation of the ALICE pixel detector design, provides a very stiff support while minimizing the radiation length budget. Significant stiffness is required to control deformations from gravity, cooling air forces and differential expansion forces from both thermal and humidity variations. The composite beam carries a single inner ladder and three outer ladders. Ten of these modules form the two barrel layers. The beam, in addition to its support function, provides a duct for cooling air and adds cooling surface area to increase the heat transferred from the silicon chips. By making the beam from high strength and high thermal conductivity carbon fiber the wall thickness can be as thin as 200 microns and still satisfy the strength and heat transfer requirements. The final thickness however, is limited by fabrication challenges. A forming method has been developed which uses a single male mandrel with vacuum bagging. We have constructed a seven-layer, 244 micron thick, carbon composite beam using a female mandrel which satisfies our requirements.

The ladders will be glued to the beam using low strength silicon adhesive as was done in the ATLAS pixel design. This adhesive permits rework replacement of single ladders.

Support of the sectors (beam with ladders) is done in two halves with 5 sector beams per half module shown in Figure 10. The sector beams are attached to a carbon composite D-tube with precision dove tail mounts for easy assembly and replacement. The D-tube supports the 5 sector beams and conducts cooling air to the sectors.

Kinematic Support and Docking Mechanism

When the pixel detector is in its final operating position it is secured at 3 points with precision reproducible kinematic mounts to the Inner Support Cylinder (ISC) as shown in Figure 11.

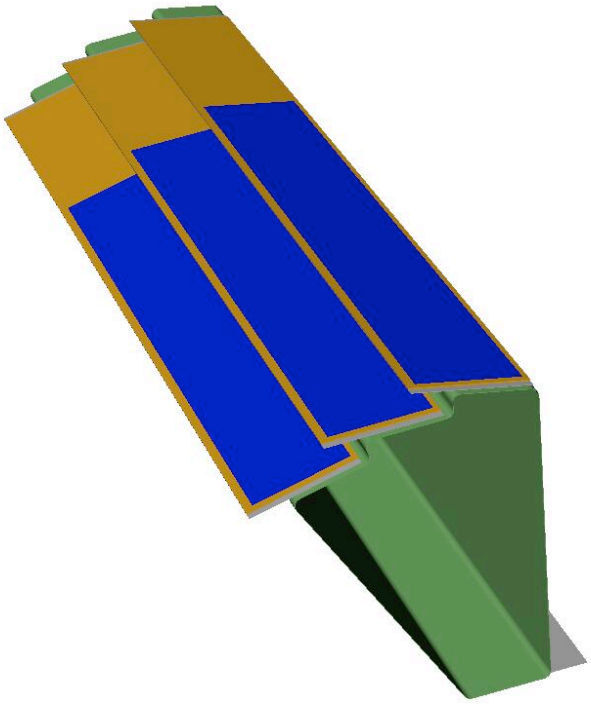

Figure 9: Thin wall carbon support beam (green) carrying a single inner barrel ladder and three outer barrel ladders. The beam in addition to supporting the ladders provides a duct for conducting cooling air and added surface area to improve heat transfer to the cooling air.

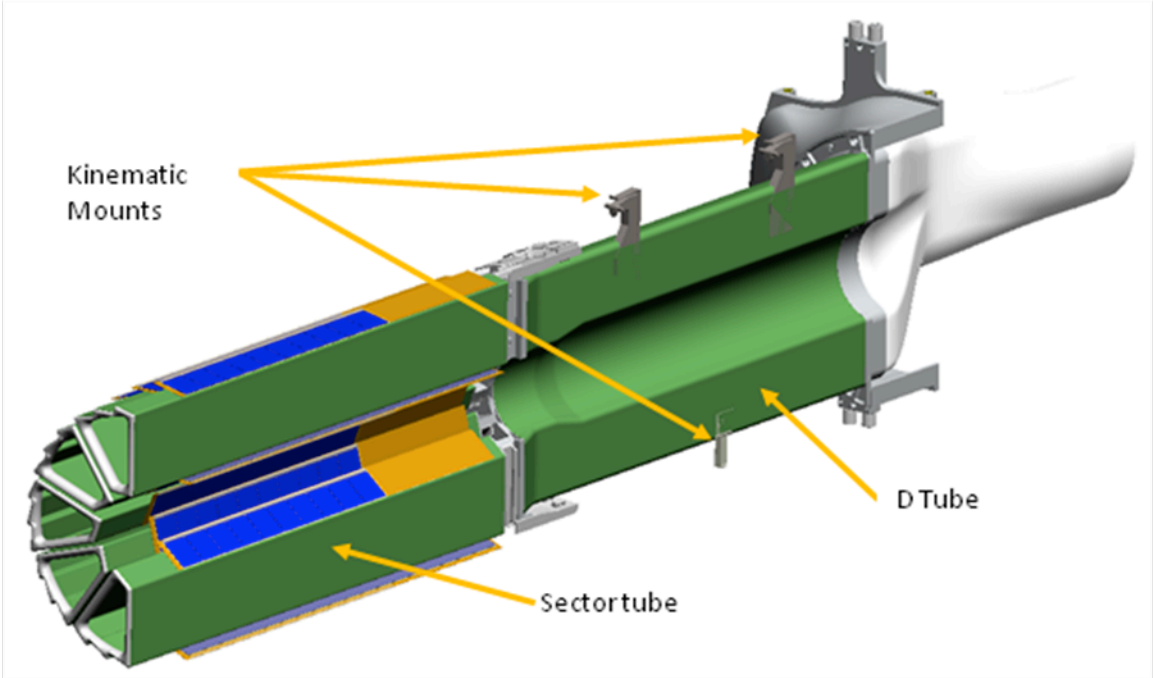

Figure 10: Half module consisting of 5 sector beam modules. The sector beam modules are secured to a carbon composite D tube using a dovetail structure, which permits easy replacement of sector modules. Carbon composite parts are shown in green for greater visibility.

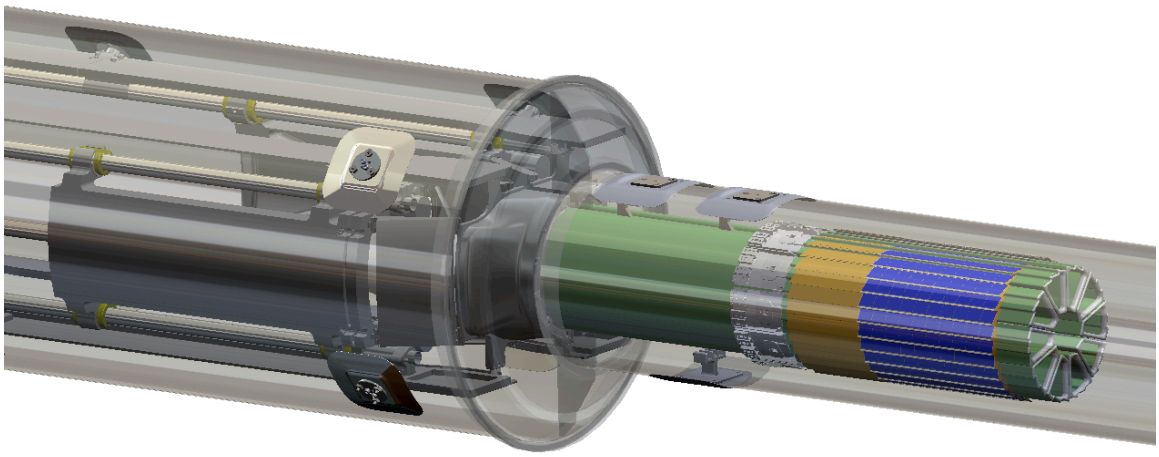

Figure 11: Detector assembly in the installed position supported with three kinematic mounts.

Insertion Mechanism and Installation

The mechanics have been designed for rapid installation and replacement. Installation and removal of the pixel detector will be done from outside of the main STAR detector with minimum disruption to other detectors systems. This will be done by assembling the two halves of the detector on either side of the beam pipe on rails outside of the STAR magnet iron. The detector carriage will be pushed into the center of STAR along the rails until it docks on the kinematic mounts. As shown in Figure 12 and Figure 13, the hinged support structure is guided by cam followers to track around the large diameter part of the beam pipe and close down at the center into the final operating position. Once the detector is docked in the kinematic mounts the hinged support from the carriage is decoupled allowing the kinematic mounts to carry the light-weight detector system with a minimum of external forces affecting the position of the detector barrels. The external loads will be limited to the cables and the air cooling ducts. The cables are loosely bundled twisted pairs with 160 micron conductor plus insulation, so this load should be minimal. The two inch cooling ducts will be the greater load and may require additional design effort to isolate their effect so that the 20 micron position stability for the pixels can be maintained.

Cooling System

Cooling of the detector ladders with pixel chips and drivers is done with forced air. The pixel chips dissipate a total of 160 watts or 100 mW/cm^2 and an additional 80 watts is required for the drivers. In addition to the ladder total of 240 watts some fraction of this is required for voltage regulators and latch-up electronics that are off the ladder but reside in the air cooled volume. The temperature of operation is still under consideration. An optimum temperature for the detectors is around 0 deg C, but they can be operated at 34 deg C without too much noise degradation. The cooling system design is simplified if we can operate at 24 deg C, slightly above the STAR hall temperature; however if a cooler temperature is required, the cooling system will be equipped with thermal isolation and condensation control when the system is shut down. In any case the design will include humidity and temperature control as well as filtration. Cooling studies (see HFT CDR document[21]) show that air velocities of 8 m/s are required over the detector surfaces and a total flow rate of 200 cfpm is sufficient to maintain silicon temperatures of less than 12 deg C above the air temperature.

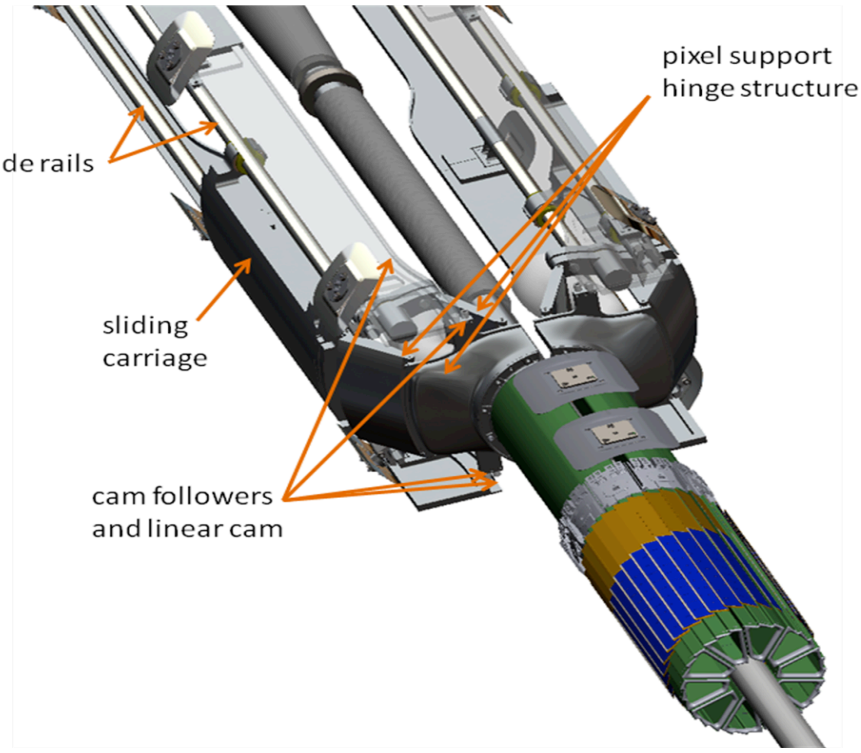

Figure 12: Track and cam guide system for inserting the detector.

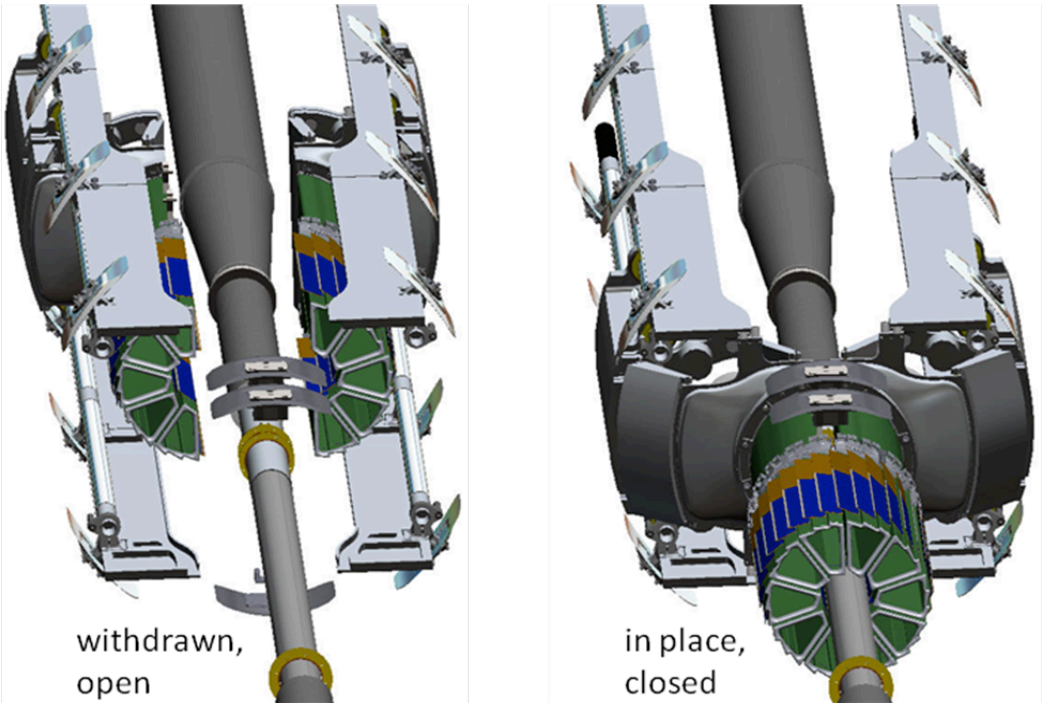

Figure 13: Initially the detector halves have to be sufficiently open to clear the large diameter portion of the beam pipe. They then close down sufficiently to fit inside the Pixel Support Tube (PST) while clearing the beam pipe supports and finally close down to the final position with completely overlapping coverage of the barrels. The beam pipe supports are not shown.

The detector cooling path is shown in Figure 14. Air is pumped in through the support beam. A baffle in the PST forces the air to return back over the detector surfaces both along the beam pipe and along the PST.

The air chiller system providing the cooling air circulating through the PXL detector has not been completely specified yet, but cooling test show that 730 cfpm is sufficient to maintain a detector delta T of 12 deg C. The chiller will be located in the Wide-angle Hall within 50 ft of the pixel enclosure and will be connected with 6 inch flexible ducts. An estimate of the required chiller heat capacity is given in Table 4. This amount of cooling is readily available in the commercial sector.

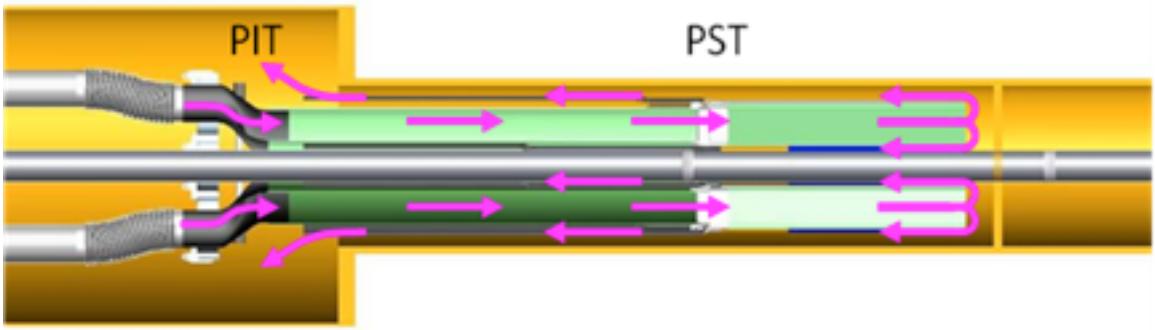

Figure 14: PXL detector cooling air path. The air flows down the center of the sector modules and returns back over the detector ladders on the sector modules and into the larger PIT volume where it is ducted back to the air-cooling unit.

Heat source	Power (watts)
Detector silicon	270
On-ladder signal drivers	80
Voltage regulators in ISC	24
Heat influx through ducting and ISC if 35 deg C below ambient	600 - 2000
Total load on chiller	970 - 2400

Table 4: Preliminary estimate of heat load on the chiller for the PXL air cooling system.

Cabling and Service System

The required wiring connections are identified in Figure 18. The 2 m fine wire twisted pair (pair diameter .32 mm) bundles leading from the ladders to the interface cards are designed to minimize mass, space and mechanical coupling forces that could disturb the pixel positions. The space envelope required for these bundles is illustrated in Figure 15.

There will be a 2'x2'x3' crate for the readout boards. This must be located outside of the main magnetic field and outside of the highest particle flux region. To achieve the required data transfer rates the LVDS signal cables running between this crate and the drivers inside the ISC are limited to 6 meters. To meet these constraints the readout crate will be located on the floor of the hall at the end of the magnet (there is no space on the magnet end ring for mounting the readout box). This will allow for the operation of the PXL system both with and without the pole tip in place.

Alignment and Spatial Mapping

The PXL system is being designed to have full pixel-to-pixel spatial mapping at installation with a 3D tolerance envelope of 20 microns. This will eliminate the need for spatial calibration with tracking other than to determine the 6 parameters defining the PXL detector unit location relative to the outer tracking detectors. Tracking, on the other hand, can use the PXL detector to spatially map the outer detectors, if required.

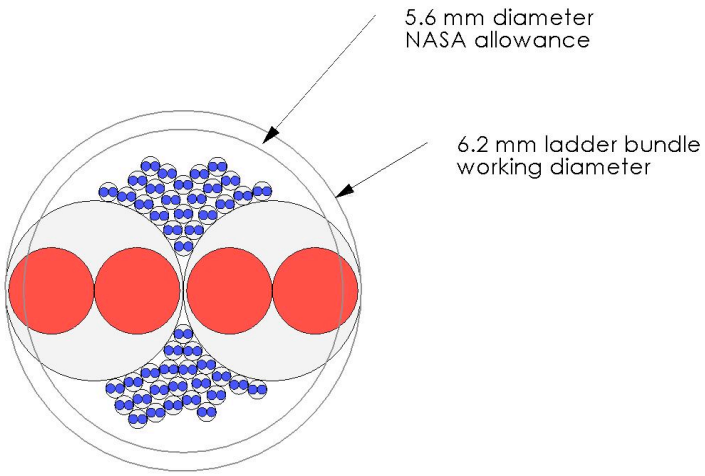

Figure 15: Cable bundle envelope for the ladder connections. The blue pairs include 40 signal pairs, clock and trigger lines and JTAG communication. The red conductors are for power.

The mapping and alignment will be done using a vision coordinate machine to determine the detector locations on the fully constructed ladder half modules. A full 3D map of the ladders is necessary since the manufactured ladder[2] flatness[3] will exceed the 20 micron envelope. After mapping, the half modules will be installed in STAR without disturbing the relative positions of the pixels.

Addressing this in more detail, a support fixture for the half modules will be used in the vision coordinate machine, which has kinematic mounts identical to the kinematic mounts in the ISC for securing the half module. The pixel chips will be manufactured with reference targets in the top metal layer that can be picked up by the vision coordinate machine and the ladders will be mounted such that there is an unobstructed view. The fixture will be rotated for each ladder measurement. Full 3D measurements of the chips on the ladder are required since the ladder flatness will lie outside of the 20 micron envelope. The fixture will have precision reference targets on each ladder plane so that the ladder points can be tied together into a single coordinate frame. The map of the fixture targets can be measured once with a touch probe measuring machine and thus avoid extreme machining tolerance requirements for the fixture. Precision machining, however, will be required, for the kinematic mounts and their placement tool.

For this approach to work the ladders must hold to their mapped position within 20 microns independent of changes in temperature, humidity and gravity direction. Since the detector ladders have 1 mm overlapping active regions with their neighbors, a check of the mapping accuracy will

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[2] http://rnc.lbl.gov/hft/hardware/docs/position_writeup.pdf

[3] http://www.lbnl.leog.org/crossing_lines_measurement_first_look.htm

be done with tracking. Detailed information on mechanical design simulation and prototyping may be found in the HFT CDR document.[21]

3.2.2. Sensors and Readout

Sensor Development

We approach the design of the electronics for the PXL detector as a two stage development process with the readout system requirements tied to the stages of the sensor development effort. The sensor development is taking place at the Institut Pluridisciplinaire Hubert Curien (IPHC) in Strasbourg, France, where we are working in collaboration with Marc Winter's group. The first set of prototype sensors to be used at STAR will have digital outputs and a 640 μs integration time. We will use these sensor prototypes to construct a prototype sector for deployment in the STAR detector. This prototype system will employ the mechanical design to be used for the final PXL detector as well as a readout system that is designed to be a prototype for the expected final system. We will also test the final PXL sensors with a full scale prototype.

Monolithic Active Pixel Sensor Development at IPHC

The sensor development path for the PXL detector sensors is tailored to follow the development path of the technology as it was set by the IPHC group. In this path, the Monolithic Active Pixel Sensors (MAPS) with analog multiplexed serial analog outputs in a rolling shutter configuration are envisioned as the first generation of sensors followed by a more advanced final or Ultimate sensor that has digital outputs. The analog MAPS have been produced and tested and our sensor development path will soon move to digital binary readout from MAPS with fine-grained threshold discrimination, on-chip correlated double sampling (CDS) and a fast serial LVDS readout. A diagram showing the development path, with the attendant evolution of the processing and readout requirements, is shown in Figure 16.

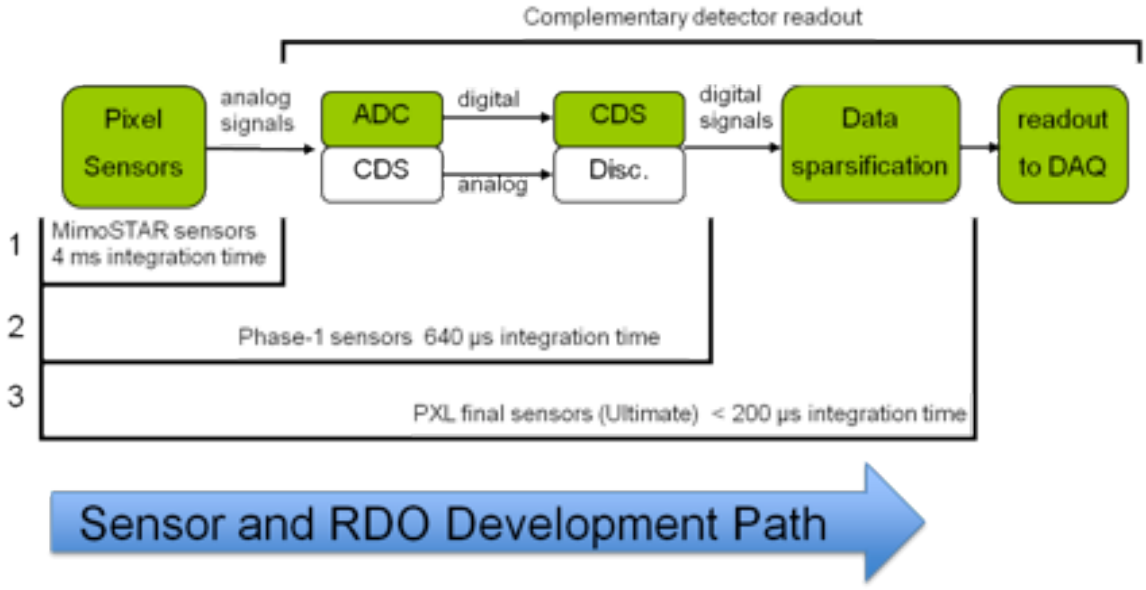

Figure 16: Diagram showing the development path of sensors for the STAR PXL detector at IPHC in Strasbourg. The readout data processing required is shown as a function of sensor generation.

The Mimostar series sensors are the first generation of sensors that have been fabricated and tested. These are 50 MHz multiplexed analog readout sensors with 30 μm × 30 μm pixels in variously sized arrays depending on generation. This generation has been tested and characterized and appears to be well understood. Testing with these sensors is described in Reference [23].

The current generation of sensor is named "Phase-1". This sensor is based on the Mimosa-8 and Mimosa-16 sensor technology and contains on-chip correlated double sampling and column level discriminators providing digital outputs in a column parallel shift configuration. The Phase-1 sensors are full sized 640 × 640 arrays resulting in a full 2 cm × 2 cm sensor. In order to achieve a 640 μs integration time, the Phase-1 sensor is equipped with four LVDS outputs running at 160 MHz.

The final sensor generation is named "Ultimate". The Ultimate sensor includes all of the attributes of the Phase-1 sensor with the pixel sub-arrays clocked faster to give a < 200 μs integration time. The pixel size has been reduced to 20.7 μm × 20.7 μm to increase the sensor radiation tolerance in the higher luminosity RHIC II environment. The Ultimate sensor also includes a row level run length encoding based on a data sparsification and zero suppression circuit. There are two data output lines from the sensor and the data rates are low thanks to the newly included data sparsification circuitry. The first prototype sensors of this design have been delivered for testing in April of 2011.

Sensor Series Specifications

The specifications of the sensors under development are shown in Table 5. The Phase-1 sensor is a fully functional design prototype for the Ultimate sensor, which results in the Phase-1 and Ultimate sensors having very similar physical characteristics. After successful development and testing of the Phase-1 sensors, a data sparsification system named SUZE which has been developed and tested by IPHC will be integrated with the Phase-1 design. Finally, the Ultimate sensor will include an enhancement allowing for faster clocking of the sub-arrays.

	Phase -1	**Ultimate**
Pixel Size	30 μm × 30 μm	20.7 μm × 20.7 μm
Array size	640 × 640	928 × 960
Active area	~ 2 × 2 cm	~ 2 × 2 cm
Frame integration time	640 μs	100 – 200 μs
S/N	>12	>12
Readout time / sensor	640 μs	100 – 200 μs
Outputs / sensor	4	2
Operating mode	Column parallel readout with all pixels read out serially.	Column parallel readout with integrated serial data sparsification.
Output type	Digital binary pixel based on threshold crossing.	Digital addresses of hit pixels with row run length encoding and zero suppression. Frame boundary marker is also included.

Table 5: Specifications of the Phase-1 and Ultimate sensors.

In addition to the specifications listed above, both sensors will have the following additional characteristics:

- Marker signal indicating frame boundaries.
- Register based test output pattern JTAG selectable for binary readout and troubleshooting.
- JTAG selectable automated testing mode that provides for testing pixels in automatically incremented masked window to allow for testing within the overflow limits of the zero suppression system.
- Independent JTAG settable thresholds.
- Radiation tolerant pixel design.
- Minimum of 3 fiducial marks per sensor for optical survey purposes.
- All bonding pads located along one side of the sensor.
- Two bonding pads per I/O of the sensor to facilitate probe testing before sensor mounting.

Architecture for the Phase-1 Sensor System

We have designed the prototype data acquisition system to read out the large body of data from the Phase-1 sensors at high speed, to perform data compression, and to deliver the sparsified data to an event building and storage device.

The requirements for the Phase-1 prototype and final readout systems are very similar. They include:

- Triggered detector system fitting into the existing STAR infrastructure and to interface to the existing Trigger and DAQ systems.
- Deliver full frame events to STAR DAQ for event building at approximately the same rate as the TPC (~ 1 KHz for the STAR DAQ1000 upgrade).
- Reduce the total data rate of the detector to a manageable level (≤TPC rate).

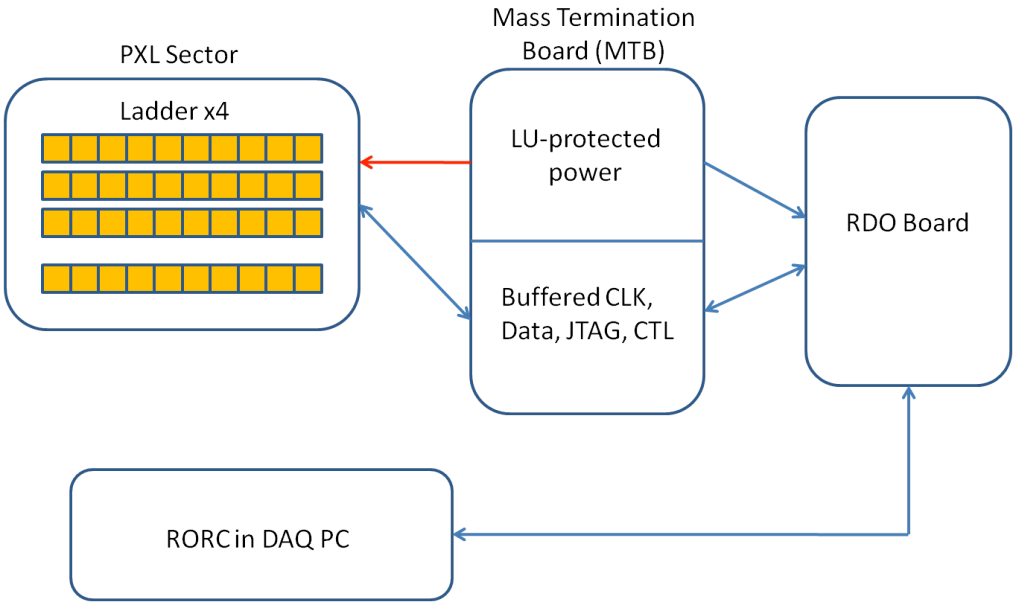

Figure 17: Functional block schematic for the readout for one sector of a Phase-1 prototype system. The detector ladders and accompanying readout system have a highly parallel architecture. One system unit of sensor array/readout chain is shown. There are ten parallel sensor array/readout chain units in the full system.

The proposed architecture for the readout of the Phase-1 prototype system is shown in Figure 17 with the physical location and separation of the system blocks shown in Figure 18.

The architecture of the readout system is highly parallel. Each independent readout chain consists of a four-ladder mechanical carrier unit (a sector) with each ladder containing ten Phase-1 sensors. The current plan is to install a patch of Phase-1 sensors consisting of at least three sectors mounted with the final mechanical positioning device and located 120 degree apart.

The basic flow of a ladder data path starts with the MAPS sensors. A PXL ladder contains 10 Phase-1 MAPS sensors, each with a 640 × 640 pixel array. Each sensor contains four separate digital LVDS outputs. The sensors are clocked continuously at 160 MHz and the digital data containing the pixel threshold crossing information is read out, running serially through all the pixels in the sub-array. This operation is continuous during the operation of the Phase-1 detectors on the PXL ladder. The LVDS digital data is carried from the four 160 MHz outputs in each sensor in parallel on a low mass flex printed circuit board to discrete LVDS buffers located at the end of the ladder and out of the low mass detector region. This portion of the ladder also contains the buffers and drivers for the clocks and other control signals needed for ladder operation.

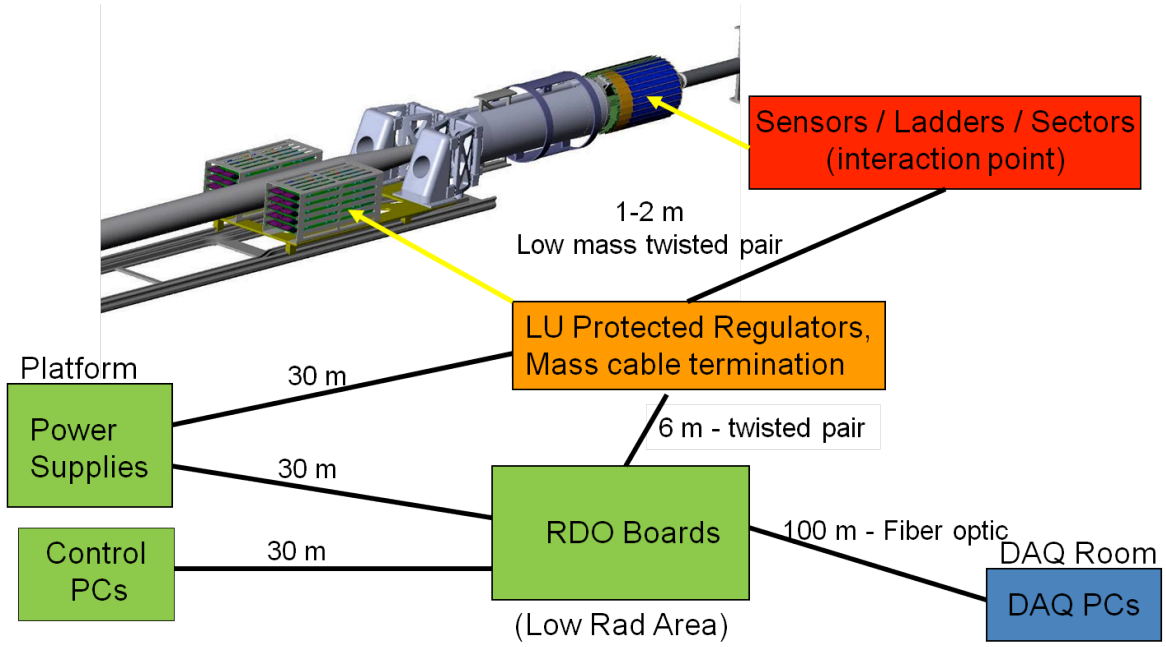

Figure 18: Physical layout of the readout system blocks. This layout will be the same for both the Phase-1 based patch and the final PXL detector system.

Each Phase-1 sensor requires a JTAG connection for register-based configuration, power, ground, a 160 MHz readout clock and a synchronization signal to start the readout. These signals, the latch-up protected power, as well as the LVDS outputs and synchronization and marker signals from the detectors are carried via low mass twisted pair cables from the discrete electronics at the end of the ladder to a power/mass termination board located approximately one meter from the PXL ladders. There is one readout board per PXL sector (40 sensors). A diagram of a ladder is shown in Figure 19.

The flex cable parameters are:

- 2 layer - 150 micron thickness in the low mass acceptance area
- Aluminum Conductor
- Radiation Length ~ 0.1 %

- 40 LVDS pair signal traces
- Clock, JTAG, sync, marker traces

The connection to the driver end of the ladders will be made with a very fine 150 μm diameter twisted pair wire. These wires will have very low stiffness to avoid introducing stresses and distortions into the mechanical structure. The other ends of these fine twisted pair wires will be mass-terminated to allow connection to the Mass-termination board (MTB) located approximately one meter away.

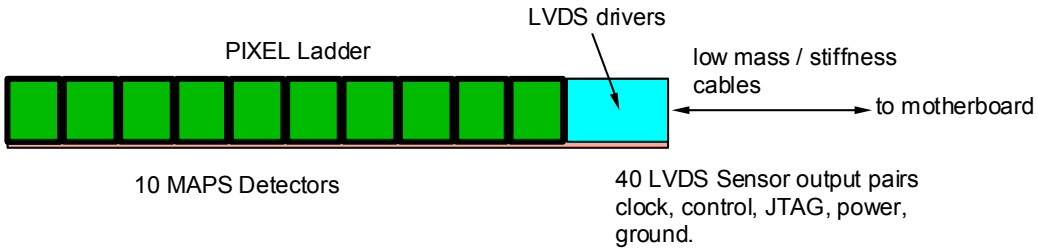

Figure 19: Assembly of sensors on a low radiation length Kapton flex cable with aluminum conductors. The sensors are connected to the cable with bond wires along one edge of the ladder.

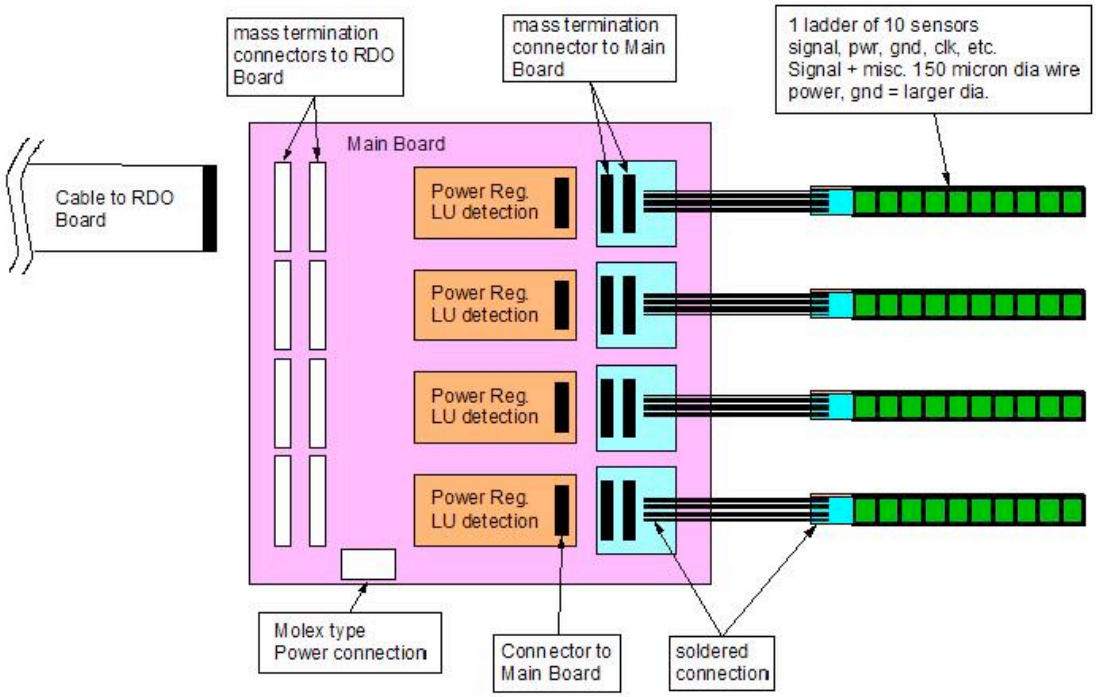

Figure 20: Power and mass-termination board block diagram. The digital signals to and from the sensors are routed through the main board and are connected to the readout boards via the mass-termination connectors on the main board. Latch-up protected power regulation is provided to each ladder by a daughter card mounted to the main board. The main power supplies will be located far from the detector (in the STAR racks).

Latch-up protected power is provided to the sensors from the MTB boards. Each ladder has independently regulated power with latch-up detection circuitry provided by a daughter card that plugs into the MTB board. There are four regulation and latch-up daughter cards per MTB board

and a total of 10 MTB boards are needed for the complete detector system readout. A block diagram for the PM board is shown in Figure 20.

The digital sensor output signals will be routed, along with a 160 MHz clock signal, to the MTB where the digital signals will be buffered and then routed to the readout boards (RDO). The RDOs will be mounted in a movable electronics rack located on the main magnet iron of the STAR magnet. The RDO location is approximately 6 meters away from the MTB boards, which are approximately 2 meters from the Si sensors. A diagram describing the RDO system can be seen in Figure 21. A functional block diagram of the RDO can be seen in Figure 22.

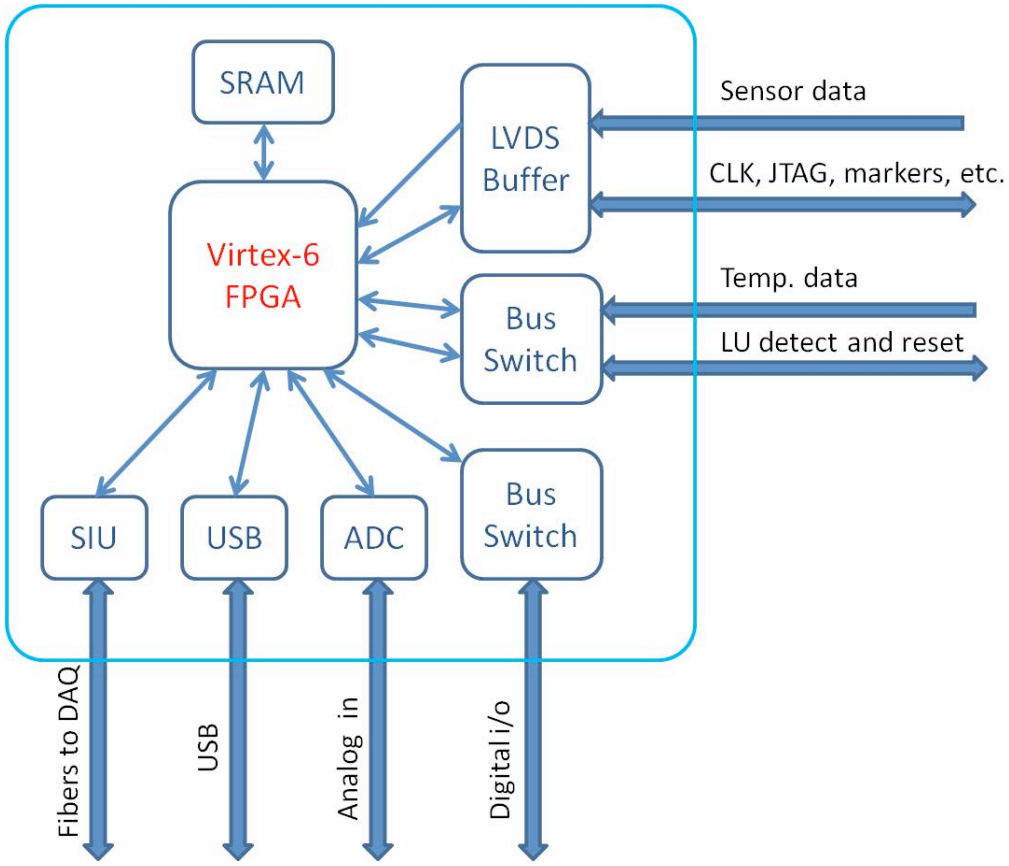

Figure 21: Readout board. The readout system consists of one RDO board per sector of 40 sensors. The RDO board is a custom PCB that provides all of the I/O functions including receiving and buffering the sensor data outputs, receiving the trigger from STAR, and sending the built events to a STAR DAQ receiver PC via the ALICE DDL fiber optic connection. The data processing on the RDO motherboard is performed with a Xilinx Virtex-6 FPGA.

The current RDO prototype boards are based on a fast Xilinx Virtex-5 FPGA development board, which is mated to a custom motherboard. The motherboard provides several functions, including LVDS buffering into the FPGA, a STAR trigger input, PMC connectors for mounting a fiber optic Detector Data Link (DDL), SRAM, and various ADCs and I/O connectors to be used in both individual sensor testing and production probe testing of thinned sensors.

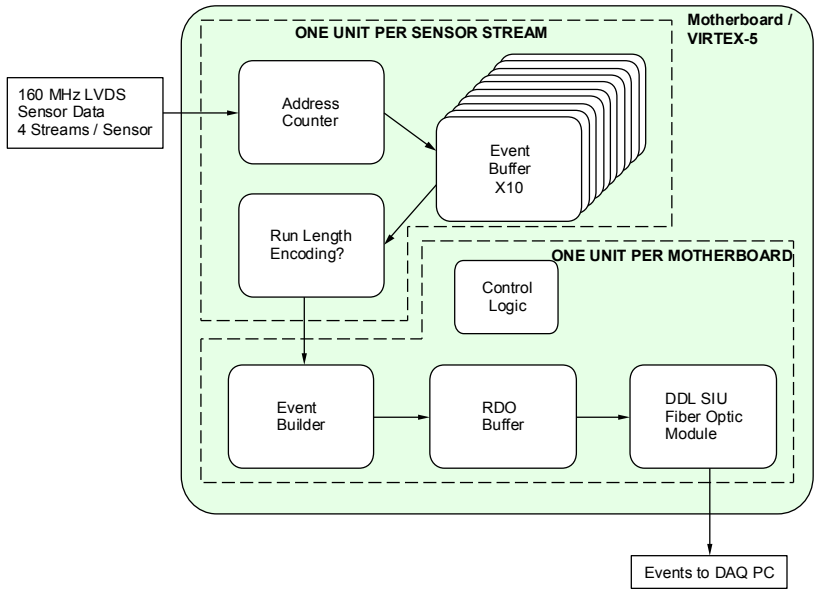

Figure 22: Functional block diagram of the data flow on the RDO boards.

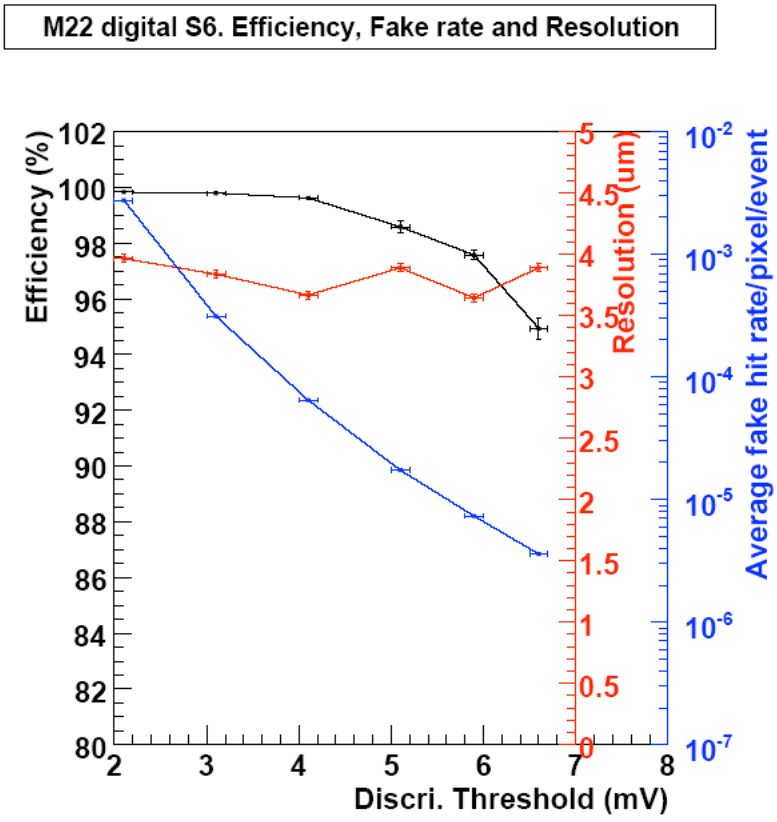

Figure 23: Efficiency versus fake hit rate for a Mimosa-22 sensor, a prototype for the Phase-1 sensor. The figure is obtained from live-beam data taken with 120 GeV/c pions at the CERN test beam facility.

The data processing path takes several steps. First, the sensor output signals are buffered and then fed into the FPGA. In the FPGA the data is re-sorted to give a raster scan, after which the location of pixels with hits are converted to pixel addresses using an address counter. Zero suppression is achieved by the conversion of hits to addresses in a relatively low multiplicity environment and this is the main mechanism for data reduction used in the readout system. The efficiency and accidentals rate for the Mimosa-22 sensor, a prototype for the Phase-1 with on chip CDS and column level discriminators is shown in Figure 23.

When a trigger is received, one of a bank of event buffers is enabled for one frame of data (409,600 pixels). After the frame has been recorded in the event buffer, the results of that frame are sent to an event builder. The event builder gathers all of the addresses on the RDO and builds them into an event, which is then passed via fiber optic links to the STAR DAQ receiver PCs.

We intend to use the Source Interface Unit (SIU) and Readout Receiver Cards (RORC) developed for ALICE as our optical link hardware to transfer data to and from the STAR DAQ system. These links have been chosen as the primary readout connections for the new STAR TPC FEE. Leveraging existing hardware and expertise in STAR allows for a faster and more reliable design than developing our own custom solution.

The complete readout system consists of a parallel set of sector readouts (4 ladders per sector) with ten separate readout chains. A system level functionality block diagram is shown in Figure 24.

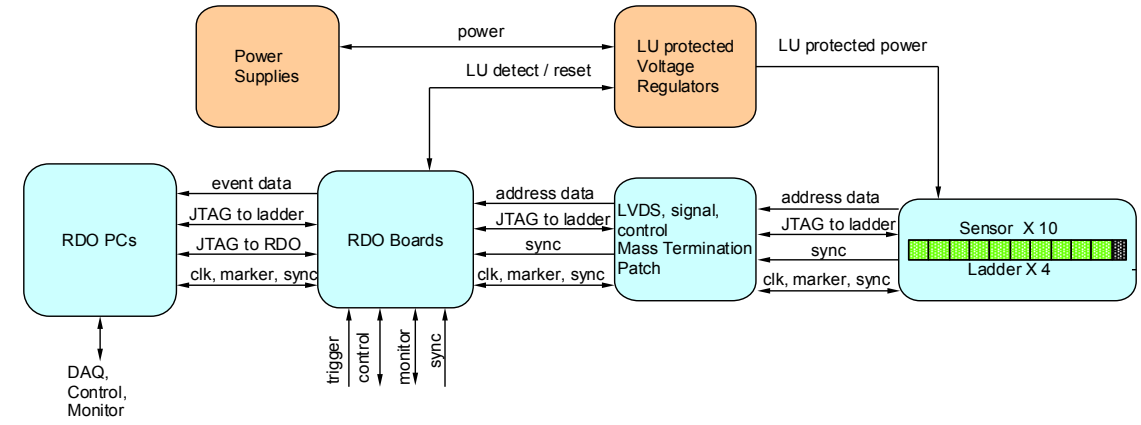

Figure 24: System level functionality diagram of the readout of the PXL sensors. One of the ten parallel readout chains is shown.

Data Synchronization, Readout, and Latency

The Phase-1 PXL sensors are read out continuously. Hit-to-address processing is always running during the normal operation of the detector. The PXL will receive triggers and the STAR clock via the standard STAR Trigger and Clock Distribution module (TCD). The receipt of a trigger initiates the saving of the found hit-addresses into an event buffer for one frame (409,600 pixels). The PXL detector as a whole will be triggered via the standard STAR Trigger Clock Distribution (TCD) module. Since 640 μs is required to read out a complete frame of interest, the data will be passed to DAQ for event building about 640 μs after the trigger is received. We will provide for multiple buffers that will allow us to capture temporally overlapping frames of data. This will allow us to service multiple triggers within the 640 μs readout time of the sensor. In this system, the hit address data is fanned out to ten event buffers. A separate event buffer is enabled for the duration of one frame upon the receipt of a trigger from the TCD. Subsequent triggers enable

additional event buffering until all of the event buffers are full and the system goes busy. The resulting complete frames are then passed to the event builder as they are completed in the event buffers. This multiple stream buffering gives a system that can be triggered at a rate above the expected average rate of the STAR TPC (approximately 1 kHz). Furthermore, since the addition of buffers is external to the sensors, the capability for the addition of large amounts of fast SRAM will be included in the RDO board design allowing for flexibility in our readout system configuration. This multiple event buffer architecture will result in the duplication of some data in frames that overlap in time. However, our data rate is low and the duplication of some data allows for contiguous event building in the STAR DAQ, which greatly eases the offline analysis. In addition, synchronization between the ladders/boards must be maintained. We will provide functionality to allow the motherboards to be synchronized at startup and any point thereafter.

Triggering Considerations

The primary tracking detector of the STAR experiment is the TPC with the Heavy Flavor Tracker upgrade designed to add high-resolution vertex information. The PXL detector is part of a larger group of detectors that make up the HFT upgrade at STAR. The other tracking detector components of the HFT include the Silicon Strip Detector (SSD) and the Intermediate Silicon Tracker (IST). Since the HFT is a system of detectors, in order to maximize efficiency, the trigger response and dead time characteristics of each detector in the HFT system should be matched, as much as possible, to the others. As the main detector, the post DAQ-1000 TPC sets the effective standard for the other detectors in the system. In the current understanding of the system, the PXL detector information is only useful in conjunction with the external tracking detectors and thus the PXL detector will only be triggered when the TPC is triggered.

The triggers in STAR are produced randomly with a 107 ns crossing clock spacing. The behavior of the TPC is to go dead for 50 μs following the receipt of a trigger. This means that the TPC, and by extension the PXL detector, will receive random triggers spaced by a minimum of 50 μs. An additional constraint is imposed by the fact that the TPC data acquisition system contains 8 buffers at the front end. This allows for the capability of the TPC to take a quick succession of 8 triggers (separated by 50 μs) but then the TPC will go busy until the data has been transferred and buffers cleared. The time required for this depends on the event size. Some of these numbers can be found at http://drupal.star.bnl.gov/STAR/daq1000-capabilities. Other statistics about DAQ1000 are private communication with the STAR DAQ group[22]. This behavior provides the basis for the assessment of the trigger response characteristics of the detectors in the HFT system. In general, the HFT detector readout system will provide for the acquisition of up to 8 successive triggers separated by 50 μs with some, as yet uncharacterized, clearing time. The goal is to have the HFT detectors "live" whenever the TPC is "live". In Reference [21] we show an analysis of the trigger response characteristics of the PXL detector.

System Performance for the Phase-1 Prototype Sensor System

The raw binary data rate from each Phase-1 sensor is 80 MB/s. Extending this data rate to the 400 sensors that would make up a Phase-1 sensor based PXL detector, the full data rate would be 32 GB/s. The raw rate must clearly be reduced to allow integration of the PXL data stream into the overall STAR data flow. Zero suppression by saving only addresses of hit pixels is the main mechanism for data volume reduction. The parameters used to calculate the data rates are shown in Table 6.

Based on the parameters given above, the average data rate (address only) from the sensors in the prototype Phase-1 detector is 237 kB per event which give an average data rate of 237 MB/s. It is possible to reduce the data rate further using a run length encoding scheme on the addresses as

they are passed from the event buffer to the event builder as indicated in Table 6. We are currently investigating this option, though the data rate reduction from this approach is expected to be moderate. The raw data rate reduction from the hit-pixel to address conversion is shown graphically in Figure 25.

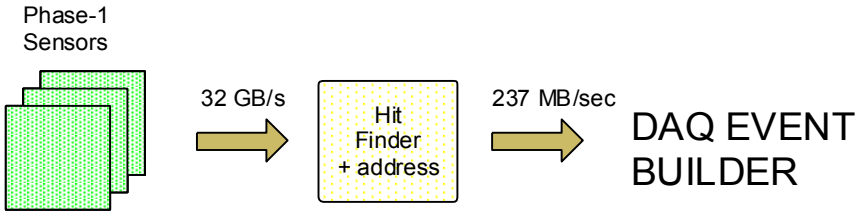

Figure 25: Data rate reduction in the Phase-1 readout system.

Bits per address	20
Integration time	640 μs
Luminosity	3 x 10^{27}
Hits per frame on inner sensors (r = 2.5cm)	295
Hits per frame on outer sensors (r = 8.0cm)	29
Sensors inner ladders	100
Sensors outer ladders	300
Average pixels per cluster	2.5
Average trigger rate	1 kHz

Table 6: Parameters used to calculate simple data rates from a Phase-1 based system.

Architecture for the Ultimate Sensor System

The most significant difference between the Phase-1 and Ultimate sensors is the inclusion of zero suppression circuitry onboard the sensor. The ultimate sensors provide zero suppressed sparsified data with two LVDS output lines per sensor. Another difference between the Phase-1 and Ultimate sensors is that the pixel size for this final production sensor is reduced to 20.7 μm. This is useful because a smaller pixel has a shorter charge collection time making it more radiation tolerant. In addition, the sub-frame arrays are clocked faster to give a < 200 μs integration time and a frame boundary marker is added to the data stream to allow for the demarcation of frame boundaries in the absence of hits in the sensor and to allow for synchronization with the RDO system. The upgrade from the Phase-1 to the Ultimate sensors in the system is expected to involve the fabrication of new sensor ladders using the same mechanical design used in Phase-1 but using the new Ultimate series sensors and a redesign of the Kapton readout cable. The Kapton cable for the Ultimate sensor will require significantly fewer traces (20 LVDS pairs instead of 40) for readout and the new cable design should have a lower radiation length. The task of reading out the Ultimate series sensors is actually less challenging than the readout of the Phase-1 sensors since the data reduction functionality is included in the sensor.

The readout hardware described above for the Phase-1 readout system remains the same for the Ultimate readout system. Some reconfiguration of the functionality in the FPGA is required for readout of the Ultimate sensor PXL detector but that is all done in the software. A functional block diagram for the RDO boards is shown in Figure 26.

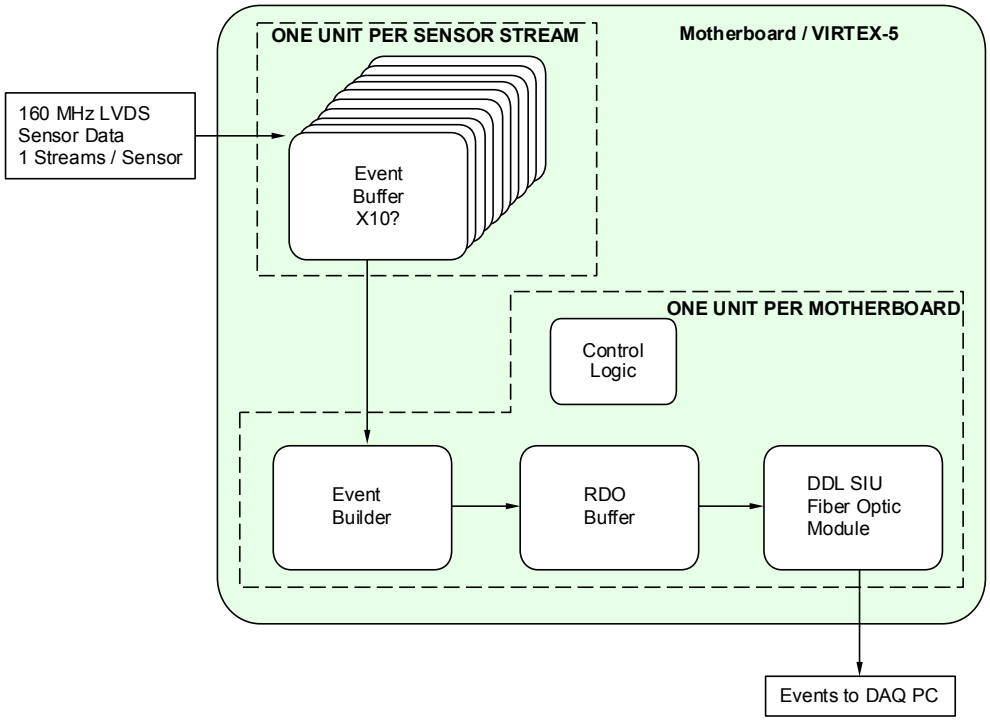

Figure 26: Functional block diagram of the RDO boards for the readout of the Ultimate detector based PXL detector.

The Ultimate sensor operates in the same column parallel shift readout mode as the PHASE-1 sensor. The address data, which is clocked out of the Ultimate chip has well defined latencies that we will use to keep track of triggered frame boundaries and which can be verified using synchronization markers from the sensors. For example, the first pixel marker from the sensor corresponds to the actual scan of pixels through the sensor and the frame boundary marker delineates frame boundaries in the sparsification system on the sensor. Using this information and knowing the internal latencies in the sensor, we can generate the internal logic in the FPGA to implement the same multiple buffering technique that was previously described.

Bits per address	20
Integration time	200 μs
Luminosity	8×10^{27}
Hits per frame on inner sensors (r=2.5cm)	246
Hits per frame on outer sensors (r=8.0cm)	24
Sensors inner ladders	100
Sensors outer ladders	300
Average pixels per cluster	2.5
Average trigger rate	1 kHz

Table 7: Parameters used to calculate data rates from an Ultimate sensor based system.

System Performance for the Ultimate Sensor System

The parameters used to calculate the data rates for the system are shown in Table 7. From these parameters, we calculate an average event size of 209 kB giving an address data rate of 209 MB/s

from the Ultimate sensor based PXL detector. A more detailed analysis of the readout chain including parameters for the size of buffers and a discussion of the internal FPGA functions are included in Reference [21].

3.2.3. Sensors and Readout Simulation and Prototyping

Mimostar-2 based Telescope Test at STAR

Using a preliminary system design for the analog readout, we have taken data with a set of Mimostar-2 sensors at STAR. This system is an early prototype whose performance is evaluated as part of the overall vertex detector development effort. We have successfully implemented a continuous readout using a 50 MHz data acquisition system with on-the-fly data sparsification that gives nearly three orders of magnitude data reduction compared to the raw ADC rates. The readout system was mated with a prototype Mimostar2 sensor and configured in a telescope geometry to measure the charged particle environment in the STAR environment near the PXL detector position. The detector telescope is shown in Figure 27.

Figure 27: Three Mimostar-2 sensors in the telescope configuration used in the beam test at STAR.

We found that the system worked well, gave reasonable efficiency and accidental hit rates, and measured an angular distribution of tracks consistent with imaging the interaction diamond and with imaging a beam-gas interaction type background. The prototype readout system integrated well into the existing STAR electronics and trigger infrastructure and functioned successfully as any another STAR detector subsystem. The prototype readout system and the results have been published in NIM.[23]

LVDS Data Path Readout Test

The readout system architecture for the Phase-1 and Ultimate sensors contains a high-speed digital data path that is required to read out the sensor hits during the sensor integration time. The RDO sensor data interface path requires that LVDS data move over a total distance of 6 to 8 meters at a rate of 160 MHz for Phase-1 and 125 MHz for Ultimate. 1 to 2 meters of this distance is over high impedance fine twisted pair wire. Since the design is challenging, though it works on paper, it was decided that it would be prudent to make a prototype set of test boards and check the performance of our design as a precursor to starting a production design for the final set of readout boards. We have completed making a complete set of test boards for one basic block of the highly parallel RDO system consisting of a functional ladder mockup, mass-termination board prototype and a limited functionality RDO motherboard coupled to a Xilinx Virtex-5 Development board. The test was successful with bit error rates of approximately 10^{-14} for the configuration and clock speed needed for the detector. A report on this test may be found in the HFT CDR document.[21]

Ladder and RDO board Prototypes

In addition to developing readout systems to test the individual sensors described in the development plan, we have been actively prototyping the readout system described above. The prototyping has concentrated on producing a working readout chain consisting of a ladder of ten Phase-1 sensors connected to a prototype mass-termination board (with LU protected ladder power supply daughter-cards), read out with a prototype RDO motherboard into a DAQ PC via the ALICE DDL fiber system. A set of photographs of the components of our prototype system may be seen in Figure 28.

The Infrastructure Test Board (ITB) is a FR-4 based early prototype ladder. This is the first stage in our ladder/cable development plan which is summarized below.

- Stage1 – Infrastructure Testing Board - evaluate the general design of running 10 sensors on a ladder and find and test the working envelope of bypass capacitance and power supply and ground connection.
- Stage 2 – FR-4 ladder cable prototype with Cu - Taking the knowledge gained in the Infrastructure Test Phase, we now attempt to fit the readout cable traces into the required size of the ladder readout cable.
- Stage 3 – Kapton ladder cable prototype with Cu – Translate above design to kapton flex.
- Stage 4 – Kapton ladder cable with Al – production prototype for the final ladder cable.

A complete description of this process is available as part of a response to our CD-1 review and may be found at http://rnc.lbl.gov/hft/hardware/docs/cd1/PXL_flex_cable_and_sys_test_v2.doc.

The prototype MTB and LU protected daughter-cards have been fabricated for a full 4 ladder data path.

We have developed and tested a RDO prototype based on a XILINX VIRTEX-5 development board mated to a custom motherboard. A diagram showing this configuration is shown in Figure 29. The firmware and software developed for the prototype system will be completely compatible with the final custom RDO boards which will be fabricated using a Xilinx Virtex-6 FPGA.

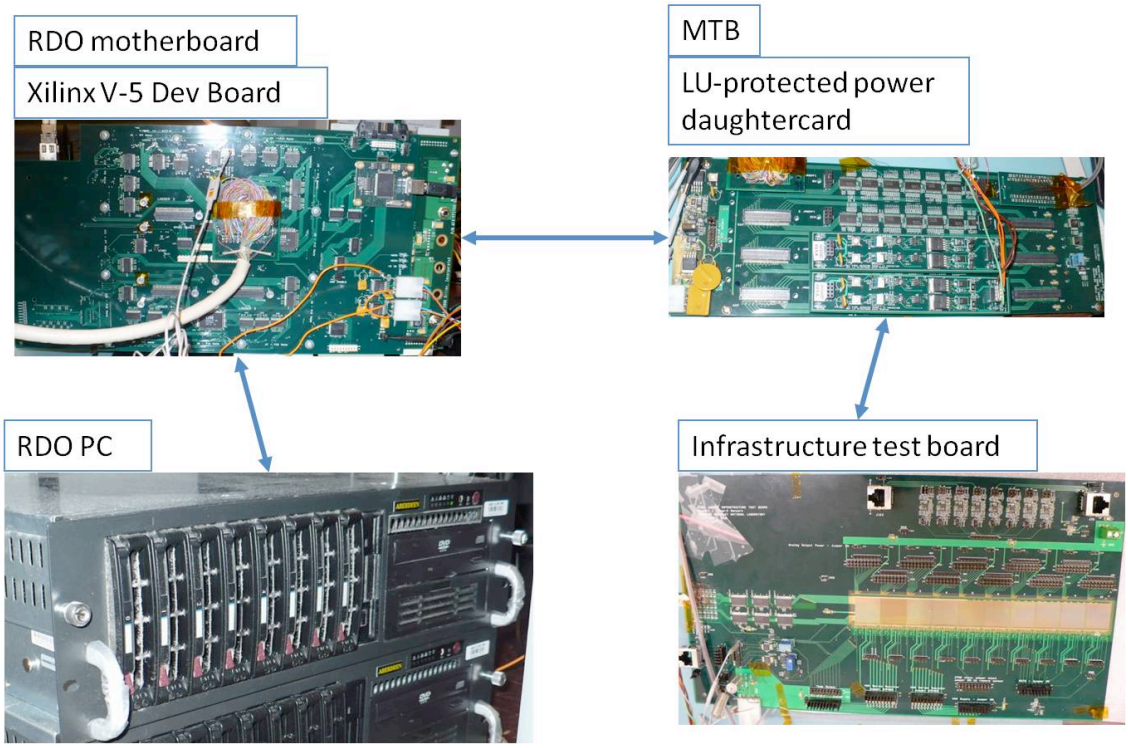

Figure 28: The prototype ladder test system. An Infrastructure Test Board (ITB) containing ten Phase-1 sensors is connected via fine twisted pair wire to a prototype MTB which provides buffering of the digital signals and provides LU protected power to the ladder. The data and control signals are then carried over a 6 meter cable to a prototype RDO board which performs zero suppression and builds an event which is then transferred to the DAQ PC via a fiber connection.

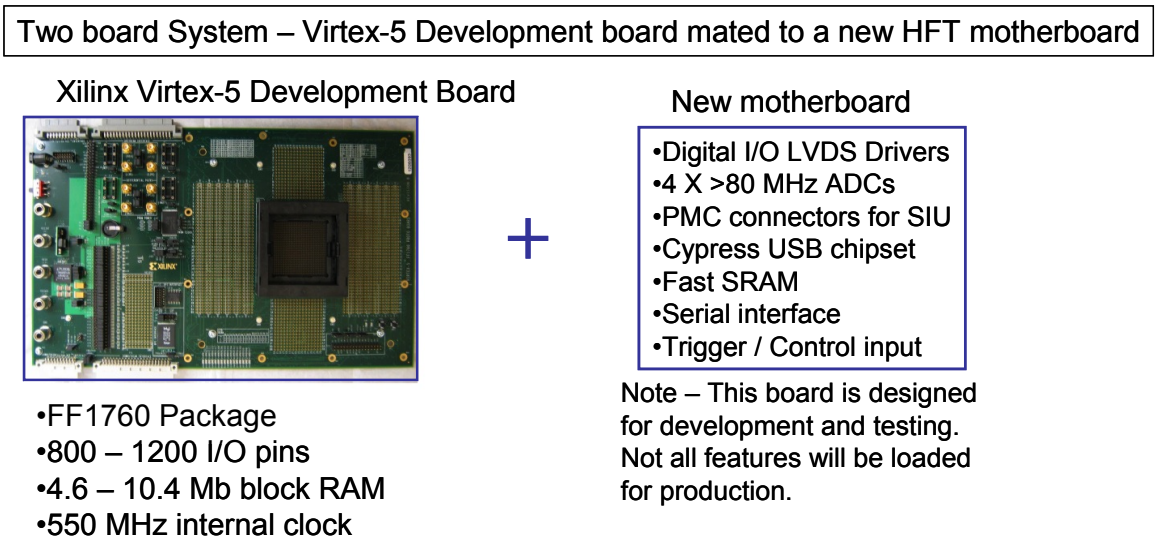

Figure 29: Prototype RDO board design is composed of a Xilinx Virtex-5 development board mated to a custom RDO motherboard. The final RDO boards will be a custom design using a Xilinx Virtex-6 FPGA.

This prototype system is assembled and working for reading out any individual sensor of the ten Phase-1 sensors loaded onto the ITB. We are characterizing the performance of the sensors in a ladder configuration and finishing the firmware to allow for the readout of all ten sensors in the event format that we expect to use in the final system. From that point, the parallelism of the system allows for easy extension of the tested pieces to the full detector.

3.2.4. Engineering Prototype

As an important milestone in the HFT construction we have scheduled an engineering prototype run with the PXL configuration shown in Figure 30. An engineering run with the HFT PXL detector serves a number of important functions that are required in the development of a robust detector system capable of producing useful physics in a timely fashion. Some functions address resolution of questions that could affect or require modification of the final design. Other functions address the need to get an early start on hardware and software commissioning in order to guarantee physics results from the first run with the HFT.

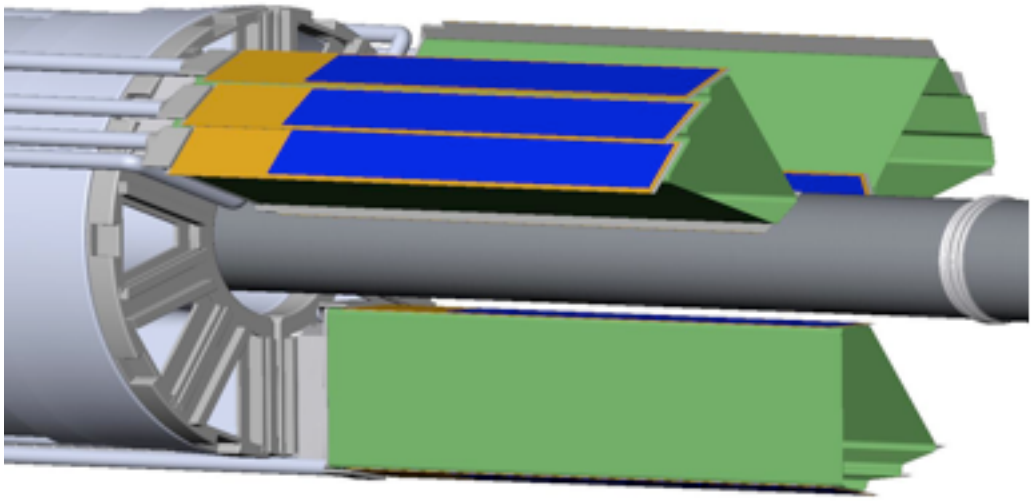

Figure 30: PXL configuration for the engineering prototype.

The engineering run will provide a test for vulnerability to wakefield generated noise or other unanticipated noise sources. We don't expect this to be an issue with our detector design, but if the engineering run exposes a problem then RF shielding would be implemented.

Every effort is being made to insure that the HFT PXL detector will meet the requirements of mechanical stability while operating in the STAR environment. However, if the engineering run reveals difficulties resulting from unanticipated issues with the STAR environment then they can be addressed before operation with the completed HFT detector.

The PXL detector electronics system, detector plus read out, will be tested with the STAR DAQ and trigger system prior to the engineering run so integration complications are not expected, but the engineering run could reveal unexpected issues with pickup or grounding associated with DAQ connections that would require correction prior to the complete HFT operation.

The proposed engineering run will test software for detector alignment through tracking so that good working software is available at the start of operation of the complete HFT detector system. The engineering run will be an important time for commissioning this software as well as other software systems such as slow controls and various diagnostic software tools. There are many

such functions that will require testing and correction that can be accomplished only through actual operation. Experience has repeatedly and painfully shown that bringing up a new detector system in a collider environment is a daunting task with many time conflicting activities which are still all essential to proper operation. It is important to recognize this and design an engineering run to provide an ordered approach to commissioning the detector.

The limited detector coverage necessary for the engineering run is being configured to provide some capability for D meson detection so there is some hope that some physics can be accomplished, but the overriding goal of the engineering run will be system verification and correction.

3.3. The Intermediate Silicon Tracker

3.3.1. Introduction

The Intermediate Silicon Tracker (IST) consists of a barrel of approximately 0.4m^2 of silicon pad sensors at a radius of 14 cm. The sensors are supported by 24 carbon fiber ladders, which are tiled for maximum hermiticity. Figure 31 shows a Solid Works model of the IST. Table 8 provides the most relevant specifications.

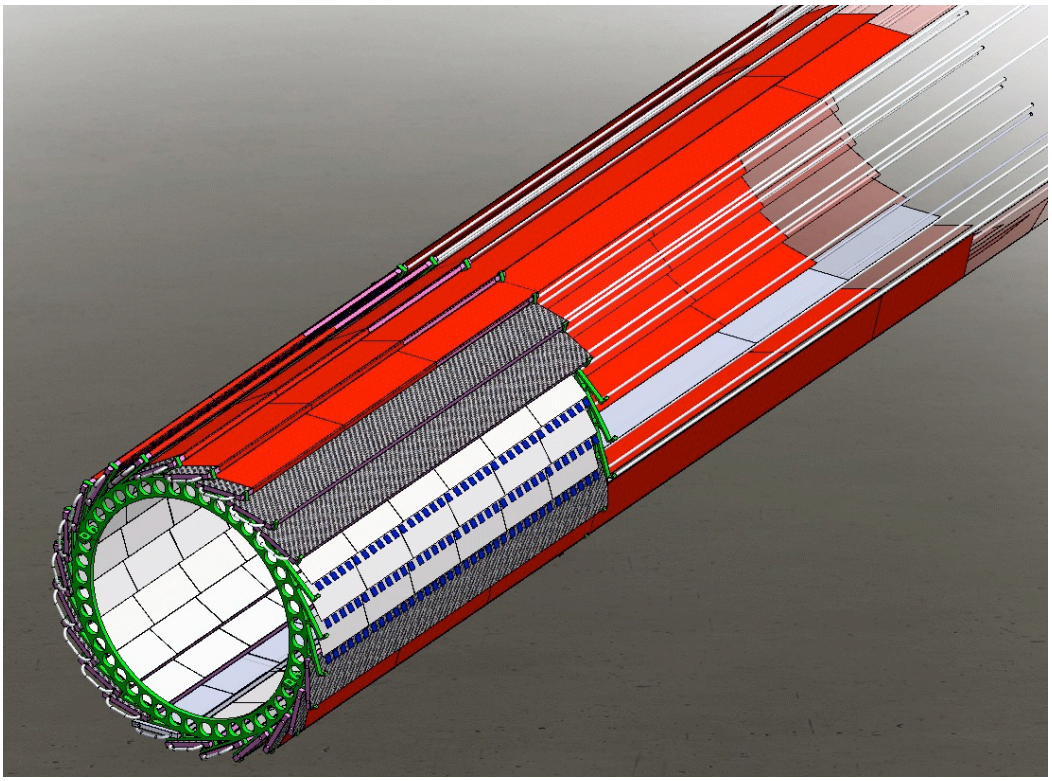

Figure 31: SolidWorks model of the IST.

Together with the Silicon Strip Detector (SSD) the IST provides the intermediate space points that tie the tracking of the Time Projection Chamber (TPC) and both PIXEL layers together. The best figure-of-merit for the total Heavy Flavor Tracker tracking capabilities is the final D^0 reconstruction efficiency. Determining this efficiency involves extensive GEANT simulations and analysis. However, for the IST and the SSD, it is sufficient to optimize these layers for high HFT+TPC single track reconstruction efficiency. How IST and SSD work together with the PIXEL layers and TPC to reconstruct single tracks is a major ingredient for the final D^0 reconstruction efficiency. However, the actual D^0 reconstruction is the sole task of both PIXEL layers. To optimize the HFT single track efficiency a fast simulation framework was used to determine the optimum radius of the IST barrel and the internal geometry of the silicon pad sensors.

The IST has to be fast enough to work together with other, sometimes already existing, STAR detectors. It should also be able to function properly still after being irradiated during its projected lifetime. Section 3.3.2 describes the constraints on the IST by the experimental requirements and the subsequent hardware choices.

Radius	14 cm
Length	50 cm
ϕ-Coverage	2π
$\|\eta\|$-Coverage	≤ 1.2
Number of ladders	24
Number of hybrids	24
Number of sensors	144
Number of readout chips	864
Number of channels	110592
R-ϕ resolution	172 μm
Z resolution	1811 μm
Z pad size	6000 μm
R-ϕ pad size	600 μm

Table 8: Specifications for the IST.

Sections 3.3.3. through 3.3.8 give an overview of the chosen hardware components. The readout and slow controls are described in Section 3.3.9. Since the IST is part of an accurate tracking device its internal and external spatial alignment are discussed separately in Section 3.3.10.

3.3.2. Requirements

The most relevant experimental constraints are data taking rate capabilities, radiation levels and material budget. The data rate and radiation levels are constrained by the RHIC environment and have to be taken into account in the sensor and readout chip choice. The material budget is connected to the tracking capabilities of the inner tracking system, but has also a large impact on the capabilities of more outward located detectors and their associated physics programs. The requirement to design a low mass IST with sufficient mechanical rigidity has led to the choice of state-of-the-art materials. The IST should be able to operate without significant event pile-up for 200 GeV Au+Au collisions. Therefore, the IST has to be able to resolve interactions from each beam bunch crossing which are occurring every 107 ns. The spin program at RHIC relies on individual beam bunch crossings to set and determine the relative spin orientations of colliding proton beams. The IST has to be able to resolve individual beam bunches.

The intrinsic resolution of the IST is required to provide sufficient pointing accuracy to both PIXEL layers. This is more critical in R-ϕ compared to the Z direction. A resolution at the level of 200 μm in the R-ϕ plane will provide the needed pointing accuracy as discussed earlier.

Extrapolating the radiation doses received by the RHIC experiments during the past RHIC operations, it is expected that the total radiation dose for the IST barrel will not exceed 30 kRad per year. Both the silicon sensors and the readout chips on the hybrids are required to be fully operational after 10 years of operation. The mass requirements for the IST are defined by the heavy ion physics requirements in the mid-rapidity region and by the W-boson spin physics program for more forward rapidities. In order to reduce the amount of multiple Coulomb

scattering to be comparable to the intrinsic detector resolution the thickness of the IST layer has to be less than or equal to 1.5% of a radiation length.

Readout Chips

The APV25-S1 chip was chosen for reading out the IST sensors because it meets the requirements and is readily available. This readout chip was developed for the CMS silicon tracker, which is using about 75,000 of these chips. The radiation hard production process of the APV25-S1 will enable it to withstand at least 2 orders of magnitude more in radiation load compared to what is expected to be accumulated during the lifetime of the IST. The chip is fast enough to handle the RHIC interaction clock, even with multiple interactions during p+p running. Moreover, the chip is already used successfully for reading out the COMPASS triple-GEM detectors and will also be used to read out the STAR Forward GEM Tracker (FGT).

Hybrids and Ladders

To meet the requirement of the IST to have on average a thickness of less than 1.5% X_0, special attention has been paid to the choice of materials for the hybrids, cables and ladders. For the cables Kapton with copper conductors was chosen. Although aluminum conductors would make the cables even lighter, they also would make them more difficult to produce and much more fragile. The radiation length requirement made it not desirable to use a ceramic substrate, like AlN, for the hybrid. A 500 μm thick AlN substrate would already contribute 0.6% X_0 while being extremely fragile. A 250 μm thick G10 substrate would only add 0.13% X_0, but still the Kapton cable would have to be connected to this hybrid. Manufacturing the hybrid and cable out of one piece of Kapton circumvents connection problems and is an elegant solution. Since the 50 μm thick Kapton is not self-supporting it is laminated directly to the carbon fiber ladder.

A honeycomb carbon fiber structure with carbon fiber skins is used for the IST ladders. These use the same construction techniques and profit from the ATLAS silicon tracker upgrade. They add about 0.4% X_0 to the IST layer, including liquid cooling. Copying the ATLAS design in the same facility greatly reduces the engineering effort and cost of the IST ladders. Also, since the IST ladders are only half the length (50 cm) of the ATLAS ladders, the design is conservative with respect to strength and gravitational sag.

Cooling

The nominal heat dissipation for the IST is 11 W per ladder, 264 W for the whole system. Although an air cooling system probably would be able to cool the IST, a liquid cooling system is able to perform this function in a more consistent way. A liquid cooling system adds at most 0.2% X_0 to the system.

Readout System

The Forward GEM Tracker is also using APV25-S1 readout chips. This system will be operational 2 years before the IST. In order to reduce the electronic engineering effort and to unify as many STAR readout systems as possible, the IST will use as much as possible of the FGT readout system. The design of the FGT readout system was made such that it can be used also for the IST with as few alterations as possible.

3.3.3. Layout

The Intermediate Silicon Tracker is located between the outer layer of the PXL detector and the SSD. The chosen radius of 14 cm has been optimized for single track reconstruction efficiency while keeping the SSD and IST redundancy in mind. The IST barrel covers the full acceptance of the STAR TPC, i.e. 2π coverage for $-1 < \eta < 1$. The actual IST acceptance of $-1.2 < \eta < 1.2$ also leads to a good coverage for collisions that take place 10 cm around the nominal interaction point.

At the highest RHIC energy of 200 GeV for Au+Au collisions the charged particle density at a radius of 14 cm can easily exceed one per cm^2. The silicon sensors are divided into pads such that the occupancy of the individual pads does not exceed a few percent. The occupancy is fully determined by the number of active elements and can be reached by different sensor geometries. What has been taken into account is the double-hit probability within the search area on the IST sensors resulting from the pointing resolution of the TPC and SSD. Figure 32 shows the occupancy of a sensor with 768 active elements and the fraction of hits that are accompanied by one or more hits in the search area. In the case of a silicon strip detector the search area would be defined by the width of the area and the length of the strips. At the chosen radius of 14 cm this would result in more than 10% of the tracks having ambiguous IST hits. For silicon pad sensors this drops to about 1%. The number of active elements is determined by the density, with which the readout chips can be conveniently packed on the hybrids. Silicon pad sensors are well suited to the RHIC environment and proved their suitability in the PHOBOS experiment.

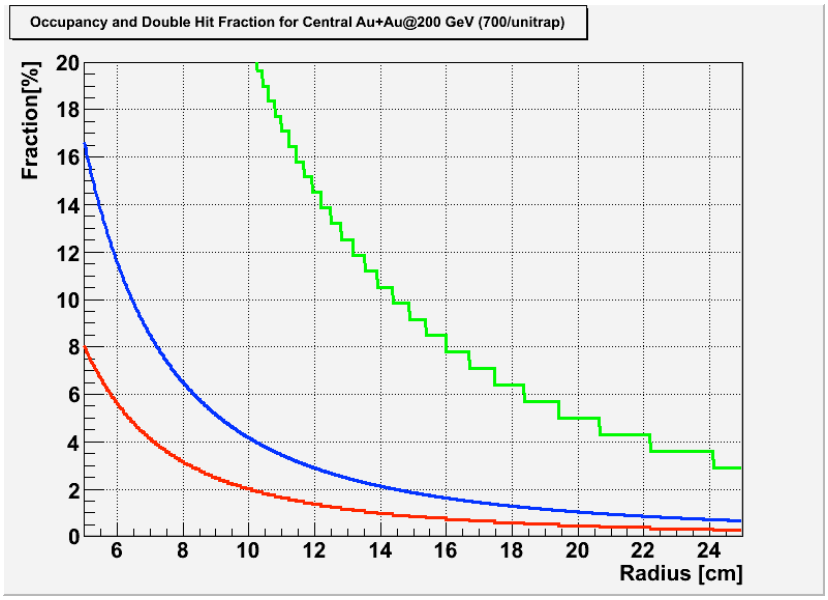

Figure 32: The blue curve shows the occupancy of a silicon sensor with 768 channels, since this is fully determined by the number of channels it is the same for a silicon pad sensor with 768 pads and a silicon strip sensor with the same amount of strips. The green curve gives the fraction of tracks that would suffer a double hit on strips leading to an ambiguous space point. The red curve shows that the same double hit fraction is much less for a silicon pad sensor.

Figure 33 shows a study of the single track finding efficiency of the whole HFT plus TPC as a function of the pad layout of the IST sensors. The better resolution (the size of the pads on the y-axis) is in R-ϕ, the bending plane. From these studies it was determined that 768 channels arranged in strips of roughly 600 µm x 6000 µm provide an efficiency of about 83%. Going to

more channels could give a slightly better efficiency, but would lead to space problems when trying to mount more readout chips on the hybrids. The right plot emphasizes the IST-SSD redundancy by excluding hits from the SSD from the tracking. In this case the single track finding efficiency decreases to 73%. This has to be compared to 50% if the IST would not be there and only the TPC would provide tracking to the PXL. Thus, the IST adds in an essential way to the efficiency and redundancy of the HFT. The efficiency of the whole inner tracking system is determined by an intricate interplay of the detector layer radii, resolutions and thicknesses. Since these characteristics are mostly fixed for the PIXEL system and SSD, varying the radius of the IST barrel for a certain internal sensor geometry makes it possible to optimize the radius with respect to the single track efficiency. Figure 34 shows a calculation of the single-track efficiency as a function of the IST barrel radius. Although the dependence is rather weak it is clear that 14 cm will give the best efficiency while not encroaching on the outer PIXEL layer. Going to a bigger radius would just increase the size and cost of the IST with no single track efficiency gain.

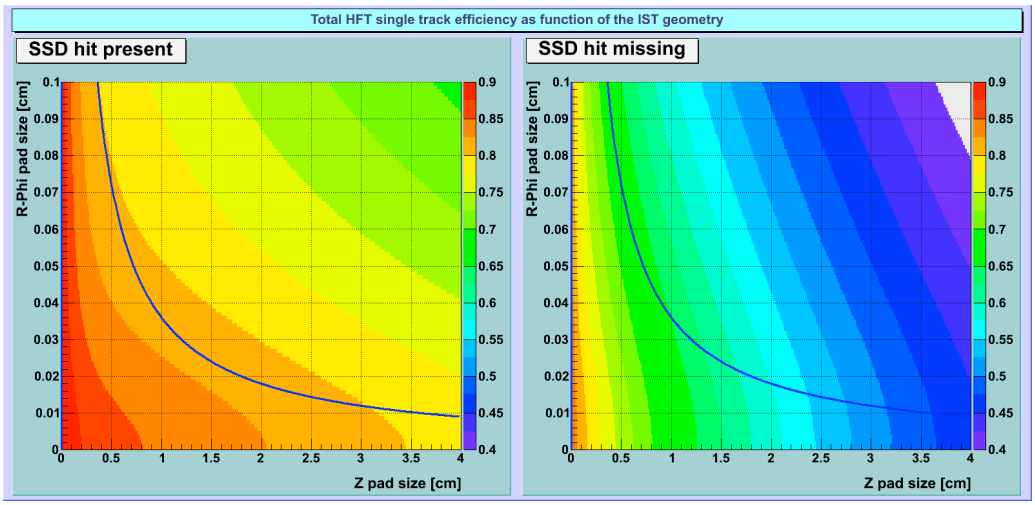

Figure 33: Single track finding efficiency for different R-ϕ and Z pad sizes of the IST. The solid line shows an iso-line for 768 readout channels. The left panel shows the efficiency when hits from the SSD are included. In the right panel the SSD hits are not included in the track. Particles tracked are kaons at 750 MeV/c.

3.3.4. The Silicon Pad Sensors

The manufacturing techniques for silicon sensors are well established and are mastered by several manufacturers. The preference is to produce single sided devices with p-implants on n-bulk silicon using poly-silicon resistors. Such sensors are relatively easy to produce with high yield and can also be handled without much difficulty in a standard semiconductor lab. In contrast, double-sided devices have a lower yield (thus more expensive) and need special equipment to handle them.

Figure 35 shows the internal layout of the IST silicon pad sensors. The active elements are arranged in such a way that the best resolution is in the bending direction, i.e. R-ϕ. Along the beam direction, the resolution will be ten times larger. The sensors will be roughly 7.7 cm x 4 cm with 768 channels. All channels are AC coupled and connected through a second metal layer to bonding pads on one long edge of the sensor. From the manufacturing point of view this design

is reasonably standard. Preliminary discussions with Hamamatsu showed that they are able to produce such sensors within the proposed budget.

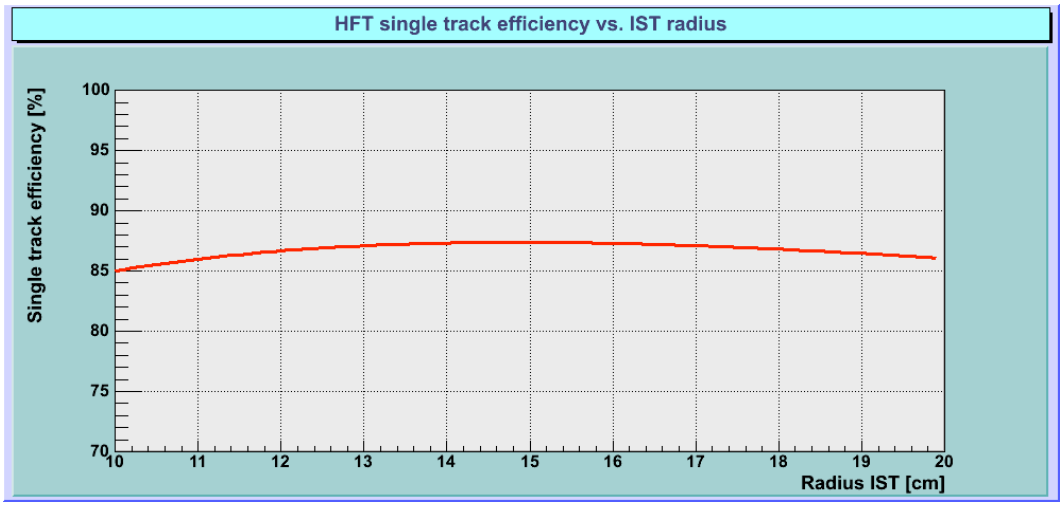

Figure 34: Single-track efficiency as a function of the IST barrel radius. The assumed internal sensor geometry was 600 μm in R-ϕ and 6000 μm in Z.

Hamamatsu is the preferred vendor because of their excellent track record with respect to the quality of their produced sensors. This will greatly reduce the amount of quality control that has to be performed for these sensors. It will be sufficient to fully measure the characteristics of one or two samples per produced batch of about 20 sensors. Moreover, Hamamatsu uses special design rules, which make their sensors radiation hard. Therefore, we foresee no performance degradation during the expected IST lifetime.

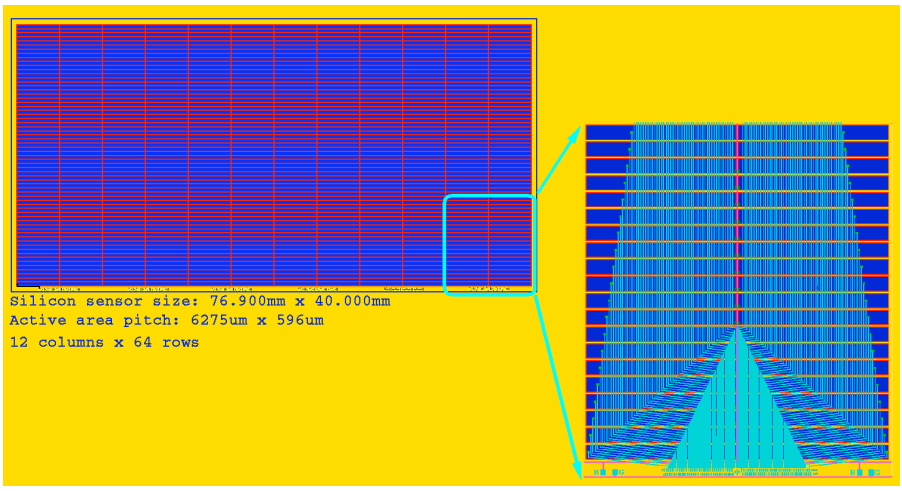

Figure 35: The silicon pad sensor internal layout.

3.3.5. The Readout Chips

In total 110,592 channels are being read out in the IST. Readout chips with the necessary requirements for this system are already being used for similar purposes by other experiments.

We chose the APV25-S1 readout chip. Each channel of the APV25-S1 chip consists of a charge sensitive amplifier and shaper whose output signal is periodically sampled at up to 40 MHz (the LHC interaction rate). The samples are stored in a 4 μs deep analog pipeline. Following a trigger, the data in the pipeline can be processed by an analog circuit, mainly de-convoluting the amplifier response from the actual signal and associating the signal with a specific bunch crossing. The resulting analog data can then be multiplexed and sent to digitizer boards. Although the analog data lead to higher data volumes at the front-end, it is an advantage that charge-sharing between strips and common mode noise can be studied in detail, which greatly improves the understanding and performance of the detector. The equivalent noise charge (ENC) of the APV25-S1 depends on the capacitance of the strips and the de-convolution algorithm used. For our purposes, the noise is better than 2000 electrons. With 300 μm thick silicon sensors this will give a signal-to-noise ratio of better than 11:1 based on the most probable energy deposition by a minimum ionizing particle (MIP). The nominal power consumption of the APV25-S1 chip is 2.39 mW per channel, i.e. about 0.3 W per chip. The chips are fabricated in a radiation hard deep sub-micron 0.25 μm process.

3.3.6. Hybrids and Modules

Figure 36 shows the Kapton IST hybrid design with 6 sensors and 36 APV25-S1 readout chips. For clarity the part that constitutes the readout cable and which extends further to the right is not shown. Both hybrid and cable are about 70 μm thick and are directly laminated to the front and back of the ladder, respectivily. The radiation lengths of sensors, readout chips, hybrid and carbon fiber ladder add up to about 1% X_0. The readout chips are grouped in 3 sections of 12 chips, i.e. serving 2 sensors. Since also the power for sensors and readout chips is divided in the same way, the ladder consists of 3 electrically independent parts reducing the chance of a whole ladder failing.

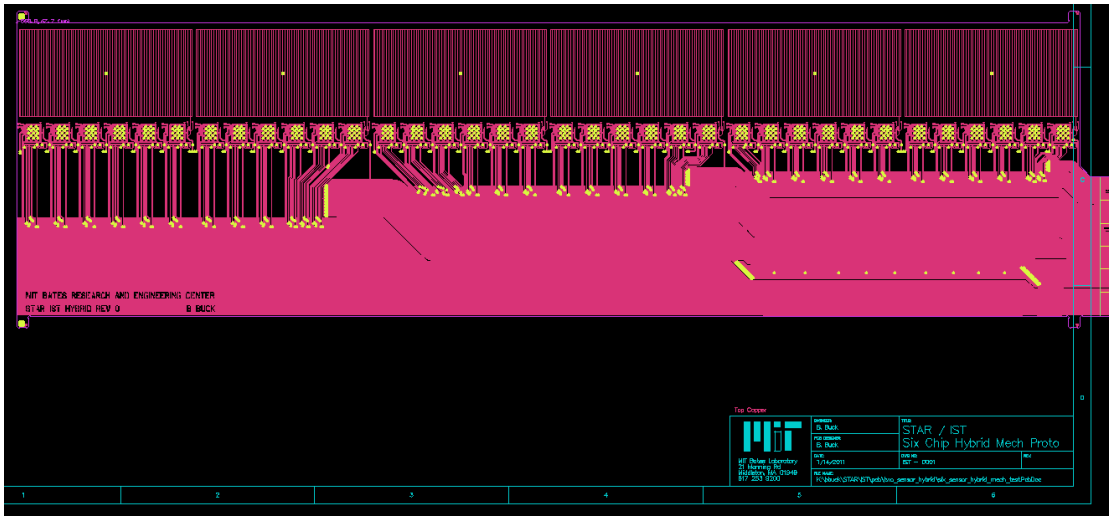

Figure 36: Kapton IST hybrid design.

A more detailed mechanical drawing of one such section is shown in Figure 37. There is a gap of 400 μm between the sensors. Overlapping the sensors would lead to complications in the assembly process. These acceptance gaps are compensated because of the redundancy between the SSD and IST. Since the cable is folded over to the backside of the ladder the cable does not obscure visual access to the modules, which is needed for spatial survey purposes and inspection.

Figure 38 shows a prototype Kapton hybrid design with an integrated long Kapton cable. Both hybrid and cable are about 70 µm thick. For this prototype four PHOBOS Inner Vertex sensors were used because there were no IST prototype sensors available yet and because the PHOBOS sensors are very close to the sensors used in the IST. The PHOBOS sensors are silicon pad sensors with 512 active elements per sensor, the elements are AC coupled to the second metal signal traces that connect to the bonding pads. To ensure mechanical rigidity the Kapton hybrid was laminated to a 500 µm thick carbon-carbon substrate. Power, control and readout connections were wire bonded to the hybrid. Figure 39 shows the raw readout signal from the prototype, the four raised areas with APV pedestal signals can easily be distinguished. The spikes in between the APV areas are the tick marks of the APV heartbeat. The signal from 500 events at full depletion sensor bias was aligned in time, pedestal and common mode noise corrected and plotted in Figure 40.

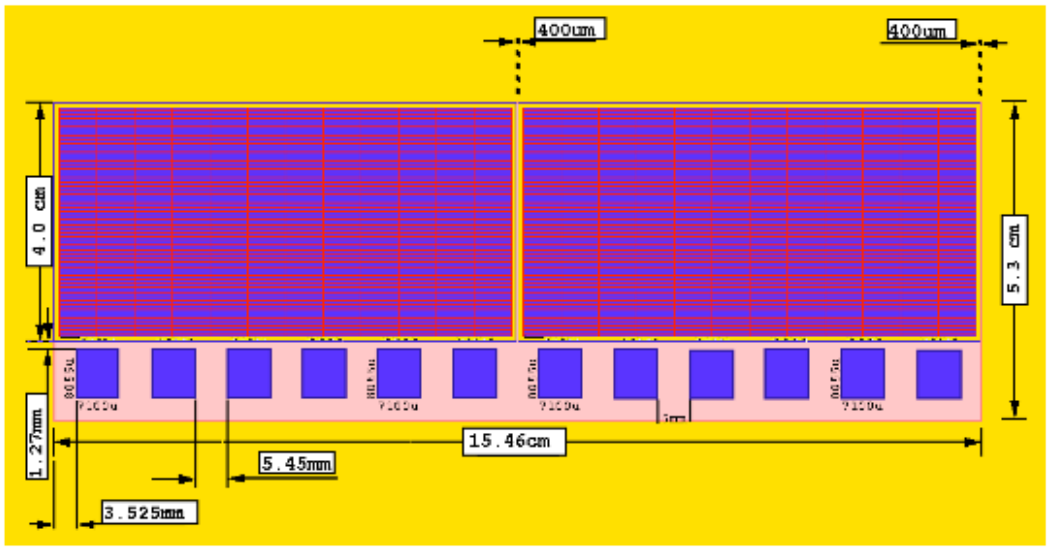

Figure 37: Layout of an IST module.

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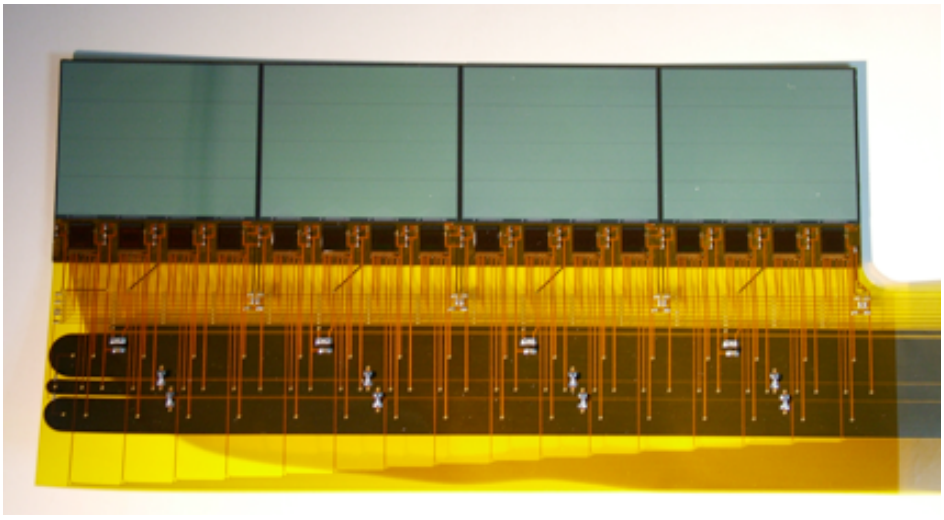

Figure 38: IST prototype with 4 PHOBOS IV sensors and 16 APV25-S1 readout chips.

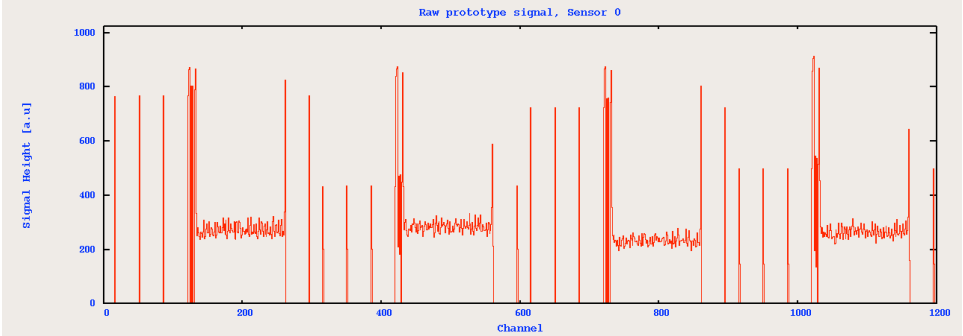

Figure 39: Raw signal from the IST prototype. Shown is the first bank of 4 APV readout chips which correspond to one sensor of 512 channels being read out.

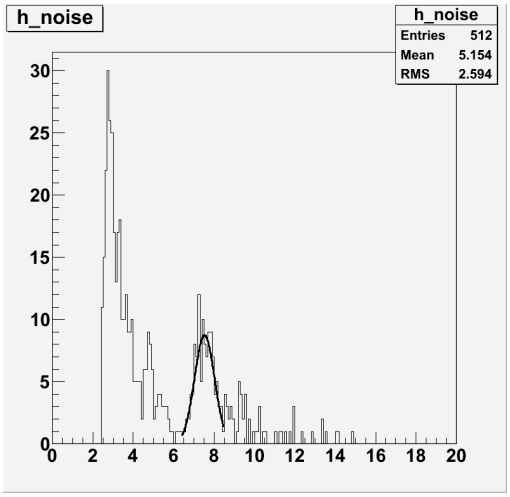

Figure 40: Signal plot from analyzing 500 pedestal events at full depletion voltage.

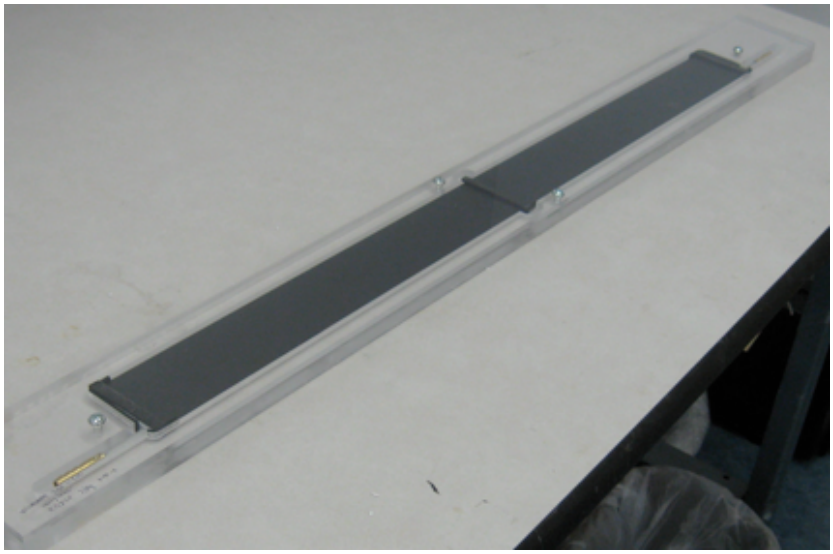

Figure 41: Long IST prototype ladder made out of carbon fiber honeycomb and carbon fiber skins. This prototype has one cooling channel.

3.3.7. Mechanical Support Structure

The IST barrel will consist of 24 ladders, which are mounted on a carbon fiber support cylinder. This Middle Support Cylinder (MSC) is described in Section.

The ladders are a shorter version of the staves under development for the ATLAS tracking upgrade. Because they are shorter they are even more rigid than the ATLAS staves and it is expected that their midpoint sag will be less than 100 μm when only end supports are used. A prototype ladder has been produced, as shown in Figure 41, and is being tested.

A more detailed cross-section of the ladder and mounted modules can be found in Figure 42. This design shows the 300 μm thick silicon sensor, the 300 μm thick APV25-S1 readout chip, the 100 μm thick Kapton hybrid-cable, the 500 μm thick carbon-carbon substrate and the 5 mm thick carbon fiber ladder with cooling tube. It also shows nicely how the Kapton hybrid folds over to the backside of the ladder where it is routed out to the readout system.

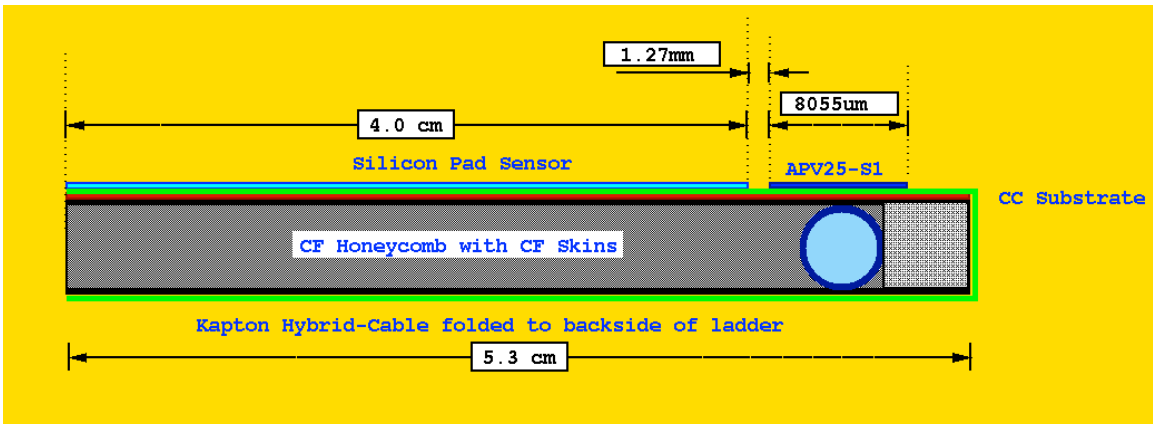

Figure 42: Cross-section of the ladder and modules. The Kapton hybrid shown in green is folded over to the backside.

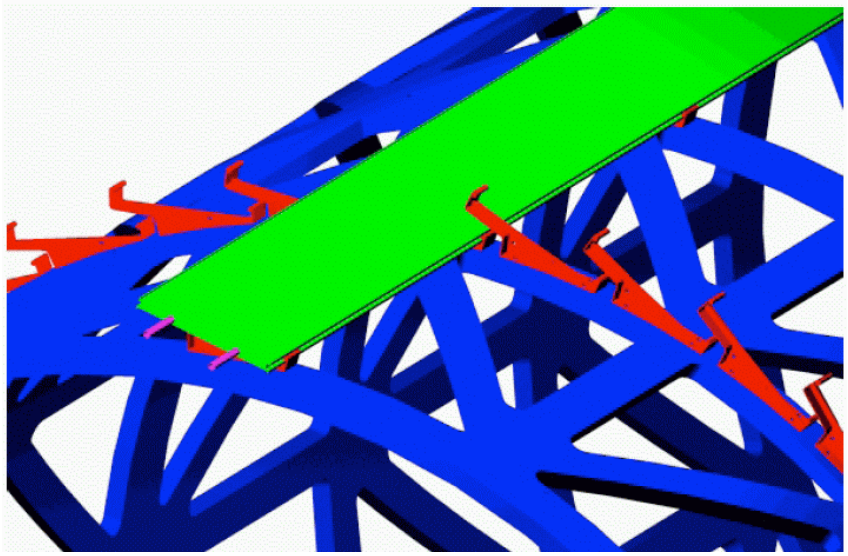

Figure 43: Ladder 'clip' mounting of the IST ladders onto the supporting cylinder (ISC).

The ladder mounting scheme follows the ATLAS upgrade design efforts. Figure 43 shows a schematic impression of the ATLAS mounting scheme. Here the ladders are mounted with clips on the MSC. Because of the shorter length of the IST ladders it is sufficient to use endpoint supports only. One end of the ladder would be kept fixed while the other end allows thermal expansion. A prototype of this clip-on design has been prepared, as shown in Figure 44, and is currently under investigation.

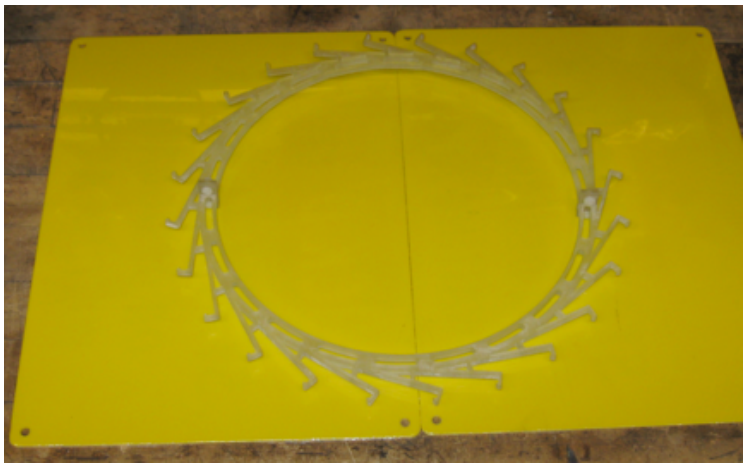

Figure 44: Rapid prototype of the IST ladder mounting structure.

The mechanical support structure will be manufactured with an overall accuracy of 100 μm. Locally, the structure supporting the IST requires an accuracy of less than 100 μm. For instance, the mounting surfaces of the sensor modules will have to be flat to within 50 μm to avoid stress on the sensors.

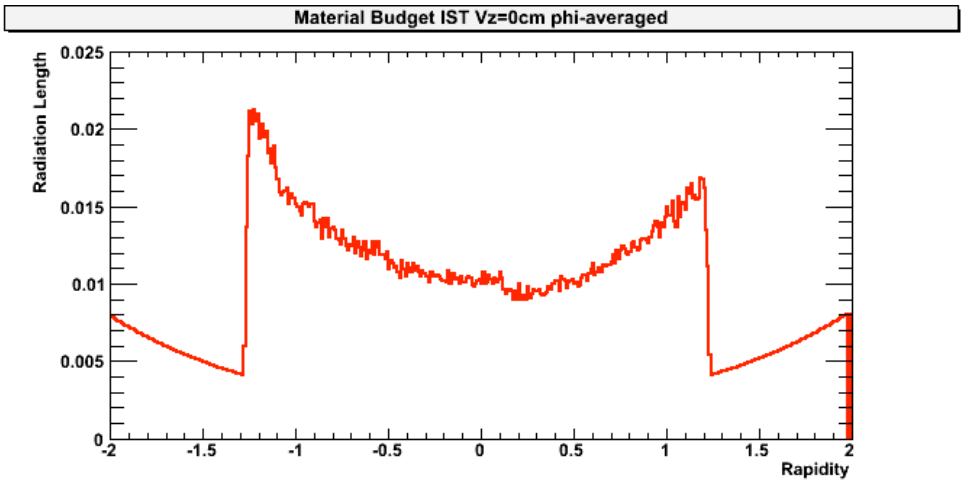

Figure 45: Phi averaged material budget for the IST as a function of rapidity.

Figure 45 provides a realistic estimate of the IST material budget by describing ladder and module designs in a GEANT geometry. These results were obtained by propagating 100,000 geantino events through the IST geometry using GEANT 3.21/08. The material budget at mid-rapidity is well below the required 1.5% X_0. The MSC and support clips where not included in

this calculation. The Kapton readout cables only running in the negative rapidity direction causes the asymmetry in the material budget.

3.3.8. Cooling

The only source of dissipation on the ladders is due to the 36 APV25-S1 readout chips. Although the nominal power consumption is about 300 mW per chip, the final power consumption depends on the capacitance of the attached sensor channels and consequently the optimal settings of the chip parameters. For safety margin a maximum dissipation of 550 mW per chip is assumed. This leads to a maximum dissipation of about 20 W per ladder and thus 375 W for the whole IST barrel. Trying to cool this with air only was considered too daunting and liquid cooling channels were incorporated in the ladder design. The power dissipation of 20 Watt per ladder leads to about 0.8 mW per mm^2 dissipation if the heat would spread out isotropically. The placement of the cooling tube directly under the readout chips makes the cooling of the ladders manageable with a room temperature cooling system. The cooling system was designed according to the specifications in Table 9. The maximum temperature of the readout chip guarantees acceptable noise levels. The inlet temperature is kept at 24˚C, which is the same nominal temperature as of the STAR TPC inner filed cage and avoids condensation concerns. Since the cooling lines will be of thin walled aluminum the pressure has to be kept low. The low fluid velocity minimizes vibrations in the IST system.

Maximum readout chip temperature	35˚C
Cooling fluid velocity	0.3-3 m/s
Maximum pressure	0.2MPa
Cooling fluid inlet temperature	24˚C

Table 9: Cooling system specifications for the IST.

Novec 7200 was chosen as the coolant. This fluid evaporates quickly in the event of a cooling leak and the vapors will not add to the ozone layer depletion. The vapor is also non-flammable and non-toxic in this application. Simulations making use of FloWorks and SolidWorks (Figure 46), showed that cooling two IST ladders in series was able to satisfy the required specifications.

Table 10 summarizes the results. Cooling two ladders in series has the advantage that it reduces the amount of cooling lines that service the IST. These cooling services have to pass through an area which is already crowded with readout cables. Another advantage is that there is no need for a cooling return line within a ladder, thus lowering the material budget per ladder. Investigations into the possibility of cooling 4 ladders in series are still ongoing. This would limit the amount of services even further. Table 10 shows that there is still enough headroom to increase the flow rate which makes it likely that also cooling 4 ladders in series is feasible. This is exemplified in Figure 47 which shows that acceptable flow rates result in acceptable readout chip temperatures even when 4 ladders are cooled in series.

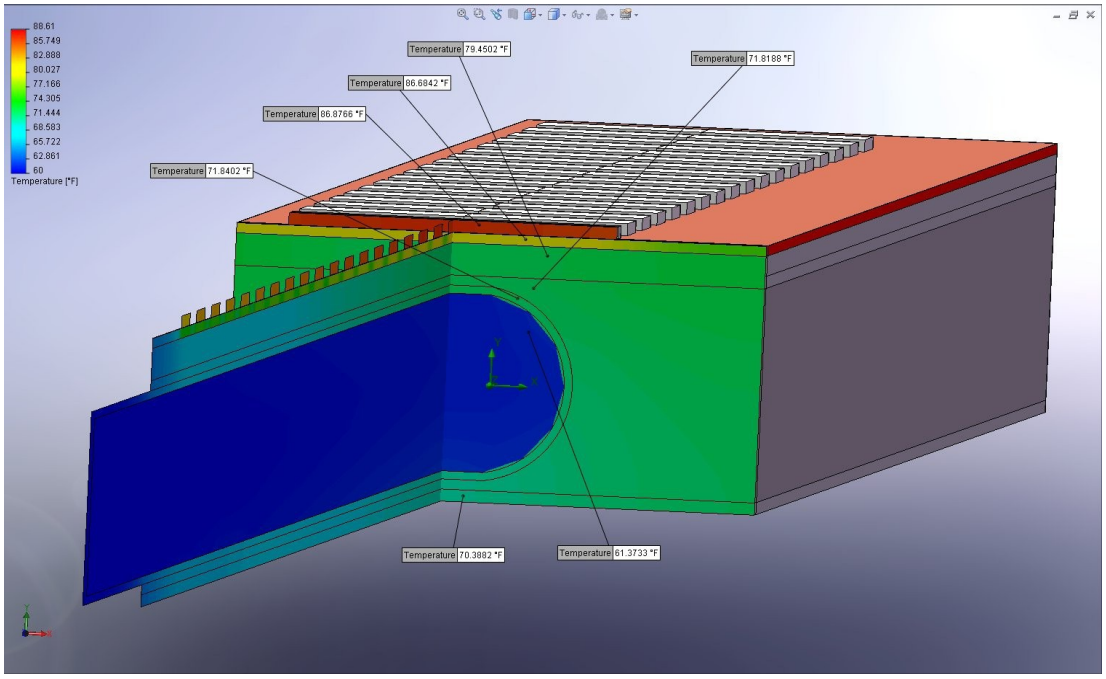

Figure 46: FloWorks simulation of a liquid cooled IST ladder.

Figure 47: Temperature of chips and cooling fluid as a function of the flow rate of the cooling fluid.

Cooling fluid	3M Novec 7200
Cooling fluid speed	1m/s
Maximum pressure	0.14MPa
Calculated maximum temperature of readout chip	34.9˚C

Table 10: Summary of the couling test results for two IST ladders in series.

3.3.9. Readout System

Figure 48 shows the schematic of the IST readout and slow controls system. The 24 IST ladders are connected in 6 groups of 4 ladders to 6 Transition Boxes (T-Box) located on the inside of the East STAR TPC wheel just outside of the inner field cage. The T-Boxes will house the voltage regulators and combine the bias voltages from the Bias Supply cables with the cables coming from the readout crates.

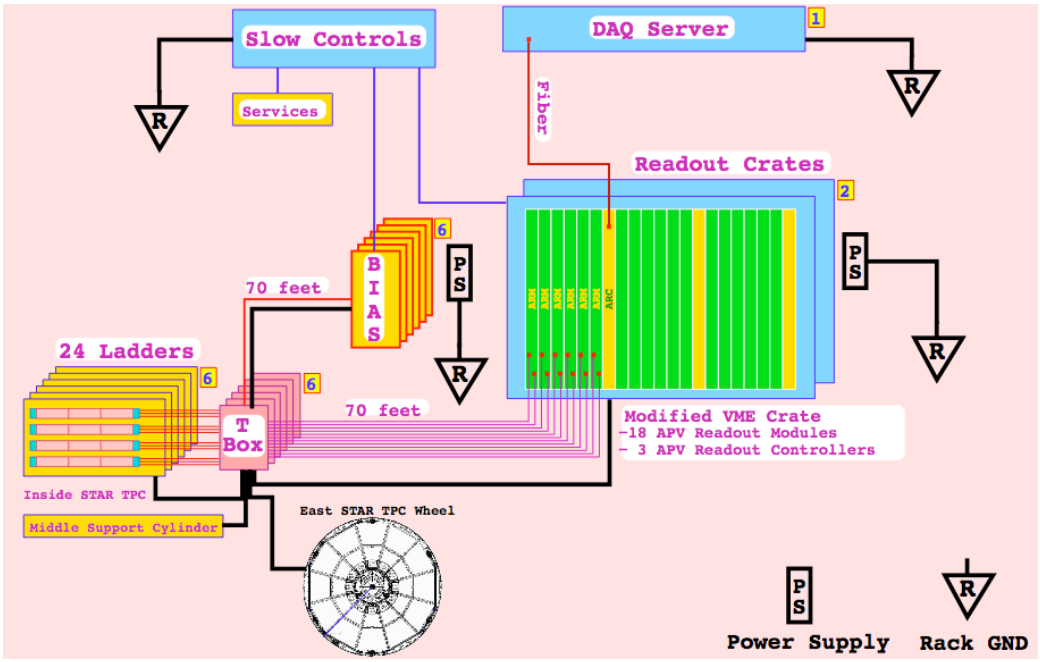

Figure 48: IST Data Aquisition block diagram. Also shows the IST grounding scheme.

Two customized Wiener VME readout crates will house the 36 readout boards (ARM) and 6 crate controller boards (ARC). The boards are of standard 6U x 220 mm size; the crate interconnects these boards with standard 7-slot passive CPCI backplanes and provides integrated low noise 5 V power supplies. The crate will be mounted on the south electronics platform next to the STAR detector. Each ARM handles two detector cables (24 APV chips), providing an ADC, data buffering and control of APV chip triggering and readout sequencing. The APV chip sample clock is 37.532 MHz, phase-locked to the RHIC bunch crossing (9.383 MHz). This stable timing ensures stable effective gain without the necessity of a timing correction. The ARM also provides the I_2C slow controls interface and isolated low-voltage power supplies to the T-Boxes. Since the analog IST signals run over a 70 feet cable to the readout crates, see Figure 49, special

precautions have to be taken to provide the best signal-to-noise ratio. Figure 50, Figure 51, and Figure 52 show the APV signal after it has passed through 70 feet of cable, after an equalizing filter and the obtained resolution with the filter. These results were obtained with a relatively simple test setup, but show that with proper filtering the signal-to-noise ratio is not limited by the long cable. More eleborate tests with the interface prototypes of the ARM readout boards are ongoing.

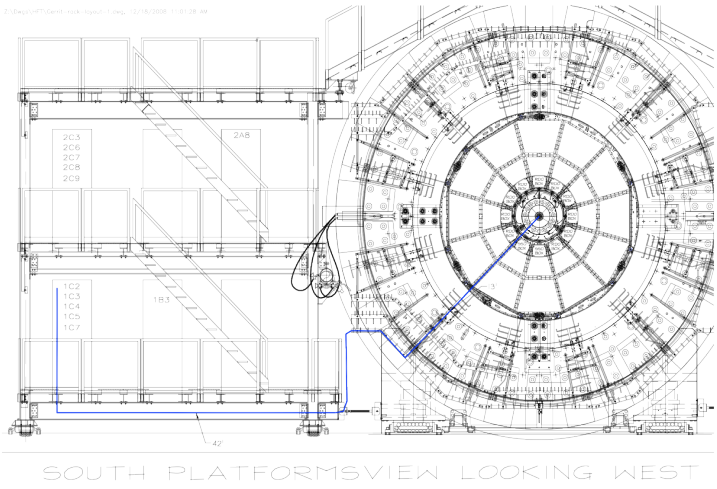

Figure 49: IST cable run in STAR from the inner field cage to the readout crates in their rack.

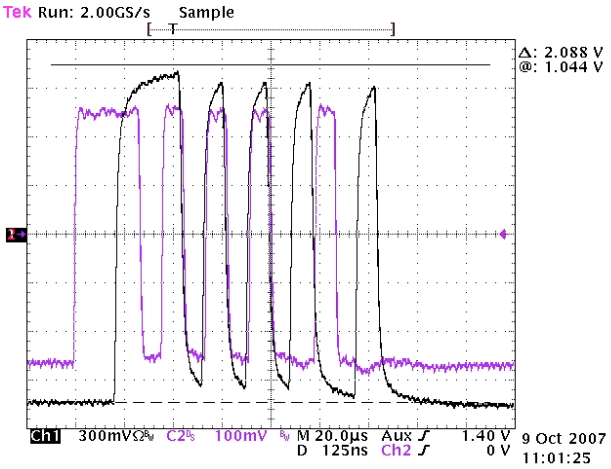

Figure 50: Unequalized APV signal after 70 feet of cable.

The ARC interfaces to the STAR trigger and to STAR DAQ via the ALICE Detector Data Link (DDL) Source Interface Units (SIU), the standard for all new STAR DAQ-connected developments for the DAQ1000, Time of Flight (TOF), Barrel (BTOW), Forward GEM Tracker (FGT) and Endcap (ETOW) tower level 2 upgrade. The readout system can buffer up to 4096 events (the maximum number of outstanding events in STAR) and therefore decouples the IST dead time from the data acquisition system, providing a simple fixed dead time. The dead time depends on operating configuration but will typically be 11 µs, with a maximum of 26 µs. A Linux box will be located in the STAR DAQ room and fitted with the ALICE DDL receiver boards and a Myrinet interface to the event builder computer.

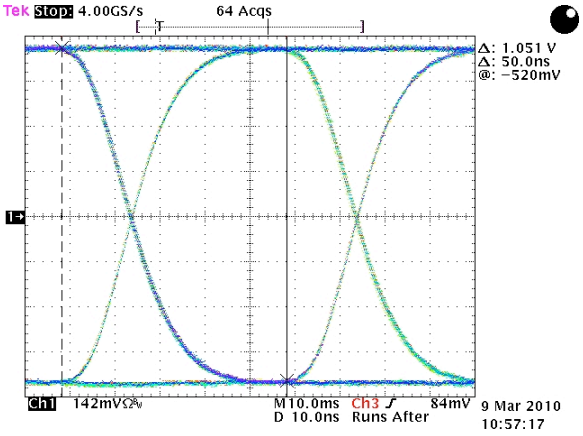

Figure 51: APV signal after 70 feet of cable and an equalizing filter.

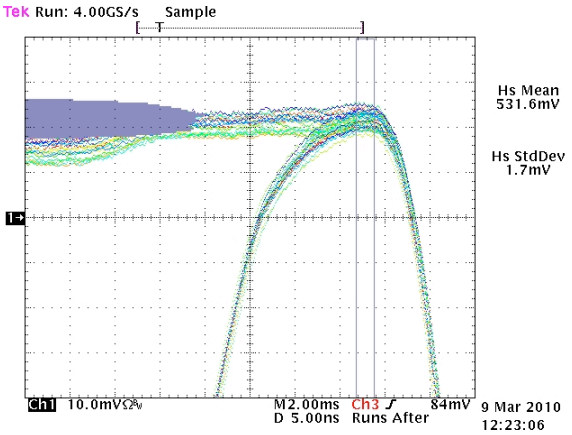

Figure 52: The resolution of the APV signal after the equalizing filter.

The slow controls system will serve as the primary means for controlling and monitoring the working parameters of the IST. The hybrid temperature, currents, voltages, cooling system flows and cooling system temperatures will be interfaced with the standard STAR alarm system. The alarm system logs the parameter history and alerts the shift crew if soft operating limits are exceeded. Immediate shutdown of the IST system will take place if safe operation is compromised.

The black dashed lines in Figure 53 show the communication flow between the slow controls computer and the hardware being controlled. The red solid lines represent the actual hardware connections, which allow this communication. The slow controls for the IST detector and readout crates will be handled exclusively by Ethernet traffic to the IST Linux box, through the ALICE DDL link to the readout crates, and then finally through the RDOs to the APV's via the local I_2C link. There will be no other hardware needed for slow controls. All power supplies will be fitted with an Ethernet controls interface.

The main grounding point of the system will be at the T-Boxes which will be grounded to the Aluminum of the East TPC wheel. This will provide a signal ground for the IST hybrids, but also a ground for the carbon-fiber ladders and the carbon fiber support cylinder. This signal ground

will also be fed to the readout crates and bias supplies. The power supplies of the readout crates, bias units, DAQ server and Slow controls will use clean rack grounds.

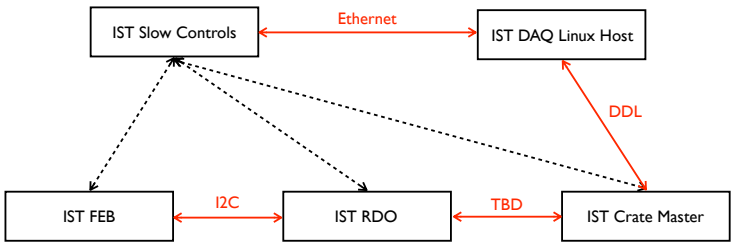

Figure 53: IST slow controls flow diagram.

3.3.10. Spatial Survey and Alignment

The IST will have to be aligned with respect to other detector subsystems of the inner tracking upgrade, PXL and SSD. The final alignment will be done with tracks through an iterative residual method. However, for this method to be successful it is important that the positions of the active elements are known in advance with an accuracy comparable to the resolution of the detectors. A careful plan can achieve this.

The positions of the sensors on the module have to be determined. Internally the structure of the sensors will be known with an accuracy of about 1 to 2 μm. This information is obtained through the production mask drawings of the sensors and accessed through alignment marks on the sensors. The modules will be built on an assembly machine under control of an operator checking the process under a microscope. The expected placing accuracy is 5 μm. After the modules have been assembled they can be surveyed with an optical survey machine at MIT. The accuracy of this machine is about 10 μm in-plane. An out-of-plane contrast measurement leads to an accuracy of 50 to 100 μm.

The same methods will be used for the ladders. Three modules will be glued to one ladder with an accuracy of about 5 μm. Then the ladder will be optically surveyed with an in-plane accuracy of 10 μm and an out-of-plane accuracy of 50 to 100 μm. After the ladder is approved it will be shipped to BNL where an additional survey will take place.

At BNL the ladders will be put together in two clamshell cylinders that can be measured on a coordinate measuring machine. After the clamshells have been put together on the ISC to form the IST barrel another survey needs to take place. Up to this point it should be possible to survey the silicon sensors themselves. The sensors have the highest internal accuracy (1 to 2 μm) and in the end it is their position, which should be known with the best accuracy. However, after the clamshell has been closed visual access to the sensors will become impossible, especially after the ISC gets integrated with the rest of the inner tracking system. It is important to have survey points on the ladders, the clamshell structure and the ISC, which are visible to the BNL survey group. These survey points then 'anchor' the IST inside the inner tracking system and finally to the whole STAR detector.

3.4. The Silicon Strip Detector

The SSD[24] is a high-resolution, double-sided silicon strip detector that is mounted at a radius of 22 cm. Its radial location puts it midway between the event vertex and the first active row of the TPC. Thus, it is ideally suited for the purpose of improving the TPC's pointing and momentum resolution.

The SSD was designed to work with the TPC and the STAR Silicon Vertex Tracker (SVT). The design readout frequency of the existing SSD is 300 Hz. This does not meet the HFT readout frequency requirement of at least 1 kHz. Therefore, the readout electronics needs to be upgraded. To achieve the new speed requirement, the existing silicon detector wafers and the ladder structure are kept and a significant amount of the electronics are replaced. The upgrade also requires new cabling, cooling, and mounts. Table 11 shows the relevant parameters of the SSD.

SSD radius	22 cm
SSD length	106 cm
$\|\eta\|$ coverage	< 1.2
Number of ladders	20
Number of wafers per ladder	16
Total number of wafers	320
Number of strips per wafer side	768
Number of sides per wafer	2
Total number of channels	491520
Silicon wafer size	75 × 42 mm
Silicon wafer sensitive size	73 × 40 mm
Silicon thickness	300 μm
Strip pitch	95 μm
Strip length	73 mm
Stereo angle	35 mrad
R-ϕ resolution	20 μm
Z resolution	740 μm

Table 11: Summary of SSD characteristics and performance.

3.4.1. The SSD Barrel

The SSD barrel is composed of 20 individual ladders. The ladders are made of carbon fibre and each ladder supports 16 detector modules. An overview of the assembly is shown in Figure 54. Each of the modules is composed of one double-sided silicon strip detector and two hybrid circuits equipped with analog readout electronics. On both ends of a ladder, two electronics boards are used to read out and control the detector modules and convert the analog signal from the Si wafers into a digital signal, which is then sent to readout boards that are located on the STAR south platform.

One ladder is shown, in detail, in Figure 55. Two cable busses (one per side of the Si sensor) transport the analog signals along the ladder to a pair of ADC boards, where the signals from the

16 sensors are digitized concurrently. After digitization, the signals are sent via optical fiber links to the Readout Boards, which are in turn linked to the DAQ system through optical fibers.

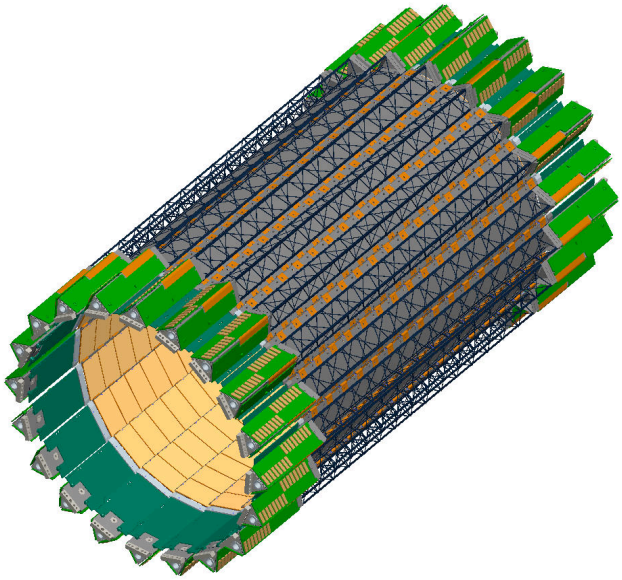

Figure 54: A CAD model of the SSD. The rectangular gold objects in the inside of the cylinder represent the silicon. The triangular structure in the center is the ladder support. The green objects at the end represent the readout electronics (Ladder Board).

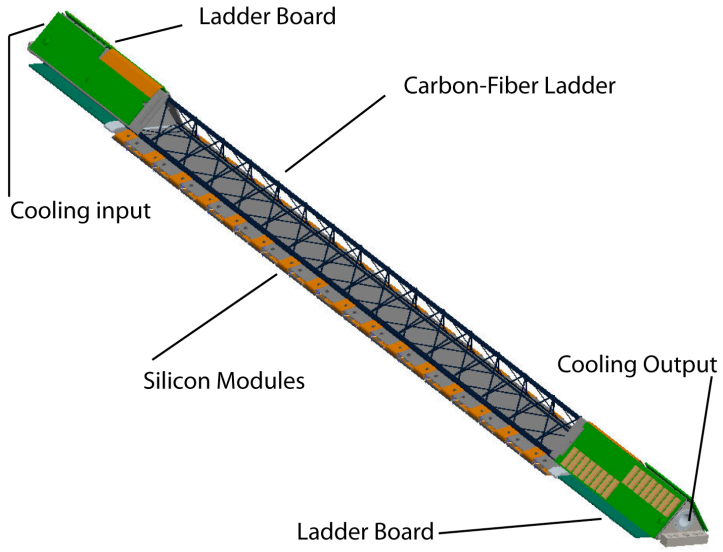

Figure 55: An SSD ladder showing its various components. The Ladder Board contains the electronics that reads out the silicon modules.

A detector module is the basic element of the SSD and it integrates a silicon sensor with its front-end electronics. One detector module is shown in Figure 56. This silicon strip sensor measures 75 mm by 42 mm. It is double-sided with 768 strips on each side of the sensor. The strips have a pitch of 95 μm, and are crossed with a 35 mrad stereo angle between the strips on the P and N side of the silicon. It takes 16 modules to fill a ladder. A Ladder Board at each end reads out one

face of the module. The two hybrid circuits are built on top of a flexible circuit made of Kapton and copper, which are, in turn, glued to a carbon fiber stiffener. The circuitry includes 6 analog readout chips (the ALICE 128C) and approximately 50 components (resistors and capacitors).

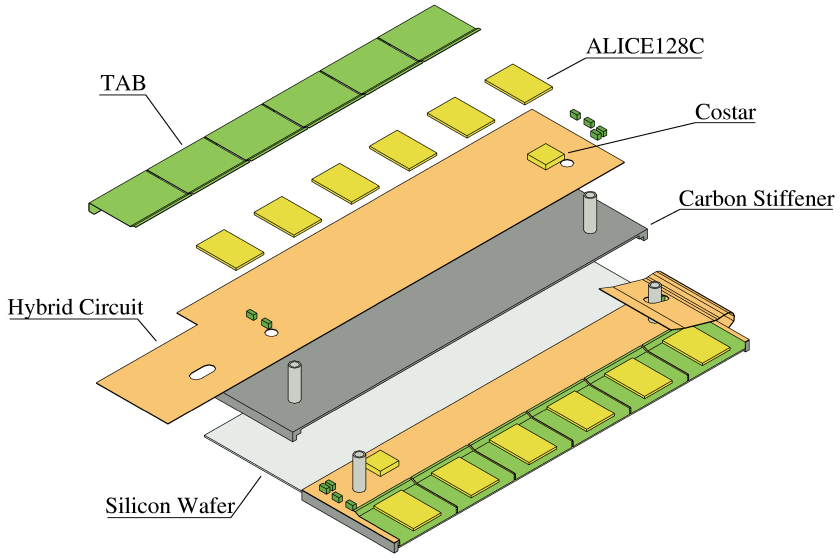

Figure 56: Exploded view of one detector module. The left half shows components and the right half shows the assembled hybrid.

3.4.2. Electronic Upgrade

A Ladder Board reads all 16 detector modules concurrently. Figure 57 shows the block diagram of the ladder board and the RDO Board. The optical connection is bidirectional; the second fiber provides trigger and slow control information to the FPGA on the ladder board, which manages the analog circuitry on the ladder.

Ladder Board

Every module on the SSD ladder has its own ADC, thus 16 ADC channels are needed on each ladder. We use 8 Analog Devices AD7356 dual ADC chips. Each chip contains two independent ADCs with 5 MHz sampling rate and a bit-serial output. The serial output produces a 14-bit pulse train, of which only 10 bits are used in this application. The outputs of these 16 ADC channels are sent to the inputs of a parallel-to-serial converter, along with the slow control output of the FPGA. The parallel signals are clocked in to the serial converter at a 40 MHz rate, resulting in a 1.0 Gb/s pulse train, which is converted to optical signals and transmitted to one of the 5 inputs of the RDO board. The optical nature of this connection allows the RDO crate to be located outside the STAR magnet. A full description of the Ladder Board can be found in a detailed document.[25]

A mechanical prototype of the Ladder Board is shown in Figure 58. The ladder board has three sections connected by a flexible cable. The flex section and the hard sections are made at the same time. When assembled the board is simply folded into a triangle. Both the optical transceiver and the power connector are indicated on the board. The corresponding cables are routed along the Outer Support Cylinder. The picture also shows the board mounted to a ladder.

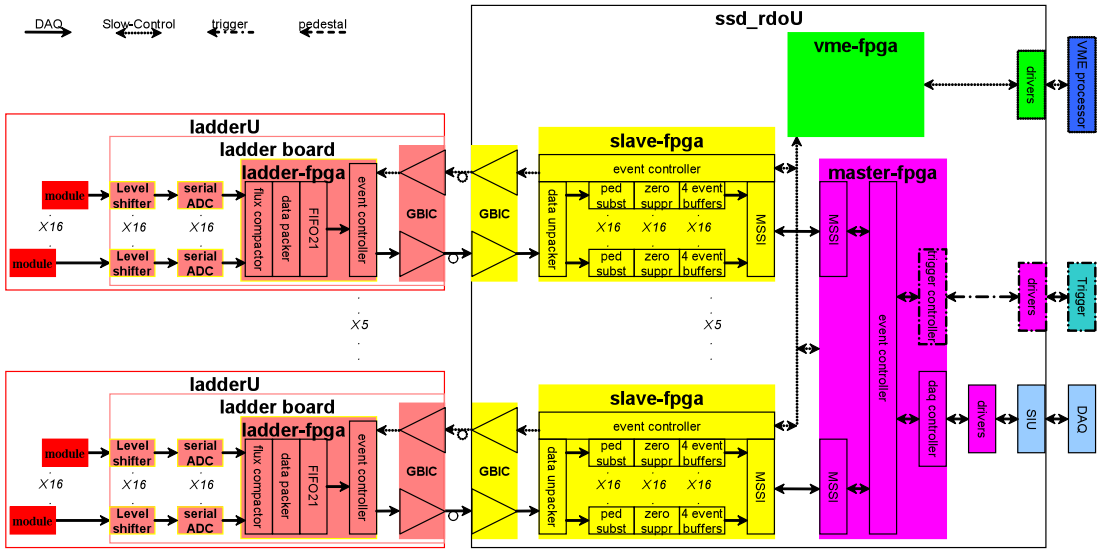

Figure 57: A schematic of the interconnection between the ladder electronics and the RDO card, Each RDO handles 5 ladders. The connection between the ladder electronics and the corresponding RDO card is a dual optical fiber.

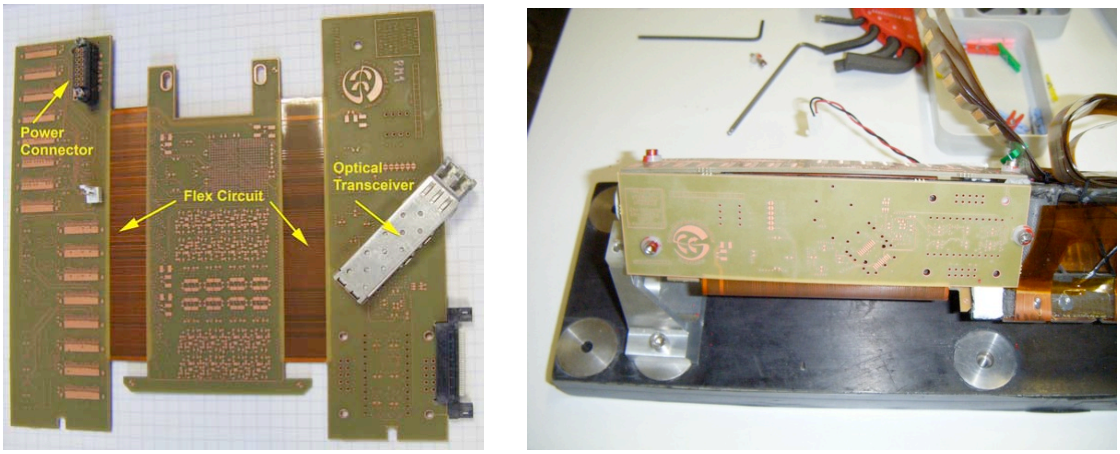

Figure 58: Prototype of a full sized ladder board. The left side shows the board as it comes from the manufacturer with several electrical connectors added. The ladder board folds into the page around the flexible circuits. The connector for power and the optical transceiver are also shown. The connector on the lower left is only for testing. The right side shows the board when it is folded and mounted to the ladder.

RDO Board

Each readout card accepts the fiber links from five ladders. A readout card is connected to the DAQ SSD PC by a DDL fiber link (50 MHz × 32 bit = 1.6 Gb/s or 40 MHz × 32 bit = 1.28 Gb/s) identical to those in reading out the TPC. Eight readout cards (four for each SSD side) reside in a 6U VME crate; there are, therefore, 8 fibers connecting the readout crates to the DAQ computers. The DDL links, together with their source interface to the SSD RDO (SIU board) and the PCI-X card residing in the SSD DAQ PC (D-RORC board), are readily available for purchase.

At the RDO card, a deserializer converts the 1.0 Gb/s bit train to a 20-bit wide data path, which is updated at a 40 MHz rate. Twenty of the 24 bits produced by the deserializer are reshaped into a 50 MHz stream of 16 bits width and delivered to a second bank of 16 1:10 deserializers, resulting in 16 10-bit wide replicas of the original ADC values produced on the ADC card. The remaining 4 bits are used for slow control functions (2) and synchronization (2). This second bank of deserializers is contained in an array of 5 FPGAs, each one dedicated to the data delivered by the fiber from a single ladder card. These FE-FPGAs perform zero suppression and multi-event buffering on the 16 data streams produced by the last bank of deserializers.

The multi-event buffers and zero suppression provide a means to reduce dead time due to data burden on the DDL optical fiber. Zero suppression is carried out in the simplest possible way – the ADC value for each strip is compared with a stored pedestal value corresponding to that strip. If the ADC value exceeds the pedestal, the strip number and ADC value are encoded into a 32-bit word and entered into the multi-event buffer.

The multi-event buffers are provided as a second means of reducing dead time. Simulation has shown that for randomly spaced triggers 4 buffers can keep the dead time to about 12 per cent for a trigger rate of 1 kHz. We expect about 3% of the strips to be hit in a central Au+Au event.

There is sufficient on-chip RAM storage in the FE-FPGAs to implement buffers for 4 events that have not been zero-suppressed. In zero-suppressed mode, these buffers can be coalesced into a single event buffer large enough to handle the largest zero-suppressed event. When a ladder is observed to be producing large zero-suppressed events, the offending module can be masked off.

The ladders are read out by passing a token to the chain of 6 ALICE128 analog multiplexers handling the analog signals corresponding to the 768 strips of a single module. Once this process has started, it must continue until the token reappears, at the end of 768 clock cycles. In the event of an abort arrival, the clock speed is doubled in order to minimize the time consumed by this process.

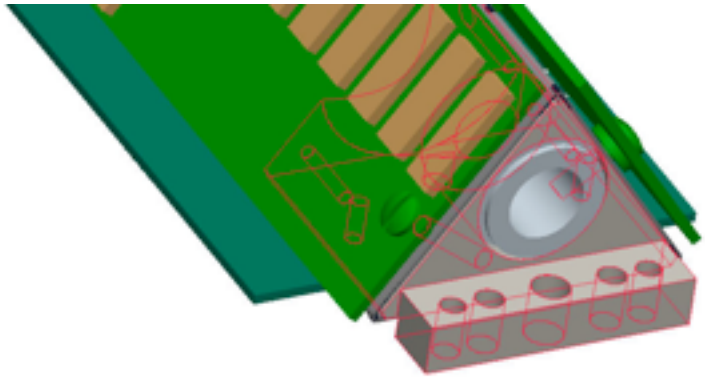

Figure 59: End bracket for the SSD that mounts to the OSC. The holes are used for alignment and to fix the detector.

3.4.3. Mechanical Mounting

The SSD is mounted on the OSC via a small bracket that is show in Figure 59. This design eliminates an end ring that creates significant backgrounds for the FGT. To assemble and repair the ladders, each ladder can be removed separately. Figure 60 shows the mechanical dimension of each ladder and that there is sufficient clearance to take out each ladder.

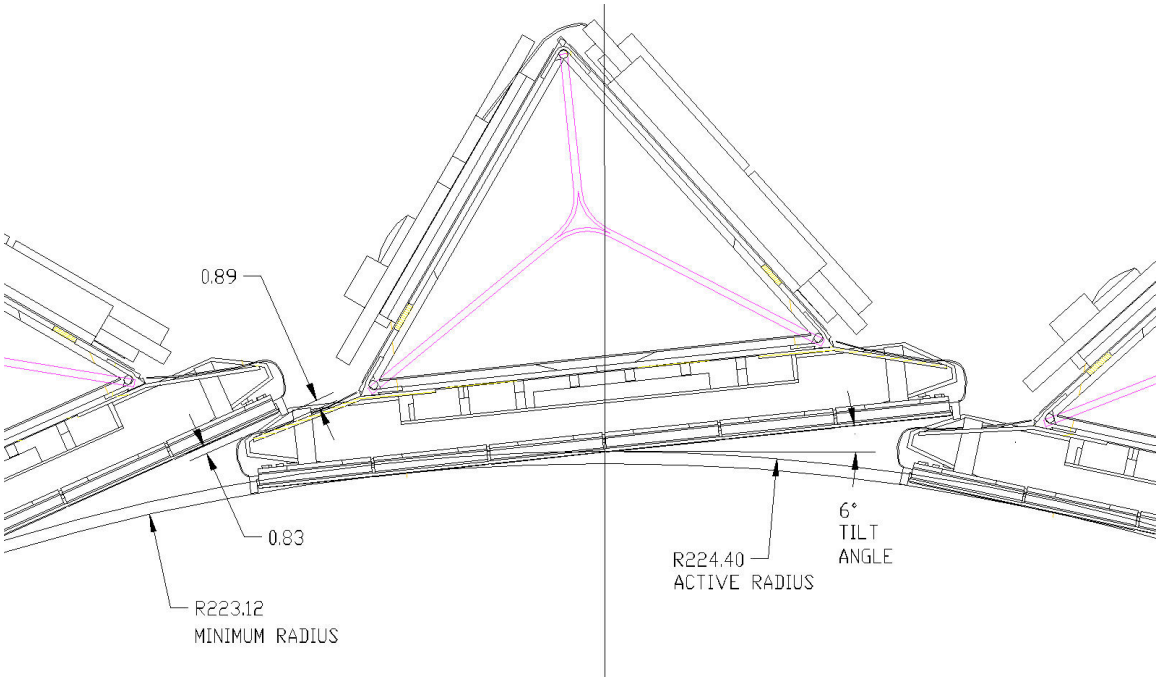

Figure 60: Physical location of each ladder. The length dimension is in mm. The tilt angle is 7° to provide clearance for a post on the modules.

3.4.4. Cooling System

The evacuation of heat produced by the electronics in the SSD is critical in order to establish stable behavior with the sensors and the associated electronics. The power consumption of the different components of the SSD ladders can be separated into two parts: The first part is due to the Front End Electronics (Alice 128C) chips which are mounted adjacent to the Si detectors. The Si detector modules, themselves, do not contribute substantially to the power budget. The second part is due to the Ladder Boards that are located on both ends of the ladders.

Table 12 compares the power consumed by the FEE electronics and the electronics boards on both ends of each ladder for the old and the new design. The power dissipated by the ladder boards will go up several watts. The ADC chips selected for the new ladder boards consume 20 mA @ 2.5 V. Taking into account all of the remaining components, the electronics at the end of each ladder are expected to consume 6.7 W. Also note that the power dissipated by the FEE cards will increase by about two watts compared to previous results even though the FEE cards have not changed in the new design. This change is due to the fact that the system will be running faster. Since the estimated dissipation for a full ladder is expected to be about 25 W, we will have to design a more powerful and reliable cooling system than before.

The Air Path in the Ladders

Each ladder is cooled by air circulating throughout the carbon fiber structure. A thin Mylar film is wrapped around the ladder to help guide the air. The electronic boards are installed on the ladder ends with the components pointing inwards and 'seeing' the inside of the triangular section. Deflectors inserted inside the ladders help guide the air to the warmest components.

	Old Electronics (measured)	New Electronics (estimate)
Total FEE	10 W	11.5 W
Total Electronic Boards	6 to 10 W	13.4 W
Total per ladder	**20 W max**	**24.9 W**

Table 12: Estimated power consumption for one ladder.

Air enters the ladder from a 1 cm orifice on one end. The triangular sections near the ladder boards and the ladder ends are completely open to allow for the full flow of air near the ends of the ladders. However, a wall blocks and guides the air into a smaller tunnel at the point where the ladder boards meet the Si detector modules. The purpose of the wall is to force the air over the Si detectors at high velocity in order to increase the rate of heat transfer from the FEE boards.

The flow of air is driven by an external vacuum system so that air is pulled through the ladders and the heated air is removed from the central part of the STAR detector. The input air comes from the TPC Inner Field Cage (IFC) at approximately 24°C. The warm air is then evacuated to the outside of STAR at a temperature of 35-40°C through a specially designed plenum.

Requirements and Functionality Tests

Cooling the electronics is an essential task to maintain the performance of the detector. The Si detectors and the ADC boards become unstable when they get too hot. For example, during RHIC Runs 6 and 7, the SSD ladders routinely tripped (due to a degraded cooling system) when they reached a temperature between 45°C and 50°C. The exact temperature that the modules tripped depended on the location and ladder number. The temperature rise produced an increase in leakage current, which resulted in lower bias voltage at the silicon due to IR loss in the bias resistor. In order to regain depletion, the voltage had to be raised. This cycle continued until the power supply tripped. So experience has shown that the SSD electronics should be maintained at 35°C to 40°C. Pushing the temperature above 40°C reduces the efficiency of the detector. Therefore, since the air inside the TPC IFC is maintained at 24°C, the heat generated by the ladders must be fully dissipated by a temperature differential of less than 15°C.

In 2002, the Nantes group did a series of thermal tests on a prototype ladder to see how it would perform under various conditions. Table 13 shows the temperature inside the ladder at a few critical points when the cooling system was off. The maximum temperature measured was 46.5°C. These tests were done at an ambient temperature of 19°C and with ladder boards that dissipated less heat than we are contemplating now. The prototype ladder consumed 16 Watts of power compared to 25 Watts, today.

	SIDE P (°C)	SIDE N (°C)
ADC	42.8	46.5
Control Board FPGA	34.8	36.5
Connection Board	45.2	45.4

Table 13: Mean electronics temperatures measured on the 2002 prototype ladder with cooling 'off'. The ambient air temperature was 19°C.

Table 14 shows the temperature distribution at the critical points with the cooling 'on'. Once again, it is worth noting that these temperatures were recorded using input air at 19°C. In the actual STAR environment, the input air is drawn from the IFC and the air in this region typically has a temperature of 24°C.

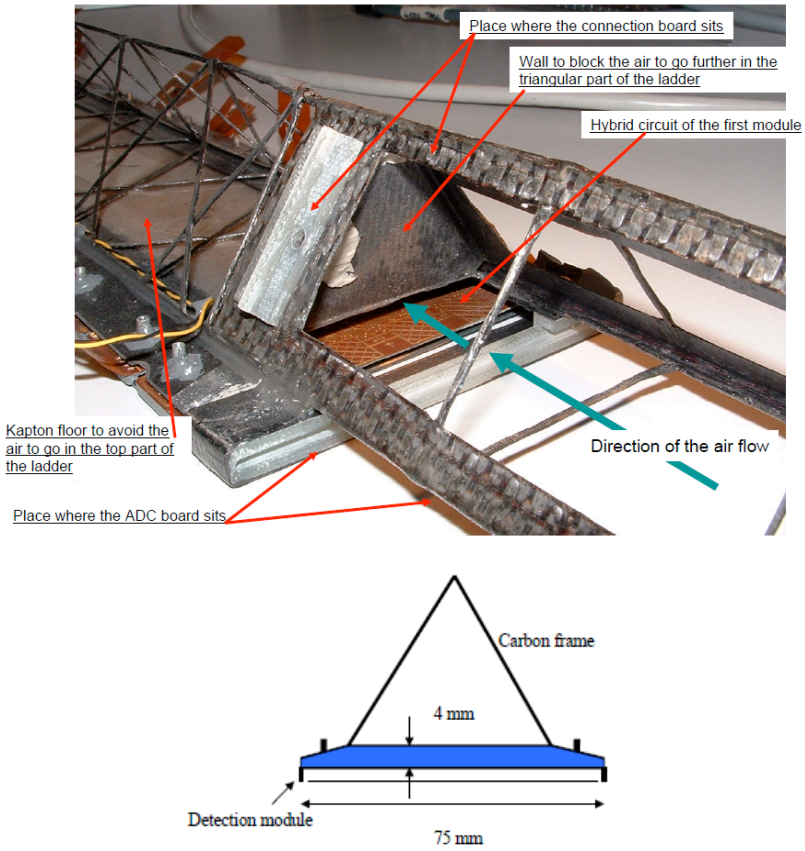

Figure 61: Top – a photograph of the carbon fiber structures near one end of a ladder. The Si detectors are mounted on the bottom of the ladder and are shown disappearing to the left in the figure. The air path is blocked at the transition point from ladder boards to the Si detectors by a wall that forces the air down and into a small tunnel over the Si modules. The dimensions of the tunnel are shown in blue in lower figure. This tunnel is 68 cm long and has a cross-sectional area that is approximately 1/5 of the area of the major triangle.

	SIDE P (°C)	SIDE N (°C)
ADC	33.1	33.2
Control Board FPGA	33.7	30.7
Connection Board	27.6	24.5

Table 14: Mean electronics temperatures measured on the 2002 prototype ladder with cooling 'on'. The ambient air temperature and input air temperature was 19°C.

Additional temperature measurements were performed at various points along the ladder and these results are shown in Table 15.

Module	Si Temperature (°C)	COSTAR Temperature (°C)
3P	27.8	35.3
5P	32.9	32.5
8P	30.9	37
11P	30.2	37.5
14P	28.7	34.9
16P	25.1	32.3

Table 15: Mean temperatures measured at various points along the 2002 prototype ladder with the cooling system turned on. The column on the left identifies the wafer number.

Note that between modules 8 and 11 (in the middle of the ladder), the temperature goes above 37°C even when the cooling system is on. This indicates the necessity of having a robust cooling system for the upgraded SSD with plenty of capacity to cool the additional heat load that will be generated by the new electronics.

The Nantes group did additional tests in 2002 that quantified the cooling requirements for an SSD ladder. Figure 62 shows a schematic drawing of the prototype ladder (Ladder #0). The ladder was connected to a Vortec airflow amplifier with an 8 mm (ID) tube that was 4.5 meters long. The flow rate was approximately 1 l/s and the pressure drop at the far end of the ladder was 12 mbar. The pressure drop at the end of the 8 mm diameter tube was 43 mbar; indicating that the long tube provided greater impedance to the airflow than the ladder.

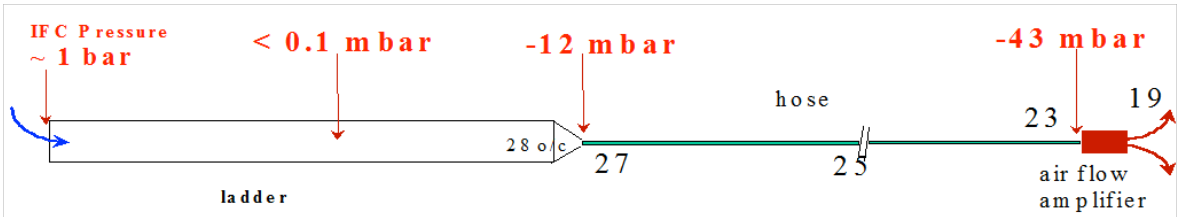

Figure 62: A schematic drawing of the Ladder cooling test that was conducted in Nantes in 2002. The ladder was cooled by drawing air through it using a Vortec airflow amplifier as the vacuum source. The pressure at various points in the system is shown in the diagram.

The pressure drop across Ladder #0 and across the 8 mm tubes attached to it can be understood in terms of a simple formula for a compressible gas passing through a round tube[26]:

$$dp = 40\ q^{1.85} L\ /\ d^5 p$$

where dp is the pressure drop in mbar, q is the flow rate in liters per second, L in the length of the tube in centimeters, d is its diameters in centimeters, and p is the input pressure in mbar. Note that the pressure drop decreases as the 5th power of the diameter of the tube and increases approximately quadratically with the flow rate.

Figure 63 shows the measured temperature profiles vs. time at various points on the ladder. A key performance parameter is the difference between the inlet air temperature (blue line) and the outlet air temperature (red line). The predicted temperature difference, for a 16 Watt source cooled with an airflow of 1 l/s, is 13°C. The measured temperature rise was 11°C. This indicates that the ladder was ~85% efficient in transferring its heat load to the air stream.

Presumably the remainder of the heat was transferred to the surrounding environment by radiation and conduction.

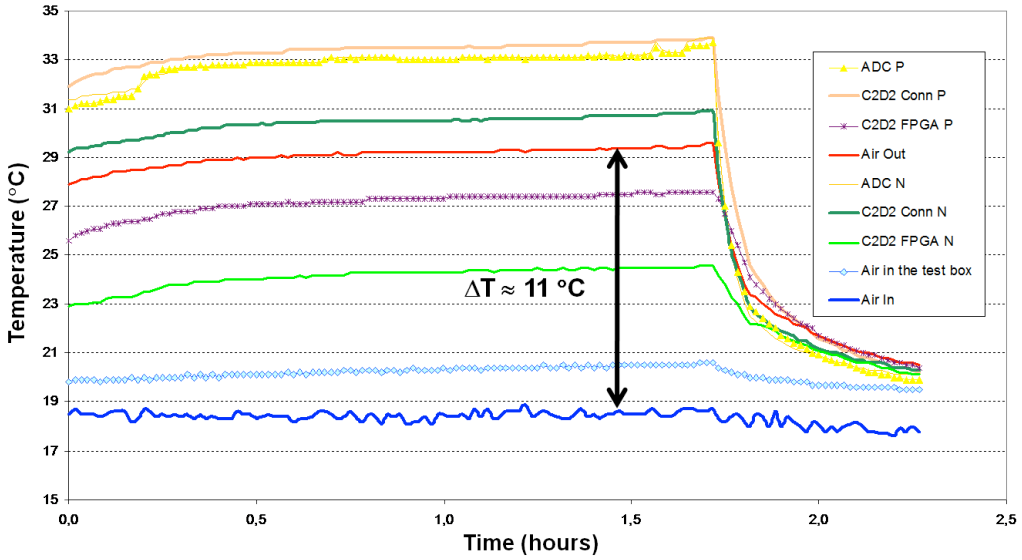

Figure 63: Temperature profiles for Ladder #0. The temperature rise is shown as a function of time after powering up the ladder is shown at various points on the ladder.

Vacuum source

Figure 64 shows the performance parameters for various vacuum sources. The blue line is the Vortec system that was previously used to cool the SSD. The pink and green lines represent small industrial vacuum sources that are used in the wood products industry to remove dust from around saws and lathes.

The red diamond in Figure 64 is the operating point that is required to cool five ladders with the old electronics and their associated RDO board. As shown in the figure, the Vortec (model 903) performance curve is very well matched to the task of cooling 5 ladders, which are individually attached to 4.5 meter long, 8 mm diameter, tubes

The wood products industry sells compact units that are designed for long-term use and are quite inexpensive and match the needs of the SSD cooling requirements. A typical example is shown in Figure 64.

In addition to the new vacuum source, we plan to use larger diameter tubes (or plenums) to guide the air from the endcap of the TPC to the SSD ladders because the pressure drop from one end of a tube to the other decreases as the 5th power of the diameter of the tube. This strong dependence on diameter is shown in Figure 64. This figure shows the difference between the working point marked by the triangle and the square symbol. The triangle shows the predicted performance of the 1.2 kW unit when drawing on 20 ladders at 1.6 liters/second through 0.8 cm tubes. The square shows the predicted performance of the 1.2 kW unit when drawing on 20 ladders at 1.6 liters/second but through four 2.5 cm (ID) tubes. Tests done at STAR in 2009 have confirmed that the predictions for the 0.8 cm diameter tube test agree with actual measurements in the lab. Tests with the 2.5 cm diameter tubes are still to be done.

The minimum flow rate for the SSD will be 1.6 l/s. The air velocity inside the ladders will increase from 0.5 m/s to 0.8 m/s in the large triangular sections of the ladders, and from 3 m/s to 5.0 m/s in the tunnel over the Si detectors. We do not expect the ladders to vibrate at these

relatively modest velocities, but additional bench tests are scheduled to confirm this expectation. Finally, an added benefit of changing the vacuum source for the SSD is energy efficiency. The new system will consume 1.2 kW compared to 76 kW of the previous system.

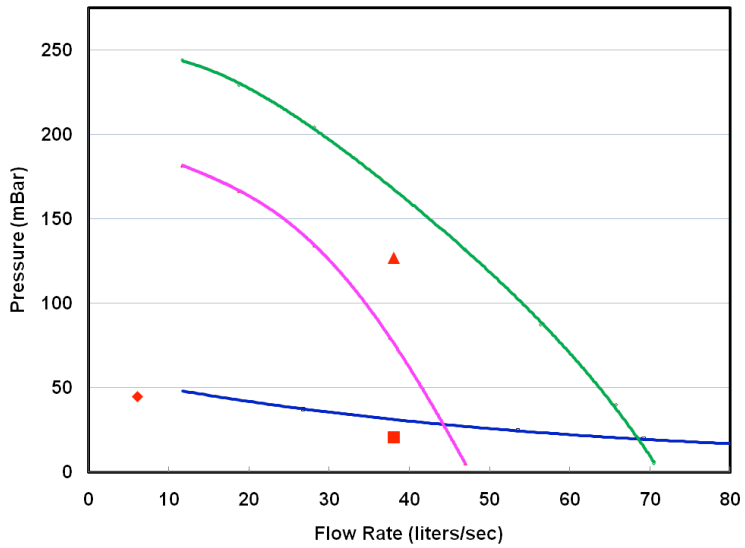

Figure 64: Performance curves for three different vacuum sources. The blue curve is for the Vortec Model 903 airflow amplifier. It was used to cool 5 ladders when each ladder was mounted on the end of a long 0.8 cm tube (red diamond). The magenta curve is for a 1.2 kW blower and the green curve is for a 2.6 kW blower. These units are commonly used in the wood products industry. The 1.2 kW unit has sufficient capacity to cool 20 ladders that use a plenum that consists of 4 long tubes, each 2.5 cm (ID) in diameter (red square), but it does not have enough capacity to cool the ladders if they are mounted on the end of 0.8 cm tubes (red triangle).

Figure 65: Model RP-116 vacuum supply from 'The Dust Collector Source'27. The unit is about the size of a two-drawer file cabinet and its performance specifications are shown in Figure 64.

3.4.5. Testing of Reading the Ladder Board at 5 MHz

The highest technical risk for the SSD upgrade is whether it is possible to readout the modules with 5 MHz. To do a test of the readout speed, we modified the existing FPGA code to skip

reading a module. This "trick" allows us to read the other modules faster, with the old electronics, as all modules are read at the same time.

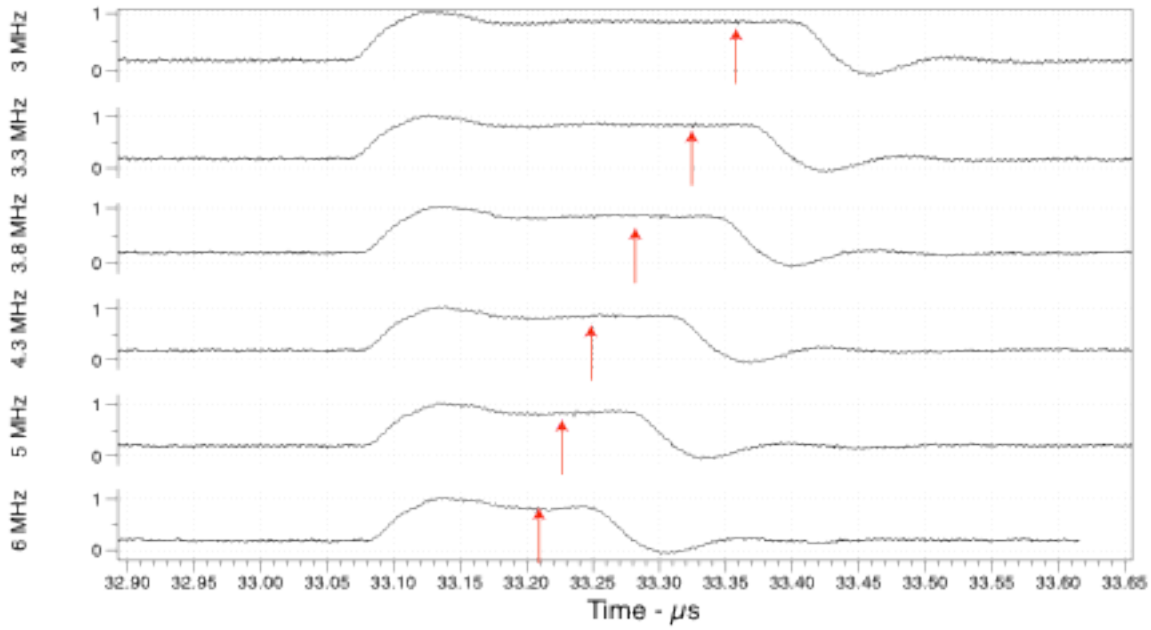

Figure 66: Analog trace of a module being read out at different seeds. The red arrow shows a stable location that is suitable for the ADC to sample.

These results of scanning a module for the current 3 MHz to the higher than design value 6 MHz can be viewed in Figure 66. The red arrows show a location that is stable area where the ADC can sample the analog output. As the new design for the readout speed is 5 MHz, this value is clearly acceptable.

The length of the analog signal varies from one side of the ladder to the other. This cable length could produce problems for the signals. We tested the ladder at 5 MHz with modules on both sides of the ladder. Figure 67 shows Module 1 being read out two times compared to Module 14 at the other side of the ladder. The ADC value plateaus so there is a "sweet spot" to set the ADC gate. Once again, an analog readout speed of 5 MHz meets the requirements of the new data acquisition system.

3.4.6. Services

The SSD services must pass through the integration constraints of the WSC and FGT on the west end, and the MSC and ESC on the east side. The most critical cables for the SSD upgrade are on the west end of the OSC. These cables must be low mass on the FGT side and fit in the two slots between the FGT. Therefore, the two slots set the constraints on cable size. Using this envelope, we found a solution that can handle the current draw and allowable voltage drop for the ladder power connections, and the count of other conductors and optical fibers needed to service the ladders. All conductors will be standard commercial CCAW wire (10% by volume copper-clad aluminum). The cable is a custom construction with an aluminum foil shield and silicone insulation and jacket materials, which have excellent performance with regard to flammability, radiation tolerance, and mass. The cable diameter estimate accounts for fill factor and for insulation and jacket thicknesses to meet the required voltage and flammability ratings.

The SSD is readout separately on each side of STAR. Each ladder is a separate detector. Therefore there will be 20 cables and 20 dual fibers on both the East and West end. As each ladder requires only one HV bias connection, these wires are simply unused in the west cables where space is more constrained. An estimate of the size needed for these cables is given in Table 16. The values specified in that table with some contingency with fit in that location. All cables from the Ladder Board and the cooling lines will be routed on the OSC and then terminated in a patch panel at the end of the OSC.

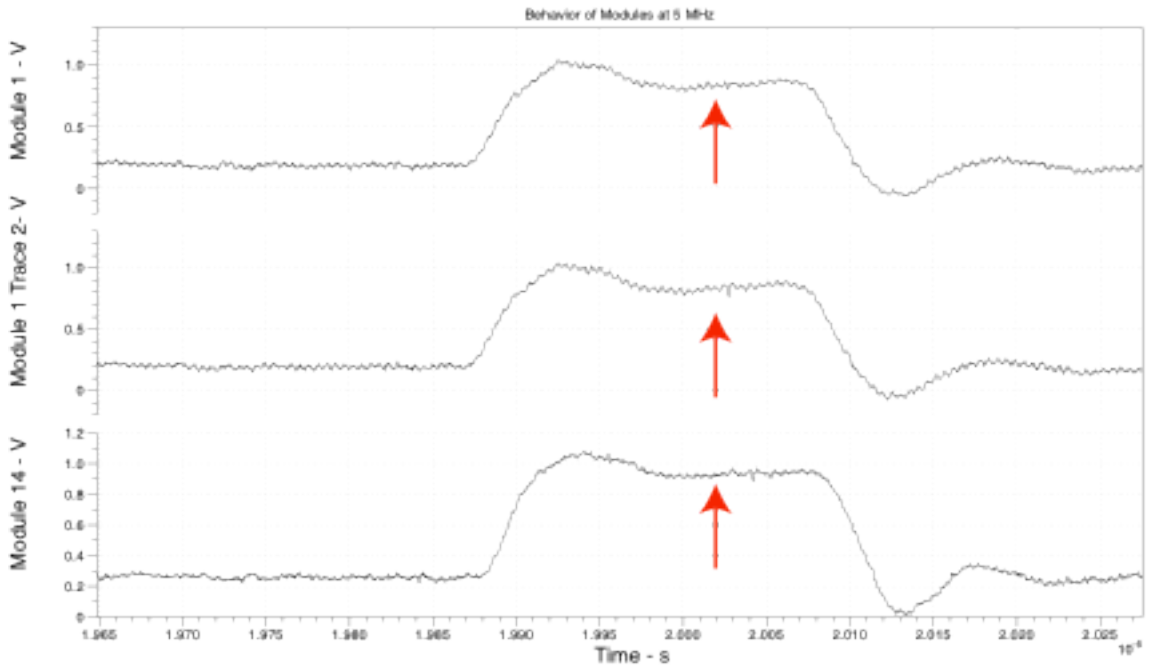

Figure 67: Test of reading out modules at the design specification of 5 MHz. Modules 1 and 14 are on opposite sides of the ladder. The read arrow shows a time slot where a sample can be taken.

Function	Type	#	Diameter mm	Area Rectangular cm^2	Total Area Rectangular cm^2
DAQ and Slow Control	Optical Fiber (dual)	20	3.0	0.1	1.8
Ladder power / bias	Sense (×6 AWG 26)	20	5.5	0.3	6.1
	LV (×8 AWG 22)				
	HV Bias (×2 AWG 26)				
Air Cooling	Air cooling to end of cone	20	12.7	1.6	32.3

Table 16: SSD services parameters. The total area is calculated in square centimeters, not accounting for packing fraction. The diameter of the air-cooling is taken from the size of the original SSD design.

Nicomatic makes the connector on the Ladder Board. As the connecting cable is copper-clad aluminum cable, we need to assure that there is a reliable connection. We have selected to mount the mating Nicomatic cable on a very small PC board. The cable will be soldered directly to the PC board so that a solid connection can be made. It is easier, more reliable, and less expensive to solder the wire to a trace. In addition, this PC board allows us to put strain relief for the cable directly on the PC board. The only other cable needed for the ladder will be a standard fiber optic cable. Both of these cables go to a patch panel – east cables go the ESC patch panel and west cables go to the WSC patch panels. The cables from ESC and WSC patch panel then go directly to a rack where the RDO cards and power supply reside.

3.4.7. Electronics on South Platform

The SSD occupies one rack on the South Platform. The readout electronics, low voltage and high voltage are located there. A VME crate contains both the RDO cards and the Slow Control communication interface. In addition there are power supply crates, and distributions boxes for the HV and power cables.

We have identified two manufacturers who can provide suitable power supplies. We will select the manufacturer at an appropriate time during the project. These power supplies provide 100 V, +2 V, -2 V, and +5 V to the ladders. They are remotely controlled by Slow Controls.

The Slow Control information to and from the ladders travels over the optical fibers to the readout cards. The SSD Slow Control interface consists of two independent JTAG chains: the Slow Control chain and the FPGA configuration chain. Slow Control communicates with the RDO board through the VME backplane. There are 8 readout cards in the VME crate. The transport of data on optical fiber between RDO and Ladder Boards is completely transparent to all the components that have to decode and answer to the JTAG orders. Each of the readout cards has a separate interface to the STAR trigger.

The 8 SSD readout cards require 8 DDL fiber links to DAQ PCs. Each DDL receiver card (DRORC) handles two fibers; thus, 4 DRORC cards are required to provide the necessary interface. This will be implemented in 2 PCs, each with 2 DRORCs. Each PC is responsible for one-half of the SSD. These PCs will be located in the DAQ room.

3.5. Global Structures and Integration

The three detector systems of the HFT Project and the FGT detector require a common support system to integrate these detector systems into STAR in a coherent fashion with limited mass. The design goal has been that the new support structures will provide for positional stability to better than 100 microns. The structure required to represent less material than the existing structures, where the presence of material impacts the physics performance of STAR. The technically most demanding potion of this WBS, 1.5, is the design and fabrication of the carbon fiber structures to meet the design goals given above.

The integration subsystem provides technical support that is common to the detector subsystems. This includes providing space and utilities for the testing and assembly of the detector subsystems. The integration subsystem will then work with the STAR Technical and Support Group (STSG) to install the detector systems into STAR. The functional breakdown to WBS Level 3 is given in Table 17:

WBS	Description
1.5.1	**Mechanics**—Fabrication of the the carbon fiber structures and tooling
1.5.2	**Electronics**—An historical place holder for a few small electronics items
1.5.3	**Assembly**—Assembly of the support structures and assembly of the detectors onto the support structures
1.5.4	**Infrastructure**—Provides for facilities to conduct assembly, detector testing and facilities for installation
1.5.5	**Installation**—The installation of the cables, electronics, and detectors into the STAR infrastructure
1.5.6	**Pre-CD3 Engineering**—Contains the engineering to support item 1.5.1 for prototype structures and initial engineering analysis
1.5.7	**Post-CD3 Engineering**—Contains the engineering for the carbon fiber structures, tooling for fabrication and assembly, and fabrication oversight
1.5.8	**Safety**—Ensure safety is incorporated along the path of the experiment.

Table 17: The Level 3 WBS sections of Global Structures and Integration.

The need for an integrated approach is easily demonstrated by a couple of figures of the detector systems. Figure 68 demonstrates the close nesting of the PXL, IST and the SSD detectors. A cut away view of the HFT system inside Star is shown in Figure 68. Only an integrated support structure could meet the needs of these detector systems buried in the center of the STAR system. A Project Mechanical Engineer is in charge of the Global structures and the attachments of the subsystems to these structures to ensure that the system has no interferences. A set of interface documents has been generated for the detector sub-system. Figure 68 displays a person inserting the PXL detector into STAR. The PXL subsystem is designed to enable replacing the PXL detector in a relatively short time period, eight to 24 hours. A spare detector is kept ready in the clean room outside the IR. Integration must make a few modest changes to the infrastructure to accommodate this goal of swapping PXL detector packages in 8 to 24 hours.

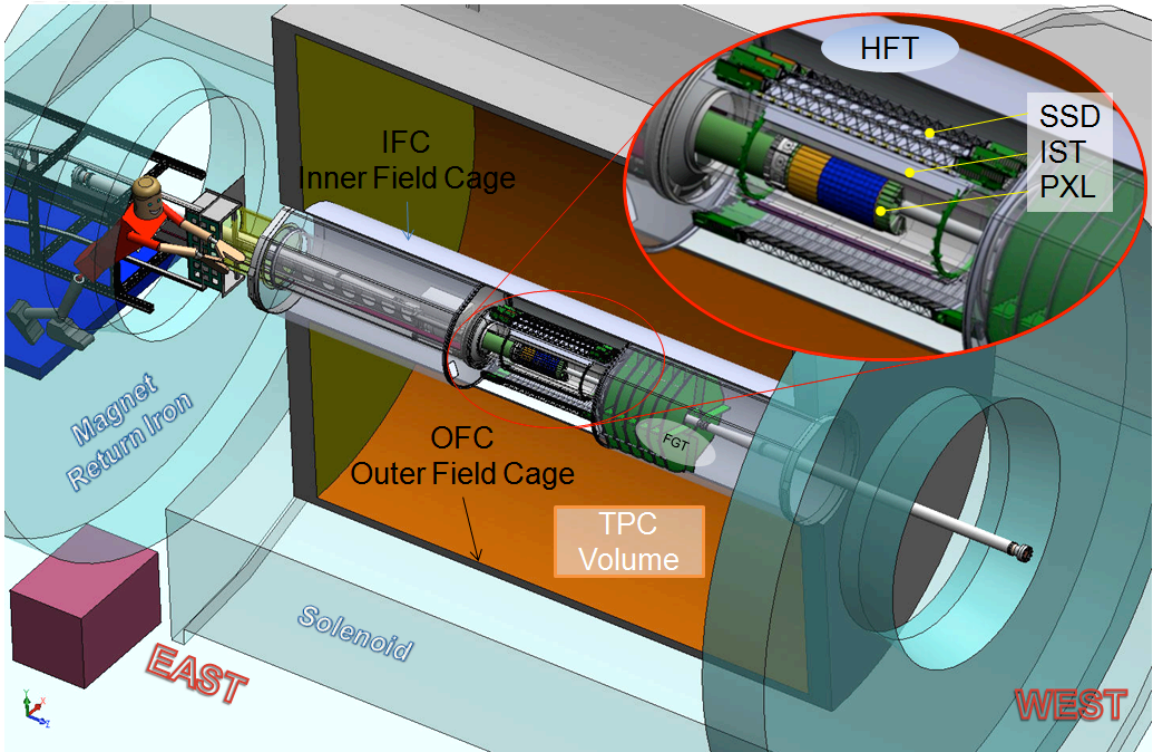

Figure 68: Cut-away of the STAR magnet showing the PXL, IST, SSD, and FGT detectors. A person is shown inserting the PXL detector system by standing on a platform and using the PXL insertion box.

A phased approach for the support structures was chosen. The desire to integrate the FGT detector with the HFT supports add the requirement that a portion of the support structures need to be ready at an very early stage of the HFT Project. The phased approach was also chosen so that initial designs can be installed to assess the validity of the design without satisfying all the detector requirements that must be satisfied by the final design. The cost and schedule support a phased assembly and installation of the HFT into STAR. The cost impact is small since a substantial portion of the cost of these structures is the engineering and fabrication tooling. The present integration cost and schedule is based on completing the HFT in the summer of FY13. The summer of FY14 is left as a contingency installation for the final project. Table 18: shows the planned phases.

Year	Goal
Summer FY11	**Install the Inner Detector Support (IDS) with existing beam pipe and the FGT.** The transition cones may not have the required ports for the SSD utilities. The OSC will not have the mounting features for the SSD. The MSC will not be installed. Clean room will be made ready for the assembly of the FGT into the IDS.
Summer FY12	**Install the IDS into STAR with the PXL prototype, FGT, and the new beam pipe**. The IDS must be removed from STAR and have the Middle Support Cylinder (MSC installed). The new beam pipe will also be integrated into the assembly. IR modifications will be completed for the installation and servicing of PXL.

	Have the clean room ready for the testing of the prototype PXL detector.
Summer FY13	**Install the complete HFT system**. Remove the IDS assembly from STAR and disassemble. Install the new OSC and transition cones. Test new detectors as they arrive in the clean room area. Complete IR infrastructure for HFT.
Summer FY14	Contingency if FY13 goal not met

Table 18: Installation goals planned for the summer shutdowns.

3.5.1. Mechanical Structures

The mechanical structures to support the detectors are the dominant effort of WBS 1.5. The design and fabrication of these rigid lightweight structures is technically demanding and requires experienced technicians and engineers. The LBNL team has the expertise and experience to successfully complete these structures. WBS 1.5.1 contains the effort to test and build the mechanical structures, but the engineering effort is accounted for in WBS 1.5.6 and 1.5.7. The costs associated with the mechanical structures total about 70% of the budget of Global Supports and integration. Table 19 provides a partial list of the structures.

Structure	Detector	Structural	Utilities
WSC—West Support Cylinder	Holds the FGT and confines FGT air flow	Transfer loads on the west side to TPC wheel	Transfers utilities for FGT and SSD to the west side.
ESC—East Support Cylinder	Holds the MSC	Transfers loads to the TPC wheel on the east side	Transfers SSD utilities to east side
OSC—Outer support Cylinder	Holds the SSD	Structural bridge between ESC and WSC	
MSC—Middle Support Cylinder	Hold the IST, PXL and beam pipe	Routes IST and PXL services	cooling volumes for the PXL and IST and routing of utilities

Table 19: List of the main support structures for HFT.

Figure 69 shows a schematic of the Inner Detector Support (IDS) components. The ESC, WSC, and OSC compose the primary structures of the IDS. The MSC structure is supported inside the IDS. There are additional sub-components such as transition cones, backing rings, and stiffening plates that are part of the MSC and IDS structures. The depiction in Figure 69 provides details of the ESC/WSC shell to OSC via the transition cone. Figure 70 provides details of the ESC/WSC shell to OSC via the transition cone.

The engineering analysis for the IDS is complete. The engineering analysis for the MSC is nearly complete. The final design report for the IDS has been sent to C-AD in preparation of an engineering review. Excerpts from the engineering reports are presented below to demonstrate

that the designs are advanced sufficiently to determine cost, schedule, and achievement of the design goals.

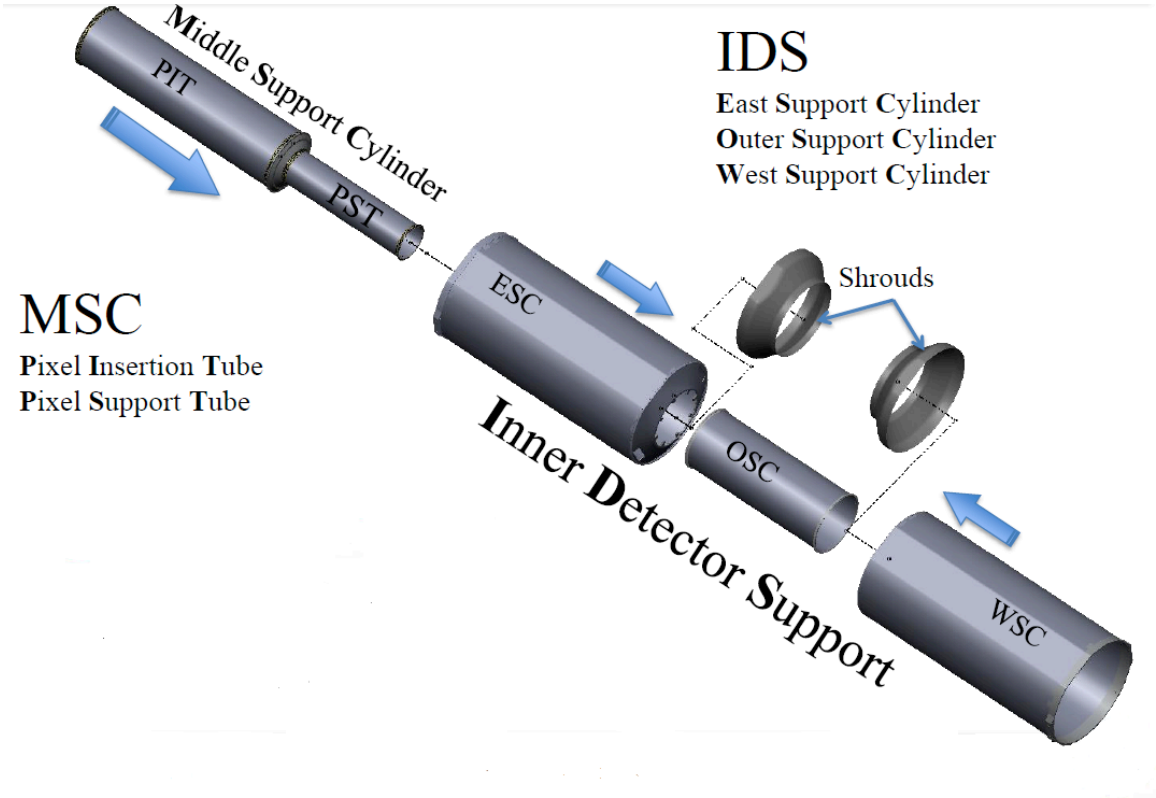

Figure 69: Schematic view of the IDS and MSC.

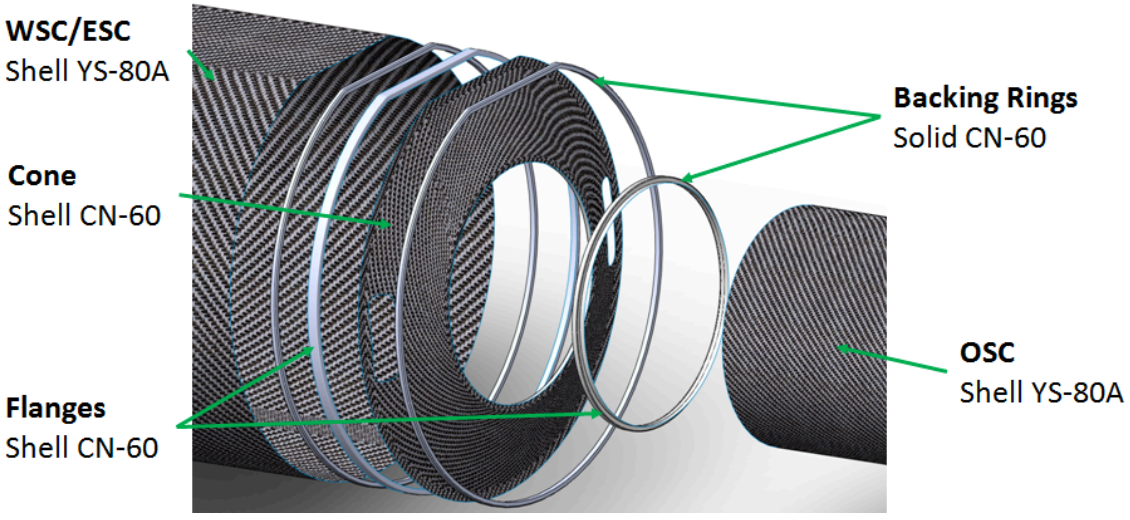

Figure 70: Schematic view of the MSC to OSC transition.

Table 20 lists the requirements that the global supports are being designed to meet.

Requirement	Structures impacted	Addressed by
Sufficient air flow along TPC Inner Field Cage (IFC)	ESC,WSC, Main flanges	Diameter of ECS and WSC and flange spacing at TPC wheel
Must not allow discharges with TPC IFC	ESC, WSC	Must be conducting material to avoid excessive charge buildup. There must be biased shrouds at the ends of the ESC and WSC
Transfer detector loads to the TPC wheel	ESC,OSC,WSC,MSC	Designs and materials used
Safety factor of 3	All structures that if failure can occur could damage the beam pipe or IFC	Designs plus external review
Avoid Physics Impact	OSC, MSC, end flanges	Thin carbon fiber design maintains minimum radiation lengths
IFC temperature	Structures act as barriers	Cooling of detectors and removing heat load
Positional Stability	All structures	Temperature controlled and low CTE material

Table 20: Design requirements given by structure and design approach.

The IDS will replace the existing cone structures that were installed to support the SSD and SVT. The SVT cone interface to the TPC wheels will be replicated in the IDS design. Several options were investigated for internal detector support structure; choice between the various options was optimized via cost, schedule, and physics objectives to arrive at the current baseline. The rejected options that were considered are not presented in this document.

3.5.2. Mechanical Requirements

The structural performance and interface requirements of the IDS are driven by both HFT and FGT requirements. The HFT requires global stability on the order of the pointing resolution of the TPC, about 1 mm. The FGT uses the beam constraint for tracking and thus requires stability on the order of the beam diameter of about 100 μm, and thus drives the global stability of the IDS.

The mechanical design must support the detector loads while satisfying the position and stability requirements. Table 21 provides a list of the loads.

Applied loads upon IDS structure

Load Description	Value (kg)	Distributed upon:
EFS West	1.45	East edge of WSC
EFS East	1.45	West edge of ESC

1/2 MSC @ East Cone	8.05	Outer flange of east cone and large flange
1/2 MSC @ ESC Main Stiffener	8.05	Inner edge of east stiffener plate
1/2 Beampipe @ West Cone	4.3	Inner flange of west cone and small flange
1/2 Beampipe @ East Cone	4.3	Inner flange of east cone and small flange
FGT all disks	20.87	Two short WSC rails
FGT services	3.18	Bottom split surfaces of WSC
1/2 MTB @ East Cone	11.97	Outer flange of east cone and large flange
1/2 MTB @ ESC Main Stiffener	11.97	Inner edge of east stiffener plate
PXL	6.15	Inner flange of east cone and small flange
PXL external parts	33.15	Main flange east
SSD services west	9.64	Two side split faces of WSC
SSD	13.26	Two split rings on OSC
SSD services east	11.79	Two side split faces of ESC
IST West	3.2	Inner flange of west cone and small flange
IST East	4.88	Inner flange of east cone and small flange
IST services, signal	33.6	Two side split faces of ESC
IST services, cooling	4.76	Two side split faces of ESC
TOTAL APPLIED LOADS	**196.02**	
Structure self-weight, as computed with composite laminate definitions in ACP		
Item	**Value (kg)**	**Modeled as:**
ESC + WSC	13.09	Composite laminate
OSC	2.48	Composite laminate
Stiffener Plates (3x)	1.62	Composite laminate
FGT Rails (4x)	0.31	Composite laminate
Composite Flanges (4x)	0.5	Composite laminate
Cones (2x)	6.34	Composite laminate
Main Flange West	6.1	Aluminum
Main Flange East	6.06	Aluminum
Rail Plugs (4x)	0.15	Aluminum
Backing Rings (6x)	2.66	Black titanium
TOTAL STRUCTURE WEIGHT	**39.31**	

GRAND TOTAL (STRUCTURE + LOADS)	**235.33**

Table 21: Loads extracted from detector interface documents

These loads have been applied to models using SolidWorks (SW) to determine the design and performance characteristics of the support structures.

3.5.3. Electrical Requirements

The IDS is inserted into the Inner Field Cage (IFC) of the STAR TPC. The IDS must be compatible with the bias voltages applied within this environment. The ESC and WSC will protrude into the IFC and the surfaces will be held at ground. The sections of the WSC/ESC with the smaller radius of curvature will have increased field gradients. A shroud is a non-structural component to provide a larger radius of curvature to reduce electrostatic fields; one will be located over the transition cones at each end of the OSC. The shrouds can either be grounded or operated at a bias voltage. STAR has used 4kV/cm as the design goal is the past to avoid corona and breakdown. The most recent simulations of the field gradients have shown that the actual maximal areas of field gradient are at the IFC (and OFC) caused by edge effects inherent in those structures rather than the introduction of the IDS with shroud at ground potential. A shroud at ground potential will result in a field gradient of 5.7 kV/cm at the resistor chain. It is expected that the shroud can be at ground and that the initial goal was too conservative. The power supply and cable exists for applying a bias voltage, if necessary. Tests will be conducted during the summer of 2011 to verify the simulations.

The structure of the shroud will be fiberglass with a high dielectric matrix (Cyanate Ester), which is also common to all of the other structures (it also has high radiation tolerance). The outer conductive layer is a co-cured Anti-static Veil 80/20 E-glass/Carbon fiber rather than conductive paint to reduce chance of contaminating debris within the IFC. The need for bias will likely require some development of this laminate in addition to its interface to the structural shells of the ESC/WSC. Standoff, both surface and thru-thickness for any applied bias voltage on ESC/WSC structures is required to be considered in the design, detailed design remains to be done. The surface of the ESC and WSC will be conductive to prevent charge buildup. The shroud will also support an EMI foil over the SSD. Figure 71 shows the design of the shroud, the WSC, and the SSD.

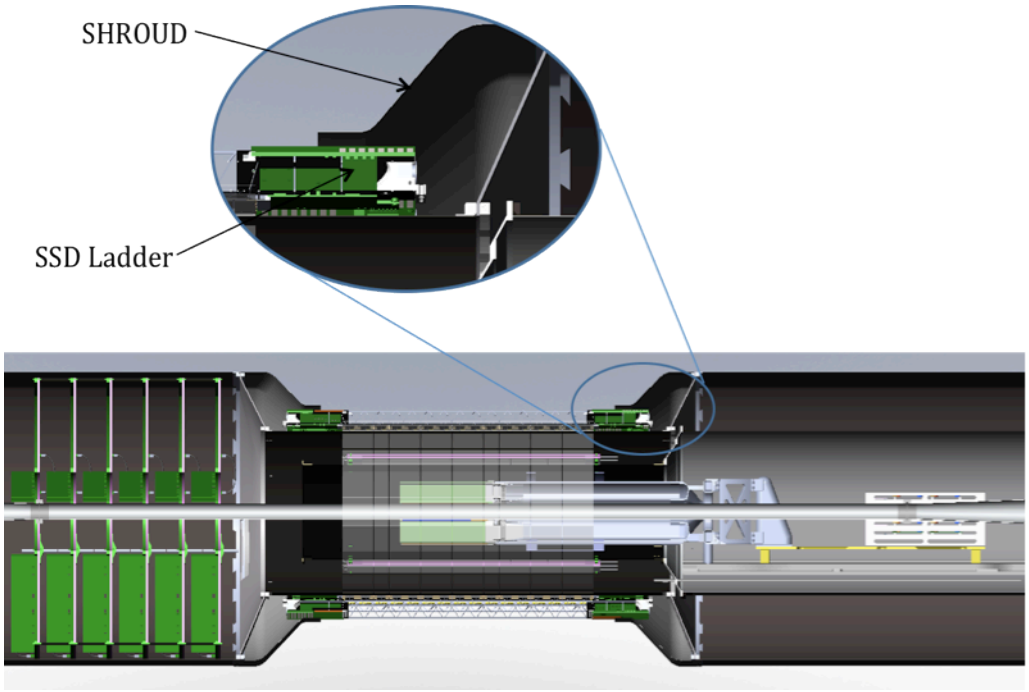

Figure 71: E-field shroud.

3.5.4. Structural Shell of WSC/ESC Assembly

The main component of the structural shell is a thin carbon fiber laminate. The inner diameter will be common to both WSC and ESC as it will be set by common tooling. Lamina may differ between the two structures based on differing structural requirements to support the FGT. The large sectional inertia of the shell implies that the global performance of the IDS is not dominated by the laminate properties as born out in the HFT CDR document. It was shown that thickening this laminate simply increased the mass, increasing the deformation implying that this is not an avenue for decreased deflection. The space requirements for the FGT established the size of the WSC. The ESC dimensions were established by the desire to reduce tooling costs.

Fabrication of the WSC (and prototype ESC) shells has begun. Figure 72 shows the WSC laminate after it has been removed from the autoclave. Eventually the WSC mandrel tooling will be modified for the fabrication of the first article ESC.

Figure 72: WSC on mandrel after being removed from the autoclave

Transition Cone

The transition cone transfers the primary moment load of the simply supported IDS from the structural shell to the OSC. Studies have shown that a conical laminate was more efficient in terms of material than a flat design. Maximizing the cone depth (frustum) maximizes performance of the entire IDS. The frustum is limited to 7 cm to meet the space requirements of the SSD and the FGT. The overall stability performance of the IDS is most sensitive to the

thickness of the transition cone. The transition cone is currently 4 mm thick, with 5 mm flanges at both inner and outer diameters to allow bolted interface to the structural shells and the OSC. Note that the total flange thicknesses are 10 mm, 5 mm for each side of the flange. Transfer of stresses into the cone via the flanges has been investigated. The flanges are CFRP with Titanium fasteners.

The transition cone from the WSC/ESC to the OSC has undergone FEA for many potential options. The phased approach for the mechanical structures benefits from having transition pieces that are bolted rather than bonded. The analysis has shown that the bolted approach provides nearly equal strength but with the ability to change components in the future and limited increase in the materials budget for radiation lengths. Figure 73 shows the deformation of the transition cone with a maximum deformation of 9.2 microns compared to 8.2 microns for a bonded structure. A latter analysis was conducted with the load transferred to the cone by the OSC shell. Figure 74 shows a transition cone after it has been cured.

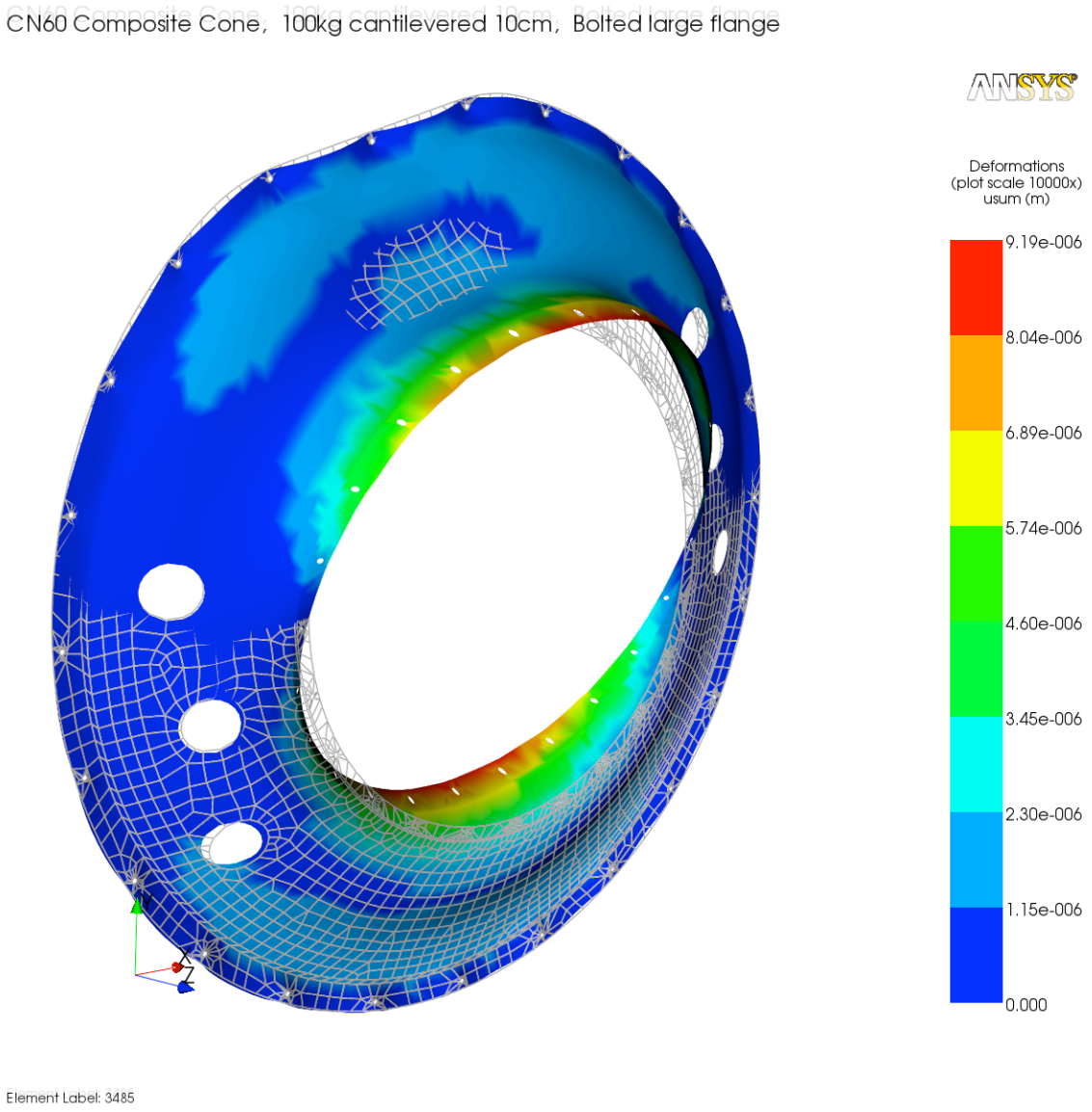

Figure 73: Deformation is the cone structure for 100 kG load cantilevered 10cm.

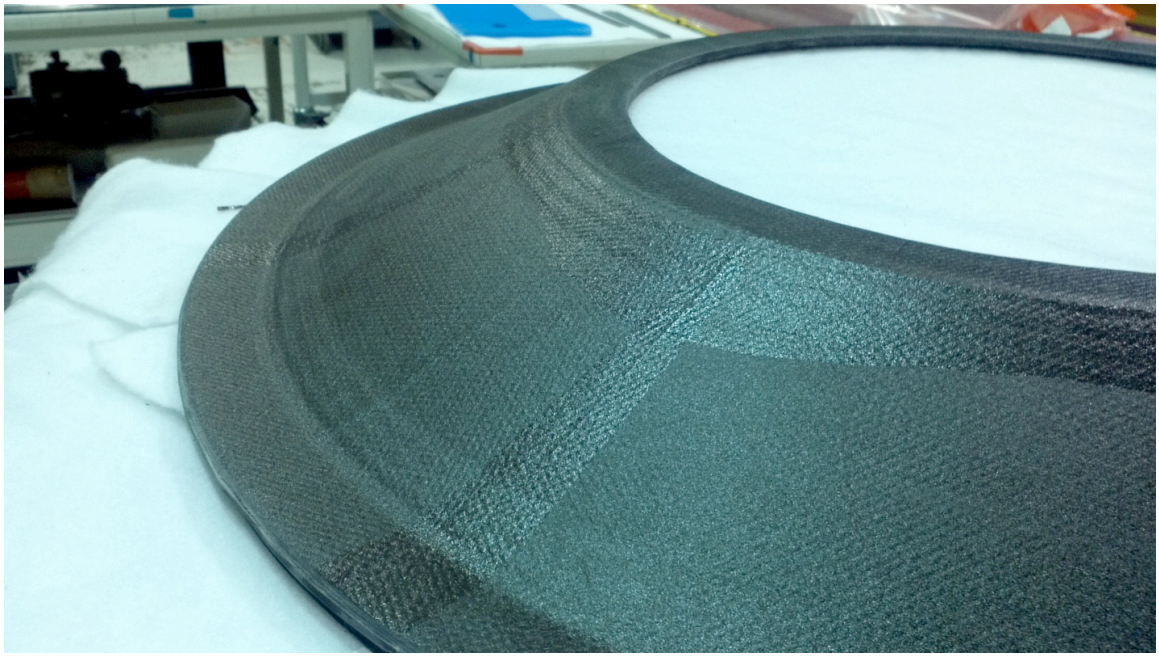

Figure 74 : First article transition cone after the curing is complete. Machining remains to be done.

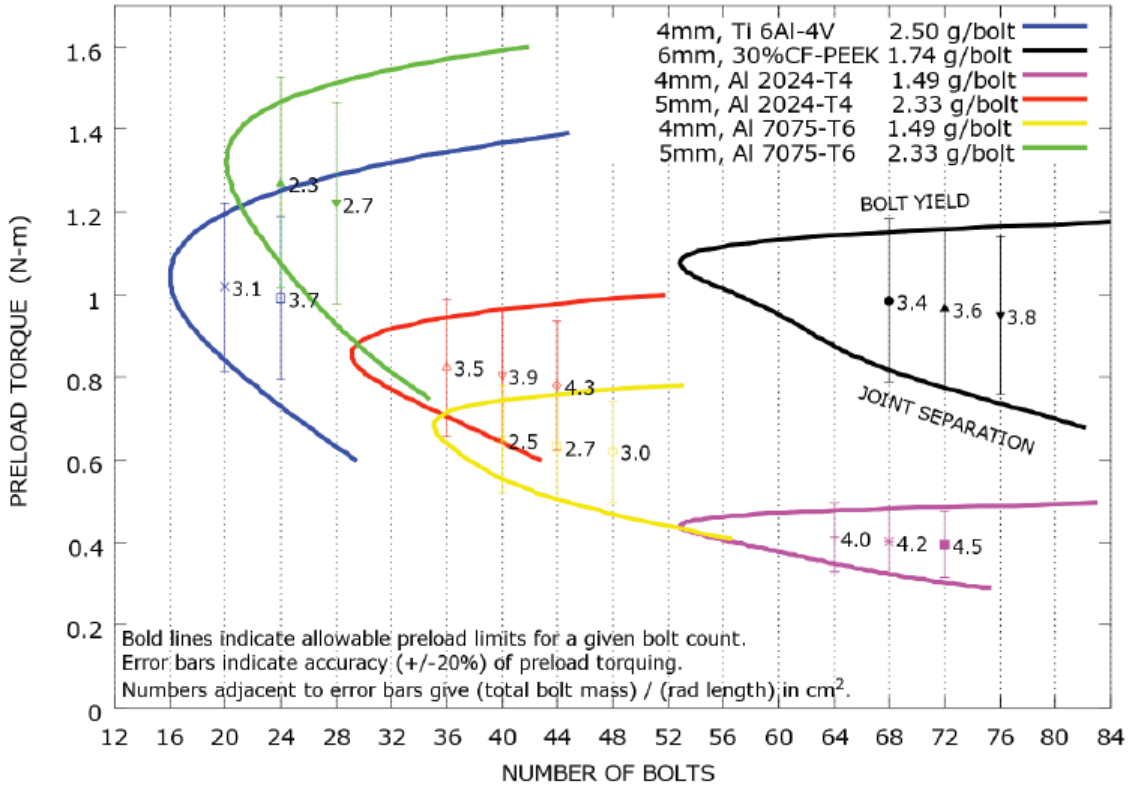

Figure 75: Number of bolts.

The flanges are CN-60 so the allowable pre-load is set to a value below the compressive strength of the composite. Factors of safety against bolt-flange yield and gap separation were calculated—the configuration space of the designs investigated are shown in Figure 75. Bolted joints are very robust when designed against joint separation with adequate preload, and yield of either the grip or bolt. The curves in Figure 75 show these envelopes—the top part is indicative of bolt/grip yield, and the bottom portion is joint separation. Each point in the chart represents a specific selection of bolt-count, material and diameter, and the required nominal seeting torque to place it mid-way between joint separation and yield. The error-bar about that point represents a preload error typical for torque based preload. It is important that the error bar lie within the curve. From this survey, two choices were clear—24 M4 Ti, or 28 M5 7075 fasteners. There is a preference for 24 as half the bolts can be aligned with dead regions of the STAR TPC. For completeness, samples of each fastener were fabricated and tested.

Termination Ring

The termination ring is shown in Figure 76 installed on this WSC with the stiffening plate. The termination ring is intended to replicate the mechanical interfaces of the current cone system, i.e. the mounts to the TPC and to the existing installation rails used to insert the cone system. It is a machined aluminum ring that will be bonded to the structural shell. The termination ring contributes to holding the ESC/WSC round. Its radial extent is limited to be the same as that of the current cone's termination rings. An auxiliary radial stiffening plate is required at each end to help resolve the point loads into the shells of the ESC/WSC. The interface to this stiffening plate is intended to be compatible with all service exits and independent removal of the stiffening plate for various service scenarios. The west stiffening plate will be removed to accommodate removal/installation of FGT disks. The implication is that the interface must 'force' the transition ring to be round via tapered pins to maintain the global shape/deflection of the IDS should one of the stiffening plates need to be removed and re-installed.

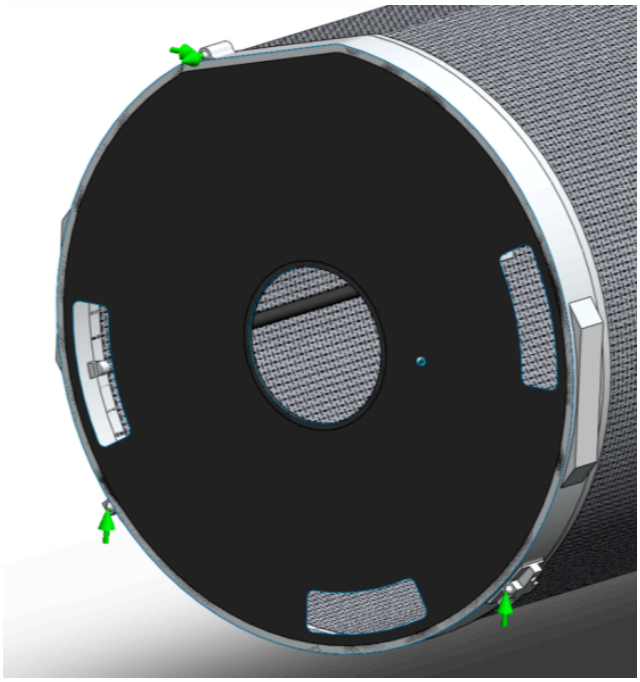

Figure 76: End of the WSC showing the aluminum termination ring, the stiffening plate, and the attachment points for suspension from the TPC wheel.

Support of the IDS to the STAR TPC is a functional part of the termination ring. As mentioned above, this will be modified to allow for more independent adjustment of the IDS position. Currently, all motions are coupled, i.e. are not independently orthogonal, and the current cone is over constrained in more than 1 DOF. The new support will be '4-2-1' i.e. 4 vertical, 2 horizontal and 1 "Z" constraint, so only over-constrained in the 'vertical' dimension.

OSC (Outer Support Cylinder)

The OSC spans the gap between the ESC and WSC and carries the moment load between them. It is designed to have the same amount of material as the current support structure beams, but distributed over a cylindrical region of volume. Its stiffness will match the current beams for vertical deflection, with the added benefit of also providing the same stiffness horizontally.

The first article OSC installed will serve solely as a structural support. The final version of the OSC will have support mounts for the SSD and any strain reliefs for its services. The cylindrical OSC allows the SSD ladders to be directly mounted to the outer surface of the OSC. The relatively massive aluminum support rings used in the previous support structure for the SSD will be eliminated.

MSC (Middle Support Cylinder)

The MSC is a stepped cylinder in form and is the primary integrating structure for the PXL and IST detectors. It is supported by the ESC via its west end. It is composed of a larger cylinder (PIT) and a smaller cylinder (PST) coupled together with a transition plate. The transition plate is the primary interface to the IDS.

The PST supports the IST, PXL detector and new beam pipe. The IST is supported on its outer surface via individual stave mounts as shown in Figure 77. The PXL detector is supported by kinematic mounts, integrated into the MSC small cylinder (PST). The beam pipe is supported on both ends of the PST, on the west end by a flange and the east end by a longitudinal plate, integrated with the transition plate, that allows for longitudinal expansion during bake-out.

The PST is cantilevered off of the ESC via the transition plate, which is attached to the PIT. The larger cylinder (PIT) supports the IST services on its outer surface and the PXL insertion rails on the inside. The length of the PIT will be optimized to facilitate PXL insertion. The PIT will have the same inner diameter as the OSC, minimizing tooling for shells and flanges.

The MSC also performs as an environmental enclosure for the PXL system, forming the return ducting for the PXL air cooling system. The IST will be on the outside and in a separate gas environment. The support of the beam pipe on the far end of the PXL detector (west) will also serve as the gas return/seal for the PXL environmental gas.

The FGT requires an enclosed volume for its cooling air, which is currently a separate structure. This is integrated into the IDS thus providing a support point for the west end of the MSC. The FY11 installation will require a baffle on the 3 inch diameter beam pipe to form the enclosed air volume, until the new beam pipe is installed in the summer of FY12.

3.5.5. Comparison to Requirements

The IDS is a deflection driven design. Its major loads are all induced by gravity, by the mass of the detectors within its volume. It is the position and stability requirements of the detectors and

beam pipe which drive the requirements of the IDS. All detectors, including the beampipe have similar requirements on build tolerance of approximately 1mm in the X-Y plane, the STAR coordinates transverse to the beam. The Z coridnate is the beam direction and the Y coordinate is the vertical coordinate. The pointing accuracy of the TPC is about 1mm. The HFT detectors can not be surveyed once installed into STAR. Only the FGT can be surveyed inside the IDS, when the IDS is in STAR. The lack of internal survey after installation requires that the absolute gravity sag of the fully loaded IDS, should be less than 1mm to simplify survey requirements, and allow a budget for internal assembly tolerances which cannot be surveyed.

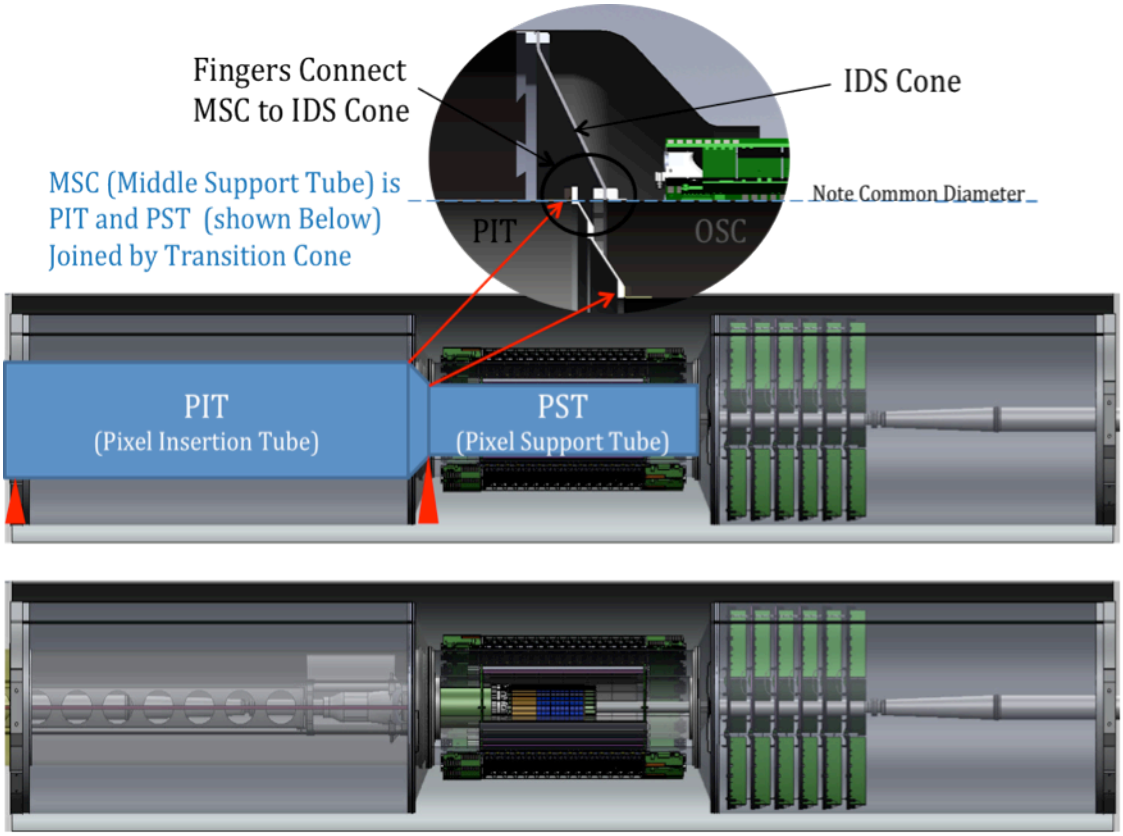

Figure 77: Middle Support Cylinder.

The overall deflection of the IDS was studied and iterated using SolidWorks (SW). The geometry of the cones in the SW CAD model used for the iterative design studies was aimed at easy modification of the CAD Geometry, not fabrication with composites. The stiffness of the IDS is most sensitive to the stiffness of the Cone Structures. Composite fabrication is a lamination process, the curvatures at flanges, and local transitions in thickness needed to be accounted for. These are easily handled in ACP, but the design of the Cone was necessarily changed to ease fabrication, with the changes in thickness now handled by ACP, not by changes in the CAD Model. It was useful to make a full Isotropic analysis in ANSYS with the new geometries and materials to verify the ANSYS Geometry and Results with the SW Simulation model before going to a full ACP model where the geometry is more difficult to change.

Using the Composite Material definitions with ACP, the same geometry, with better detail in the flange and cone regions yields the deformation results shown if Figure 78. The maximum deflection of the OSC is 0.6mm. This deflection will be used in the stability analysis.

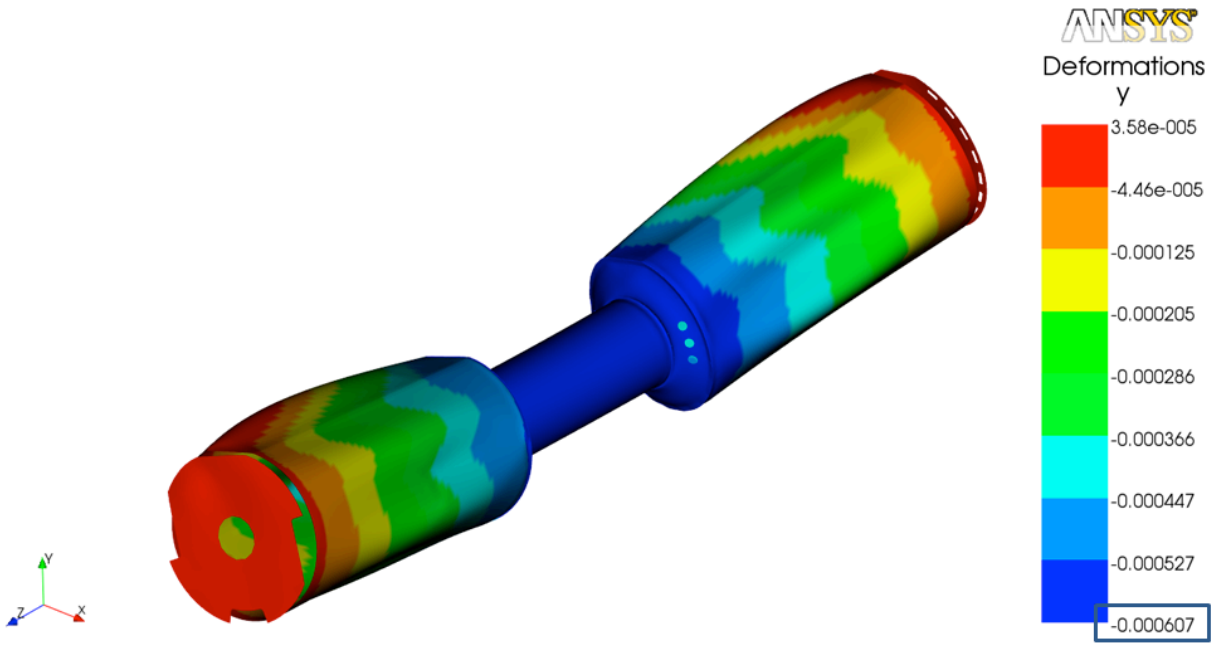

Figure 78: Max OSC Deflection, Full Composite Material Definition, Final As-Built Geometry.

The detectors have positional stability requirements. The FGT places the most stringent requirement on stability. An excerpt of it's interface document showing build and stability requirements for the FGT is shown in Figure 79. All the other detectors have similar documents. The FGT uses beam constraint (knowing beam position) for its tracking. The beam stability is ~100microns, so this sets the scale of the stability requirement. The IDS should not detract from the inherent resolution of the FGT; the IDS stability motions under induced vibration should not be an appreciable fraction of 100microns.

Build Position

Element to be positioned	Direction	Mechanical Tolerance	Relative to	Survey Tolerance	Relative to	Notes	Ref
-	-	+/- mm	-	σ mm	-	-	-
Survey marker on bearing housing	X	1.00	WSC	0.500	TPC		
Survey marker on bearing housing	Y	1.00	WSC	0.500	TPC		
Support disk back surface	Z	1.00	WSC	0.250	TPC		4
Support disk back surface	Z	0.50	next support disk	0.500			
Support disk back surface	Rx	1.00	Beamline	0.250	Beamline	At max R	4
Support disk back surface	Ry	1.00	Beamline	0.250	Be	At max R	4
Readout plane	Rz		WSC				

Survey requirements based on sigma of measurement

Mechanical tolerances relate to manufacturing and tooling tolerances

Stability

Element to be positioned	Direction	Short Term	Relative to	Long Term	Re
-	-	RMS mm		mm	
Entire Detector	X,Y	0.10	IP		
	Z	1.00	IP		

RMS vibration of FGT this drives the stability of the IDS

Figure 79: Position and Stability requirements of the Forward GEM Tracker

It is difficult to run a quantitative vibration analysis with a full Finite Element Model with RMS stability as output, however simplified models exist which over predict the magnitude of the RMS vibration. For the IDS, the maximum global deflection is the gravity sag of the OSC relative to the mount-points, which coincides with the mode shape of the first fundamental mode (F0). The

fundamental frequency is closely approximated by $F_0 = {}^{1}/_{2\pi}\sqrt{g/\delta}$ where δ is the gravity sag of the OSC. This equation is plotted in Figure 80 as the blue line. Using 0.60mm, yields a frequency of 20Hz.

The shaded region the figure above represents the bounds of the expected PSD (Power Spectral Density) of the imposed vibration environment within STAR.

$$\delta_{RMS} = g\sqrt{\frac{PSD \cdot Q}{(\pi \cdot f_0)^3}}$$

In the equation above the PSD is in units of g^2/Hz (power/cycle). The shaded region is bounded by the PSD range of 1 X 10^{-8} and 1 X 10^{-7} g^2/Hz which bounds the peaks and valleys of the PSD measured in STAR near the mount points of the IDS. Q is the 'Quality Factor' which is inversely proportional to the damping factor of the Material. Here, Q is 12.5; equivalent to a damping factor of 4% which is typical for composite materials, and bolted joints. The anticipated RMS vibration of the IDS with ~0.6mm gravity sag (20Hz F0) will have less than 10μ RMS vibration—well under the 100μ stability requirement.

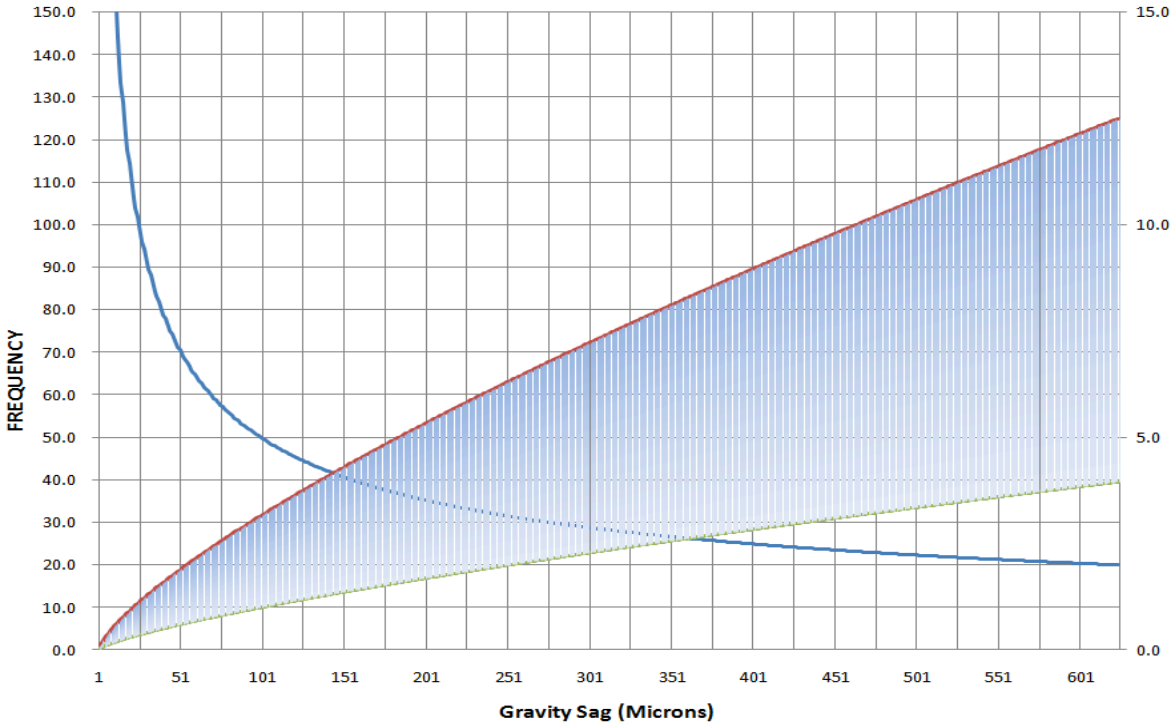

Figure 80: Vibration and response as a function of gravity sag (RMS Magnitude on Right in microns).

A discrete comparison to the measured PSD was conducted. The Blue Line in Figure 81 represents the response of a Simple Harmonic Oscillator (SHO) with equivalent damping, as convolved with the input of the PSD, as a function of frequency of the SHO and PSD. The PSD, plotted in appropriate units, is represented in red. This plot agrees with the ranges presented in Figure 80.

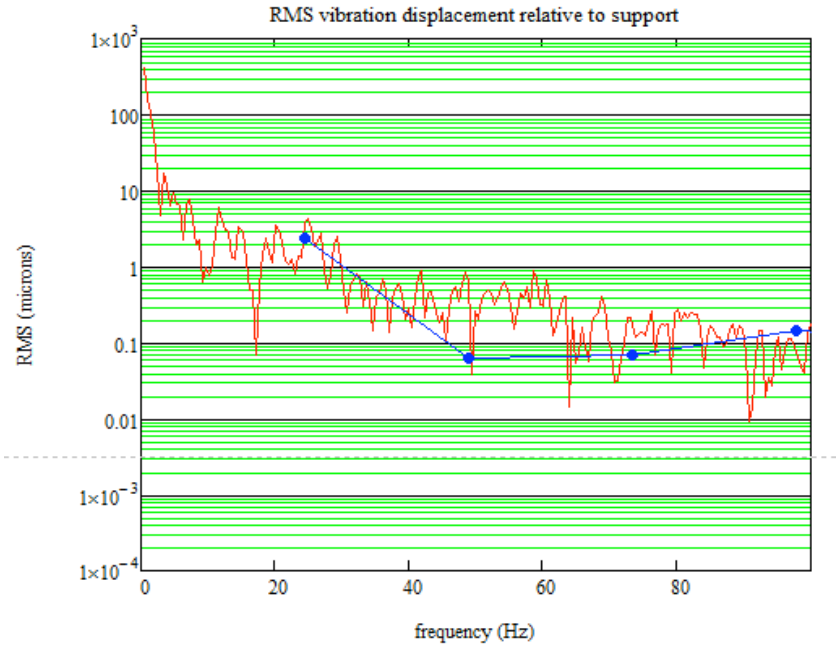

Figure 81: Numerical Convolution of idealized SHO of equivalent Q with PSD measured in STAR

Insertion of the IDS into STAR

The IDS will use the same tooling and supports that have been used in the past for installing/removing the existing support cones for the SVT and SSD detectors. The SVT lifting fixture has been reviewed and found to meet the requirements of the IDS. The current procedures will be modified to provide for safe removal of the cones and installation of the IDS.

PXL Insertion

The PXL is designed to be installed into STAR when the STAR detector system is located in the operating position in the intersection region. The east pole tip must be installed for the designed PXL insertion tooling to function. The PXL detector can be installed within a period shorter than 24 hrs, preferentially 8 hrs. Modifications are required to adjacent detectors and equipment including changing the beam pipe supports, modifying the Beam-Beam Counter (BBC) support for quick removal/reinstallation, providing for a means to transport the PXL detector into the IR from the clean room, modifying the east start counter (uVPD) support bracket, and providing a work platform for performing the removal/installation. The integration subsystem will provide these modifications for PXL.

Assembly/Testing Area Requirements

The support structures and detector systems need appropriate areas for testing and assembly. The "clean room" at STAR meets most of the initial assembly and detector testing needs. Minor improvements have been identified and completed for the summer FY11 installation of the FGT and IDS. Planning has begun for implementing additional changes for the engineering PXL run (Summer FY12) and the complete HFT (summer FY13). The initial plan is to outfit the clean room with conditioned air, racks for electronics, and locations for cooling systems for the detectors. The smoke detectors in the room will shut all power off if they detect smoke. Fire suppression is planned to be installed in FY2013, if necessary.

The final assembly in 2013 will require additional assembly space. A simple area using a portable garage with lights, smoke detectors, and power is planned near the clean room.

Beam Pipe

The beam pipes for STAR are the responsibility of the Collider Accelerator Department (C-AD). However, the very close proximity and interfacing of the beam pipe with the needs of the HFT requires that STAR/HFT personnel be involved closely with the design of the beam pipe and its supports. Technical expertise for the beam pipes is provided by the C-AD vacuum group and the HFT Project mechanical engineer.

The initial installation of the IDS will use the existing STAR beam pipe. Simple supports will be designed for installation in the ESC and the WSC for supporting the pipe. The precise positioning of this beam pipe is not crucial due to the large diameter, 7.64 cm. The C-AD vacuum group has provided engineering details necessary for the safe handling and support of the existing beam pipe. Figure 82 displays the stress in the beam pipe during the hot nitrogen gas purge that is used after the beam pipe has been let up to atmospheric pressure. In the example shown in Figure 82 the beam pipe is supported only at the extreme ends and at the TPC wheels (ends of the IDs). The assumed temperature of 200°C for the beam pipe is an well above the upper limit for the hot gas purge. There is a safety factor of 6 at 200°C . A more realistic average temperature for the beam pipe during this process would provide a safety factor of nearly ten. The stress on the beam pipe is the result of compression of the bellows at each end of the beam pipe.

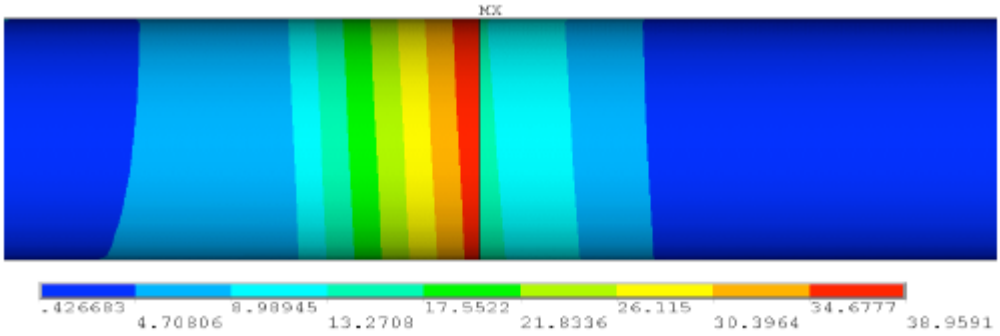

Figure 82: Von Mises stress (MPa) near the Be-Al joint in the existing STAR beam pipe.

The new beam pipe will have an I.D. of 4 cm and is expected to be delivered to BNL in August of 2011. After acceptance testing at BNL the pipe will be stored until it is ready to be NEG coated. The beam pipe has been designed to be heated to 250° C to account for incremental bake-out temperatures over the lifetime of the beam pipe. The PXL detector will be removed prior to any bake-out of the beam pipe. The central portion of the beam pipe is shown in Figure 83. The design is essentially the same as the new beam pipe that was installed in PHENIX in the summer of 2010 and successfully used in RHIC Run11.

Bake-out jackets for at least the PXL section (small diameter) of the beam pipe will be inserted and removed. The insertion mechanism will be a simplified version of the PXL detector insertion device. Other sections of the beam pipe will have removable bake-out jackets or integrated bake out jackets, similar to those installed on the Be beam pipe of ATLAS. Integrated bake out jackets are heaters laminated directly to the beam pipe, and insulated to keep heat leakage to a minimum.

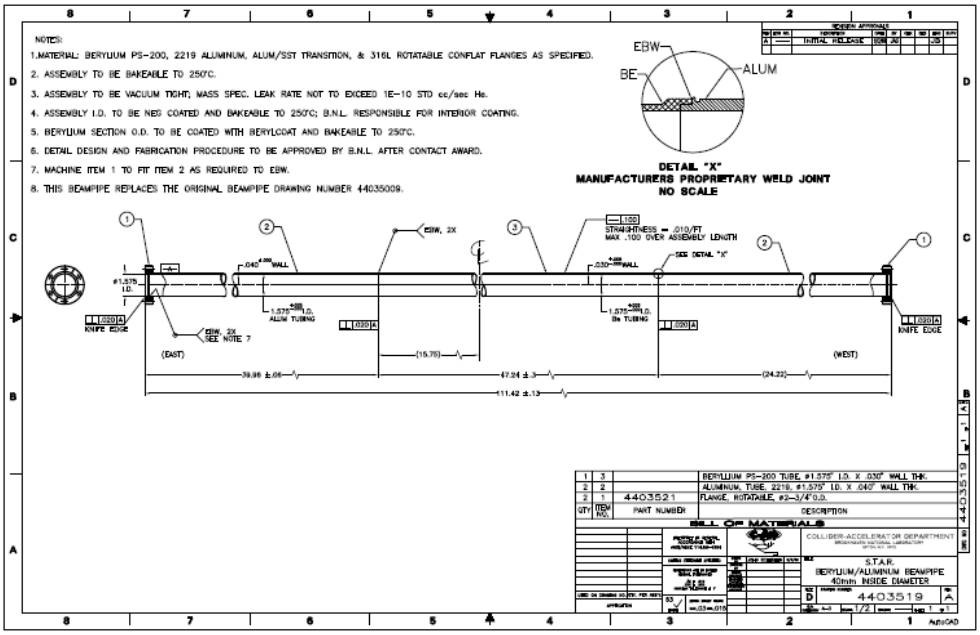

Figure 83: Small diameter beam pipe with Be mid-section.

3.5.6. Safety

The integration subsystem will work with each of the detector subsystems to ensure that the designs and work processes at BNL meet the requirements of the BNL SBMS. All designs will be presented to the appropriate C-AD committee for review and approval. Typically, the C-AD Experimental Safety Review Committee (ESRC) has the responsibility to review all experimental designs. There will also be independent reviews of the mechanical structures when appropriate.

3.6. Software

This section contains the description of the software elements required for the successful processing and analysis of the acquired raw HFT data. Since the HFT is an upgrade detector of the STAR experiment, its software needs modules to be incorporated into the existing software and computing environment of the experiment. After a brief discussion of STAR's software environment, we list and describe the online, offline and simulation modules and tools that are required to be developed for the HFT. We will finish with a discussion of resources and institutional software responsibilities and commitments.

3.6.1. STAR Software Environment

The STAR software environment comprises of a set of tools (development, simulation, production and analysis environment), mainly in the form of plug-in software modules in a ROOT – based backbone interface. At the same time it provides the data model and the coding standards and the data model for new module development and integration in the top-level shell scripts. Each detector subsystem is responsible for the development of all modules necessary for its successful operation. New, major pieces of code need to be reviewed and approved before insertion in the main repository. This work is coordinated with the rest of the experiment through a designated software representative from the group. At the same time there is a software infrastructure group based at Brookhaven National Lab (BNL-core), that maintains and manages critical pieces of code (tracking, calibrations, databases) and also provides help with the integration of new software in the system.

Online Environment

The online software primarily ensures the data integrity during data acquisition via appropriate detector monitoring and sample event reconstruction. Beyond these basic but important tasks, and as computer processing capabilities improve dramatically, more and more formerly offline tasks move to the online environment. One such task is the hit finding in the STAR TPC. Discussion has started on the possibility for online (pre-) tracking in the TPC. This is of particular interest to this group since we plan for on chip PXL clustering and hit finding for the PXL detector.

Offline Environment

The offline environment consists of the event reconstruction software packages. This starts with the raw data as input and through proper calibrations it proceeds with detector cluster/hit finding, integrated tracking, event vertex finding and event information writing on DSTs.

3.6.2. Online Software

The online software serves as a tool to monitor detector performance. It is also used to perform online calibrations where possible. Online software is detector specific and is described in Section 3.2 for the PXL, in Section 3.3 for the IST, and in Section 0 for the SSD.

3.6.3. Offline Software

Hit Reconstruction

The Cluster/Hit finder is the first piece of code applied to the pedestal subtracted raw information from the IST and PXL detectors.

In the IST detector this will be a standard search for all fired strip-lets, i.e. all strips with a pedestal subtracted ADC value above a cut/threshold value (typically a value two to three times the strip noise-RMS level. Groups of adjacent strips that are fired will be clustered and further analyzed by a peak finding program for one or more possible hits. Every such 'hit' is then first going to be assigned a set of local/wafer coordinates based on the strip's position on the wafer. This will be followed by a local-to-global transformation to STAR global coordinate system (detector hit information needs to be saved in global coordinates), which is usually done via a series of partial transformations (wafer to ladder, ladder to shell, shell to detector, detector to STAR). This is common practice in silicon strip detectors and the MIT group, which will build the detector, has extensive experience in this area.

In the PXL detector the first steps (Cluster/Hit finding) are incorporated on the chip's logic, i.e. done online during data acquisition, as discussed in Section 4.2. The local to global transformation process is identical to the IST even though the partial transformations will be different in order to incorporate the specific geometry and the specific hardware-implemented alignment features of the PXL detector (see discussion on Alignment below and in Section 4.2).

Tracking

The current STAR reconstruction environment provides a Kalman-filter based integrated tracker. This tool is in principle ready to accommodate and integrate the IST and PXL hits, with their proper error per weight, in its environment. In reality work and close collaboration with the BNL-core group will be required to tune the tracker's parameters and optimize its performance. For example it has to properly handle the high precision information coming from the PXL layers. Also, there is a need to develop methods to deal with the path ambiguities in the SSD and IST (effective strip 'hits' with relatively large errors in the long strip direction), as well as dealing with the ghosting in the PXL detector due to out of time events in a high luminosity environment. Dealing with the latter two problems of tracking/ghosting will require studies that use a several-passes tracking approach and/or knowledge of the triggered event vertex obtained from a first-pass (or quick) vertex finder. This is a critical item, which will finally determine the physics performance of the system and therefore needs special attention and effort.

Event Vertex Reconstruction

Currently STAR deploys two different event vertex finders during event reconstruction, one for heavy ion and one for proton-proton collisions. Each of them is specifically tuned to perform best in these completely different environments (high multiplicity w/out pile up in heavy ions and low multiplicity with high pile-up in p-p). In a typical heavy ion collision the TPC has to cope with events of relatively large multiplicity and virtually pile-up free whereas in p-p one needs to extract the primary vertex from a few primary tracks surrounded by a thousand of out of time (pile-up) tracks. As a direct consequence of this fact STAR uses a Minuit-based event vertex fitter (with a seed finder) in heavy ion collisions. For p-p the vertex fitting procedure is based on a chi-square minimization method but, most importantly, the information from fast detectors is

used to select (tag) the tracks that belong to the triggered event. Only these tagged tracks participate in the event vertex-fitting step.

In the RHIC-II era's increased luminosity there is going to be pile-up in the TPC but most importantly in the two PXL layers of HFT due to the relatively large integration time of the detector (see Section 4.2 and also *Pileup* discussion below). This will be the case in both p-p and heavy ion collisions. The SSD and IST are assumed to be pile-up free even for the highest rate p-p collisions. The presence of these two (as well as the other) fast detectors will require a new, revised version of the vertex finder that will combine the best features of both current finders. At this point we do not anticipate the need for any new functionality, just the need for tuning and QA-ing the new/combined finder.

We should note here that the mid-term plans of the reconstruction/infrastructure group include the deployment of a Kalman filter-type vertex finder, which at the same time will do the primary track fitting. In high multiplicity events (>30 tracks or so) one can perform without loss the vertex finding/fitting and primary track fitting (i.e. fitting global tracks with the vertex as an extra point on track for tracks with DCA within a cut value, e.g. currently 3 cm, from the vertex. This will be revised in the HFT era due to much higher precision in pointing.) in two separate steps. In low multiplicities it is generally better if one performs a simultaneous fit of primary tracks and event vertex. This is worth exploring. Let us remember that the larger fraction of the secondary/decay vertices we are trying to resolve are in the range of 10-100 microns and any improvement in determining the event vertex (the most important single reference point in the event) is indispensable.

Secondary/Decay Vertex Reconstruction

The reconstruction of short-lived particles in a collider environment is an extremely challenging task. The key measurements of HFT involve the reconstruction of D- and B mesons with typical $c\tau$ in the range of 120 – 500 microns, and Λ_C with a $c\tau$ of 60 microns. The lack of a Lorentz boost typically results in mean decay distances of about half the $c\tau$, for decays at mid-rapidity of a properly p_T weighted sample. For example, the anticipated mean p_T for D^0 mesons in Au+Au collisions at RHIC is about 1 GeV/c. This is a conservative estimate taking into account expected high p_T suppression effects. The $\beta\gamma$ factor for a mid-rapidity D^0 is 0.54 and thus its mean decay distance ($c\tau$ of 120 microns) is about 65 microns. For a 1 GeV/c Λ_C baryon this will be about 30 microns. This environment demands the highest level of sophistication in the methods used to reconstruct the decay/secondary vertices.

Up to now, the STAR secondary vertex reconstruction code had to deal with decay vertices of strange particles, typically in the few centimeters range. For those distances, simple geometrical reconstruction models coupled to crude, fixed value cuts were sufficient. Only a recent effort to reconstruct D mesons with the SVT, the first generation silicon vertex detector in STAR, started deploying decay vertex fitting techniques using the full error information of a track, on a track-by-track and vertex-by-vertex basis (sometimes also called μ-Vertexing). Cuts like the decay length are not fixed values but rather a number of standard deviations of the fitted value. This way the cuts are less biased especially the one, like DCA, which have strong momentum dependencies. This work, currently still under development, will be the basis of the modules deployed on the HFT data. These important software modules are to be developed, as they are a key piece of the new software.

Databases – Calibration and Alignment

The accurate monitoring and recording of the state and the position of the detector inside the STAR apparatus is of outmost importance as it directly impacts its performance. Calibration is the online and offline task of monitoring the state of the detector. The online part (often referred to a slow controls) gathers information of the detector in-situ, usually during running periods. Such information might be temperature or position of elements, pedestal files etc. This information is stored in a Database with a timestamp. The slow controls for the SSD, IST and PXL detectors are discussed in Sections 4.4, 4.3 and 4.2 respectively. The offline part of the calibration includes also software methods used to check e.g. the position of the detector elements using tracking information. The results of these procedures are stored as updated values in specific bank in the Database and are used in the massive offline physics production reconstruction passes.

The task of Alignment is a very demanding one especially for the PXL detector where one would like to perform/know the positioning of the detector elements with offsets and tolerances to within a few microns.

The alignment of the SSD and IST is not a challenging task provided good survey data has been collected of the detector's elements beforehand. The in-situ alignment will be done with software techniques (global and/or local alignment) and there is previous experience on this in the collaboration. All it is required is to bring the SSD (IST) hits within the TPC (TPC+SSD) track projection errors to the detector layer, typically around 100 microns or so. Global alignment techniques usually yield results accurate to about 10 microns using a set of only a few hundred thousand tracks. Rotations are also typically kept to a fraction of milliradian.

In the PXL detector this task is more difficult and the designers of the detector decided early on to incorporate 'hardware' techniques in order to minimize element displacement in-situ. The PXL detector is designed with a 20 μm 'envelope' error, i.e. maximum allowed displacement in-situ. To achieve this various sophisticated methods have been developed, e.g. interlocking, easily replaceable pre-surveyed shells with extreme precision on-bench survey data. Details on the method and the specific hardware implementation can be found in Section 4.2.

Despite this excellent 'hardware pre-alignment', software methods will have to be deployed in order to both check and fine-tune the in-situ information of the detector elements. There are two categories of software alignment techniques, the so-called Global and Local alignment.

The *Global* alignment uses TPC (+SSD+IST) track information on a statistical basis in order to obtain systematic silicon detector rotations and shifts. Typically a 'rigid body' model is applied (i.e. ignoring possible ladder twists, sagging effects and wafer non-planarity) and a misalignment model is introduced. Then a Taylor expansion with respect to misalignment parameters (3-D shifts and 3-D rotations) is performed looking for deviations of measured hit position from predicted primary track position on a measurement (wafer) plane. The track prediction comes from the detector(s) used as reference, e.g.\ initially the TPC alone, and later the combined TPC+SSD (+IST) tracking. In the next step, from the hit deviations distribution, a misalignment parameter has been calculated as a slope with a straight line fit. A global least-squares fit is also simultaneously performed on all available information. The method is applied iteratively until the fitted parameters reach stability. This global method was first applied to TPC+SSD+SVT data in STAR and it is well developed and understood. It will serve us in the IST alignment but it will need modifications for the PXL detector. This is because the PXL elements (wafers) on a ladder will have deviations from the 'flat plane' hypothesis.

In a *Local* or *Self*-alignment method one aims at the most precise *relative* placement of the detector elements. In this procedure only high precision hit information is used coming

exclusively from the detector under local alignment. A successful method using the event vertex constraint was developed and tested on simulations by the BNL-core group and this should be further developed into a working module with data for the HFT complex.

3.6.4. Simulation Framework

The current simulation framework in STAR is based on GEANT-3.0 with custom script extensions to facilitate detector geometry implementation and event generation. It also includes event generators like HIJING, PYTHIA, Phase-space etc. that are interfaced to GEANT. This framework is soon to be abandoned and will be replaced by a ROOT-based geometry and tracking package (VMC, Virtual Monte Carlo). Nevertheless, we are still using it and we will continue to do so in the immediate future. The tasks, and therefore software modules one needs to develop here are: a) the **detector geometry** definition, b) the **detector response** packages (fast and slow simulators), c) track **embedding** in real/raw events, d) a hit **pileup** handler, e) the Association Maker and structures for **evaluation** purposes, and f) Physics **analysis** code (performance, physics etc) capable of handling and evaluating the resulting information. Our group will have to contribute modules and effort in all these categories. It is worth mentioning here that besides this full and detailed simulation chain the group has developed very useful tools for quick estimates of various detector configurations, resolutions, layouts etc. These tools, sometimes referred to as 'hand calculations' or 'fast Monte Carlo' will keep playing an important role when either a quick turn around is needed or for cross checking purposes.

Detector Geometry Definition

This task is to include in the GEANT-simulated apparatus of the experiment the latest and most accurate/realistic geometry of HFT (IST and PXL), since this is the only way to ensure reliability of the resulting efficiency numbers. This task also includes the definition of the active areas of the detector, the hit information and the global positioning matrices of the detector. It has been recently realized that for certain studies (e.g. layer optimization studies, overall tracking efficiencies, 'quick' feasibility studies etc), a simplified version of the geometry could be very useful, a version where average material thickness is included but without detailed outline of the discreet components (cables, ICs, ladder support etc).

Detector Response Simulators

The detector response simulation packages in STAR reside outside the GEANT framework. They are actually invoked at the event reconstruction step. Typically there are two or three categories of response simulators: a) *Fast simulators*, which smear the hit position coordinates and assign hit uncertainties based on parameterized analytical functions. The fast simulators run extremely fast and are good for quick studies that do not need detailed implementation of the detector. They are also relatively easy to implement; we already have an HFT fast simulator in place for all subsystems, b) *Slow simulators,* which simulates hits at the ADC level (usually obtained from sampling parameterized response functions. A slow simulator is a must when accurate acceptance and efficiency numbers are requested in physics analysis. A slow simulator is also used in embedding as discussed below, and c) *Very Slow simulators*, which track individual electrons through the detector body; from their generation to the readout. This is usually very time consuming and one utilizes this method only in small-scale productions in order to determine or verify the functions used in the first two methods.

A Slow Simulator for the IST Detector

The technology similarities between the SSD and IST (both silicon strip detectors with similar Si wafer thicknesses but with SSD being a double-side, crossed strip detector and IST single-side, shorter strip detector) could be beneficial in developing a slow simulator for the IST. The currently under development SSD code could be modified and adapted for the IST needs.

A Slow Simulator for the PXL Detector

The detailed simulation for STAR Heavy Flavor Tracker PXL silicon detector consists of 4 steps. First, use the information of a charged particle passing through the PXL as inputs. The information contains the particle momentum, incident direction, path length in the PXL, and the sum of electron-hole pairs it generates. The total number of electrons generated from charged track passing through the silicon sensor is calculated using a Bichsel distribution.[28] Second, build the geometry of the detector: one chip of 640 x 640 PXL array. One pixel is 30 μm x 50 μm x 30 μm, consist of four different layers from top to bottom: readout electronics layer, diode layer, epitaxial layer and substrate layer. Third, simulate the transportation of electrons generated in the PXL[29]: diffusion, recombination and reflection at interfaces between different layers. A Gaussian equation is used to describe the diffusion as a random walk process. The electron recombination rate is dependent on the different doping density of different layers. Finally, calculate the distribution of electrons collected in the PXL array as output signal. The left panel of Figure 84 presents the simulated pixel cluster shape from 1GeV charged pion incident at 45-degree angle. The right panel of the figure shows the comparison of the deposited number of electron profile from data [29] and simulation. The two results agree with each other very well. The major problem for this slow simulator is the speed. It takes about 20 minutes to simulate a single charged track and it comes mainly from simulating the electron diffusion process. This is too slow to be used in future large-scale simulation studies.

To significantly improve the speed while keeping good accuracy, we developed a simplified method. Instead of simulating diffusion process step by step for each single electron, we calculate the probability distribution function for each electron in a specific space location to be collected by different pixels. Since any electron generated in the PXL is independent from each other, by randomly sampling this probability distribution function, we can decide which pixel collected this electron or if the electron recombined before being collected. Following above steps, we collect the pixel IDs that absorb all electrons along a charged track and add them up to obtain the number of electrons deposited in each pixel. To implement this method, we built a fine 3-D grid in a single pixel and calculated the probability distribution function for electron produced from all grid points using the slow simulator. For any one electron from incident charged track, we directly use the probability distribution function for the grid point that is closest to its production point to determine the pixel ID that collected this electron. Since all pixels are identical, we only need to make coordinate transformation if any electron is produced outside the PXL where the grid is built and repeat the same operation to finish the whole simulation for a charged track. The speed of the simplified simulator is a few seconds per charged track. The accuracy depends on the granularity of the grid and can be very good with high granularity.

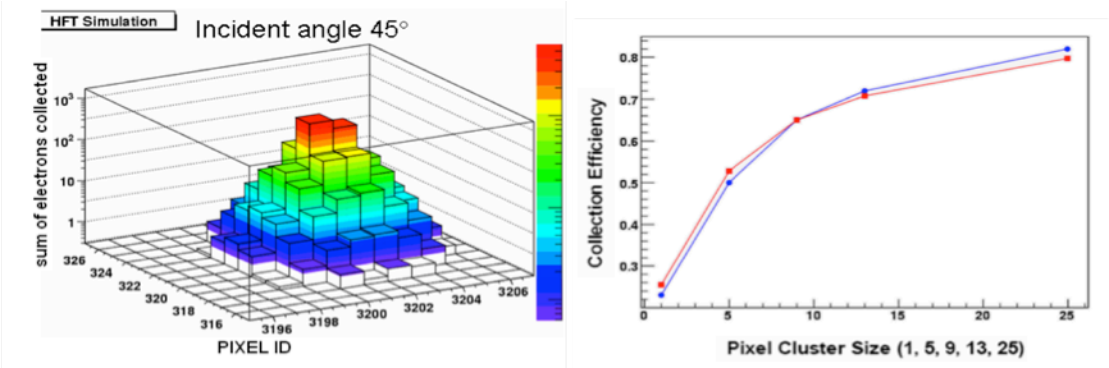

Figure 84: Left: Distribution of the number of deposited electrons on pixels from a charged pion with 45 degrees incident angle from the slow simulator. Right: Profile of the fraction of deposited number of electrons from simulation (blue) and data [29] (red).

Embedding and Pile-Up

The embedding of simulated tracks into the raw data stream (which provides the best 'background environment' for track/particle reconstruction and therefore the best way to estimate accurate efficiency numbers for physics analysis) has been around the heavy ion community for about fifteen years. It is the merging, at the raw ADC level, of a pedestal-subtracted event, for a given detector, with a few, slow-simulated hits. The resulting output is then passed through the reconstruction chain and the output is compared to MC input (this step is performed by the so-called Association Maker in STAR experiment). During the merging of real data with simulated hits and tracks one read the appropriate calibration tables so the dead areas of the detectors are properly excluded.

IST Embedding

As we mentioned above the IST could benefit from existing or under development SSD embedding code and adapt it with minor modifications

PXL Embedding and Pile-up Simulation

The embedding task in the PXL layers is more complex since cluster and hit finding is done online. Also, in simulations, one has to properly account for out-of-time events, Pile-up hits. At the projected RHIC-II luminosity of $50*10^{26}$ $cm^{-2}s^{-1}$ with vertex diamond with σ_z of 20 cm, a significant amount of pile-up from minimum-bias collisions will contribute to the hit density in the PXL layers for 200 μs integration time. The hit density at the first PXL layer will thus rise from 18 cm^{-2} to 40 cm^{-2}, and at the second PXL layer from 2 cm^{-2} to 4 cm^{-2}. This already includes rescaling applied to account correctly for contributions from UPC electrons.

Based on these numbers and similar to CD-0, a sample of minimum-bias collisions with proper primary vertex distribution was used to obtain a sample of hits in the PXL detector layers. Ten different sets were produced to account for fluctuations in pile-up hit densities. These were merged with the PXL hits in every simulated central Au+Au collision and used to obtain the results presented in Section 2.

Association Makers

The step of association comes directly after the embedding. Its basic functionality, which already exists in the STAR framework, is to correlate the MC input with the reconstructed output so one can calculate hit, track, decay-vertex etc finding efficiency. This is done either through the use of an embedded key (idtrue) in the hit structure or by 'proximity association' of reconstructed and MC clusters. The later one is less accurate and not suitable for our purposes. Currently the Association software generates a structure that contains enough correlated (matching) information to allow hit/track and partial decay-vertex evaluation. The current output is usable but not optimized for our purposes; one has to go through several steps in order to be able to perform a detailed evaluation. The current scheme will need to be modified or augmented to include vital information that will facilitate our work.

Analysis of Simulated Data

There are software modules needed exclusively during the evaluation of simulations, either full-event simulations or embedding. These are in general smaller, utility-type pieces of code. Most of these modules already exist in some form and it is a minor effort to adapt them to HFT.

3.6.5. Physics Analysis Framework

The physics analysis software is the most critical part in signal extraction. When it comes to physics analysis people use a diverse set of tools and methods to extract the physics signals, most of them developed by themselves. Most of the tools and infrastructure needed is either already in place or under development in current charm analyses. Here we will only indentify the broad areas of physics interests for the HFT mainly for the purposes of recording the institutional interests, responsibilities and commitments. These areas are: a) Charm-meson, b) Charm-baryon, c) B meson reconstruction and d) possible spin-related signals. These are the areas discussed in the next Section.

4. Acronyms

APS	Active Pixel Sensor
ARC	APV Readout Controller
ARM	APV Readout Module
CMOS	Complementary Metal Oxide Semiconductor
CDS	Correlated Double Sampling
DAQ	Data Acquisition
DDL	Detector Data Link (ALICE)
DRORC	Dual Readout Receiver Cards (ALICE)
FPGA	Field Programmable Gate Array
IDS	Inner Detector Support
IPHC	Institute Pluridisciplinaire Hubert Curien
IFC	Inner Field Cage
IST	Intermediate Silicon Tracker
JTAG	Joint Test Action Group
HFT	Heavy Flavor Tracker
LU	Latch-Up
LVDS	Low-Voltage Differential Signaling
MAPS	Monolithic Active Pixel Sensor
MCS	Multiple Coulomb Scattering
MSC	Middle Support Cylinder
MTB	Mass Termination Board
OFC	Outer Field Cage
OSC	Outer Support Cylinder
PCB	Printed Circuit Board
PEP	Project Execution Plan
PXL	PiXeL Detector
QCD	Quantum Chromo Dynamics
SSD	Silicon Strip Detector
STAR	Solenoidal Tracker At RHIC
SVT	Silicon Vertex Tracker
TPC	Total project Cost
TPC	Time Projection Chamber

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