Options for Intermediate Tracking in the HFT

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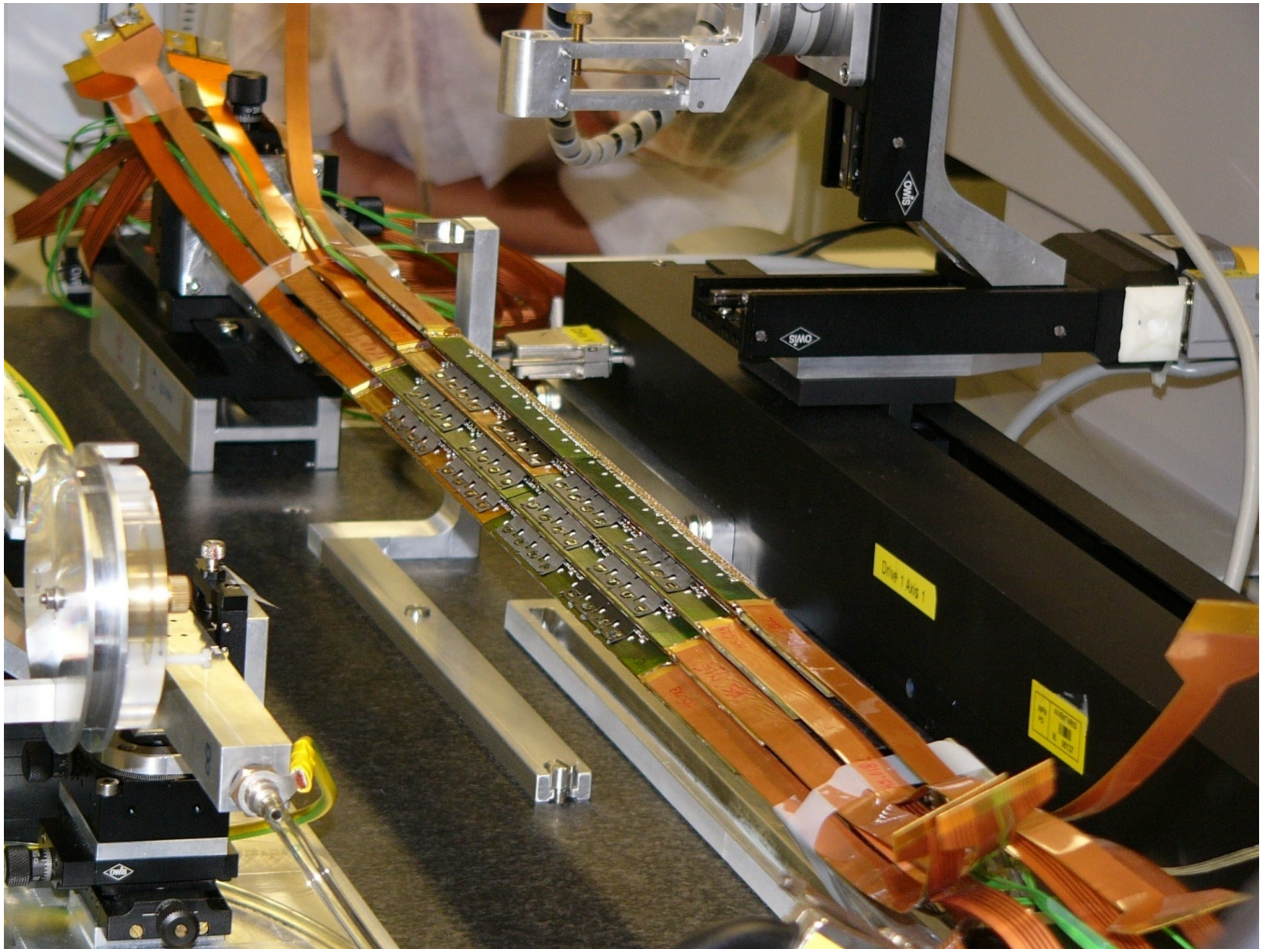
Three Excellent Technologies

- Alice style Hybrid Pixels
  - 50 x 425 μm mini-strips
  - 1% thick
- STAR SSD style double sided Si
  - 95 μm x 4 cm crossed strips
  - with charge sharing to remove ambiguities
  - 1 % thick
- PHOBOS style conventional strips
  - 60 μm x 4 cm crossed strips
  - 0.75 % thick per layer (1.5% for two)

ALICE – Hybrid Pixels … a well developed technology



Pixel dimensions:
$50\mu m$ ($r\ \phi$) x $425\mu m$ (z)

Front-end electronics:
CMOS6 $0.25\mu m$ process on 8" wafers, rad-hard design

Pixel ASIC thickness $\leq 150\mu m$

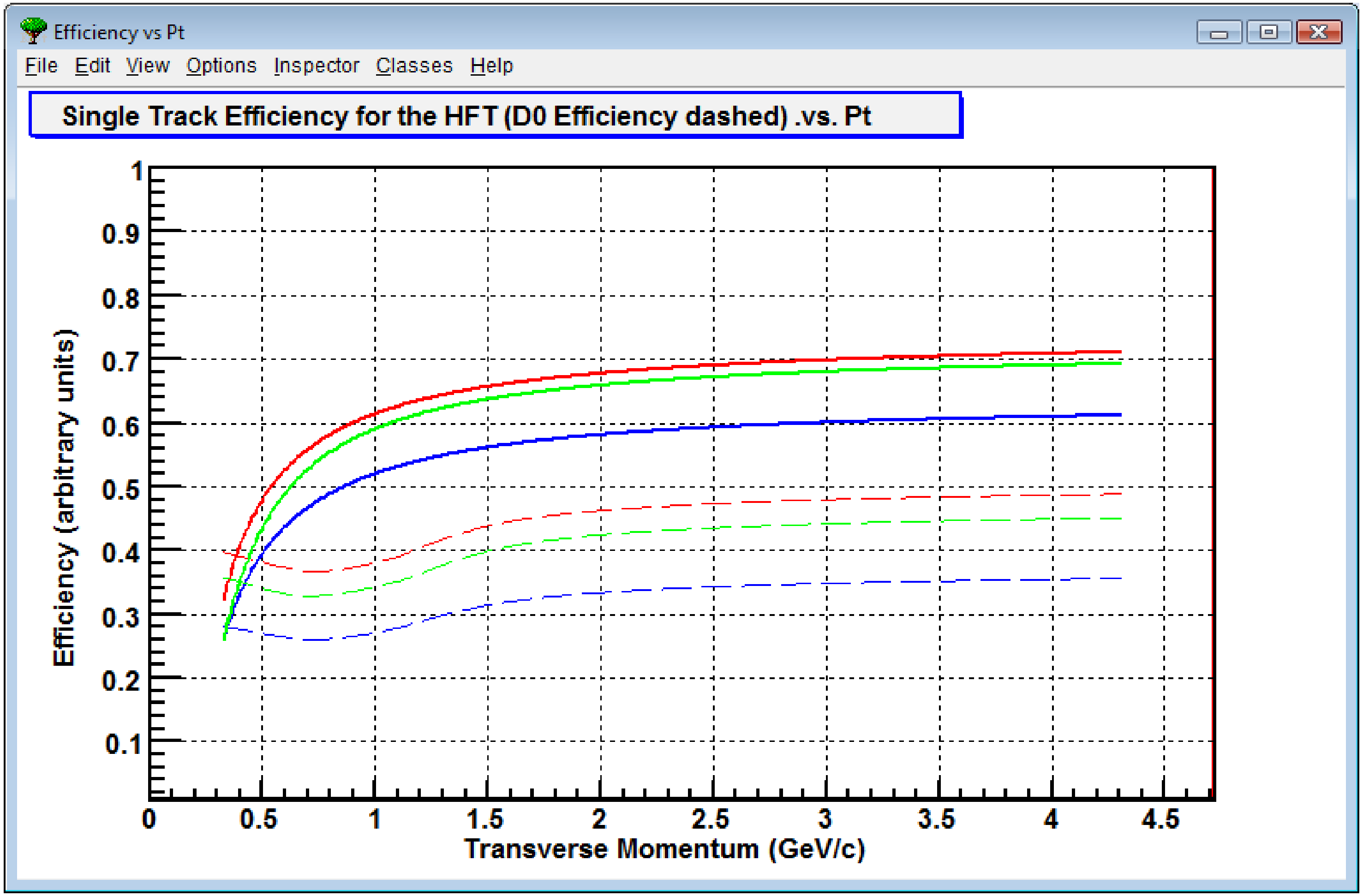
Si sensor ladder thickness $\leq 200\mu m$

Cooling:
water/C_6F_{14}/[C_3F_8 (evaporative)]

Material budget
$\approx 1.0\%\ X_0$
Si ≈ 0.35
cooling ≈ 0.3
bus ≈ 0.15
support ≈ 0.2

Occupancy $< 0.1\%$

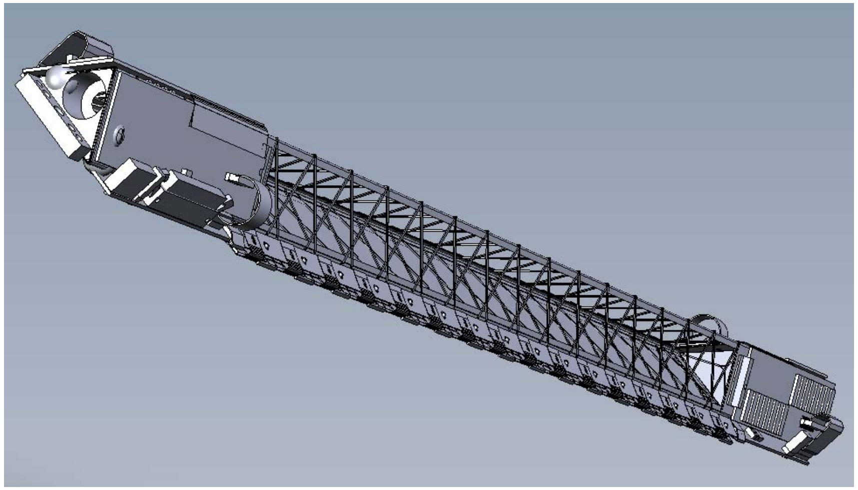
ALICE Hybrid Pixels at 12 cm radius (200 μsec HFT)

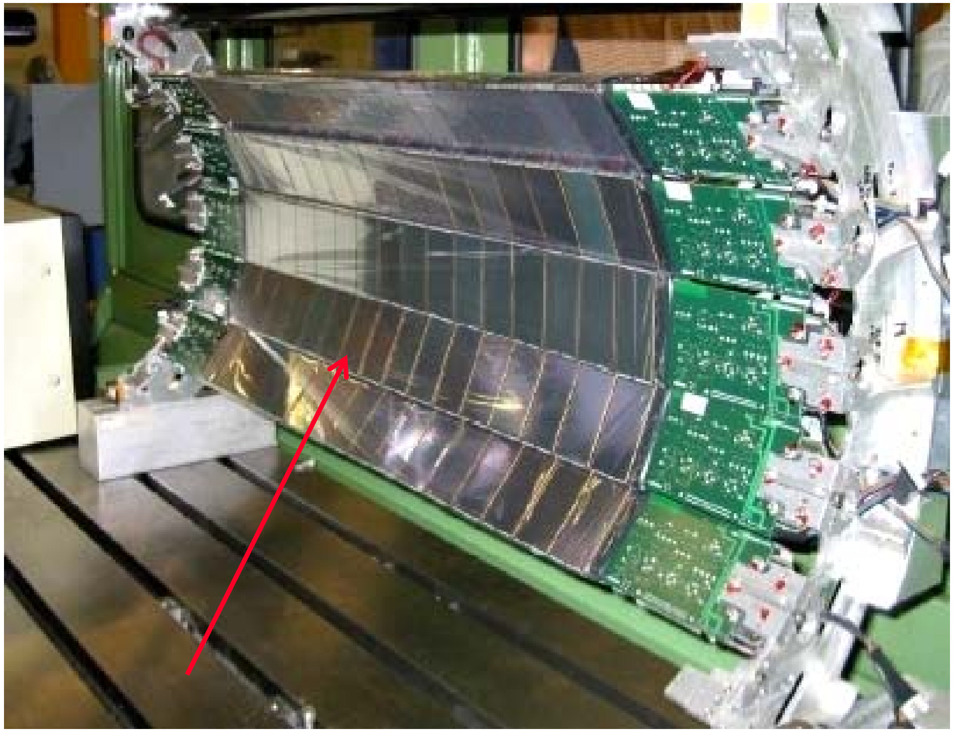


- vtx+pxl1+pxl2+ali+ist2+ssd+tpc (blue)
- vtx+pxl1+pxl2+ali+ssd+tpc (red)
- vtx+pxl1+pxl2+ali+tpc (green)

Excellent Redundancy with SSD

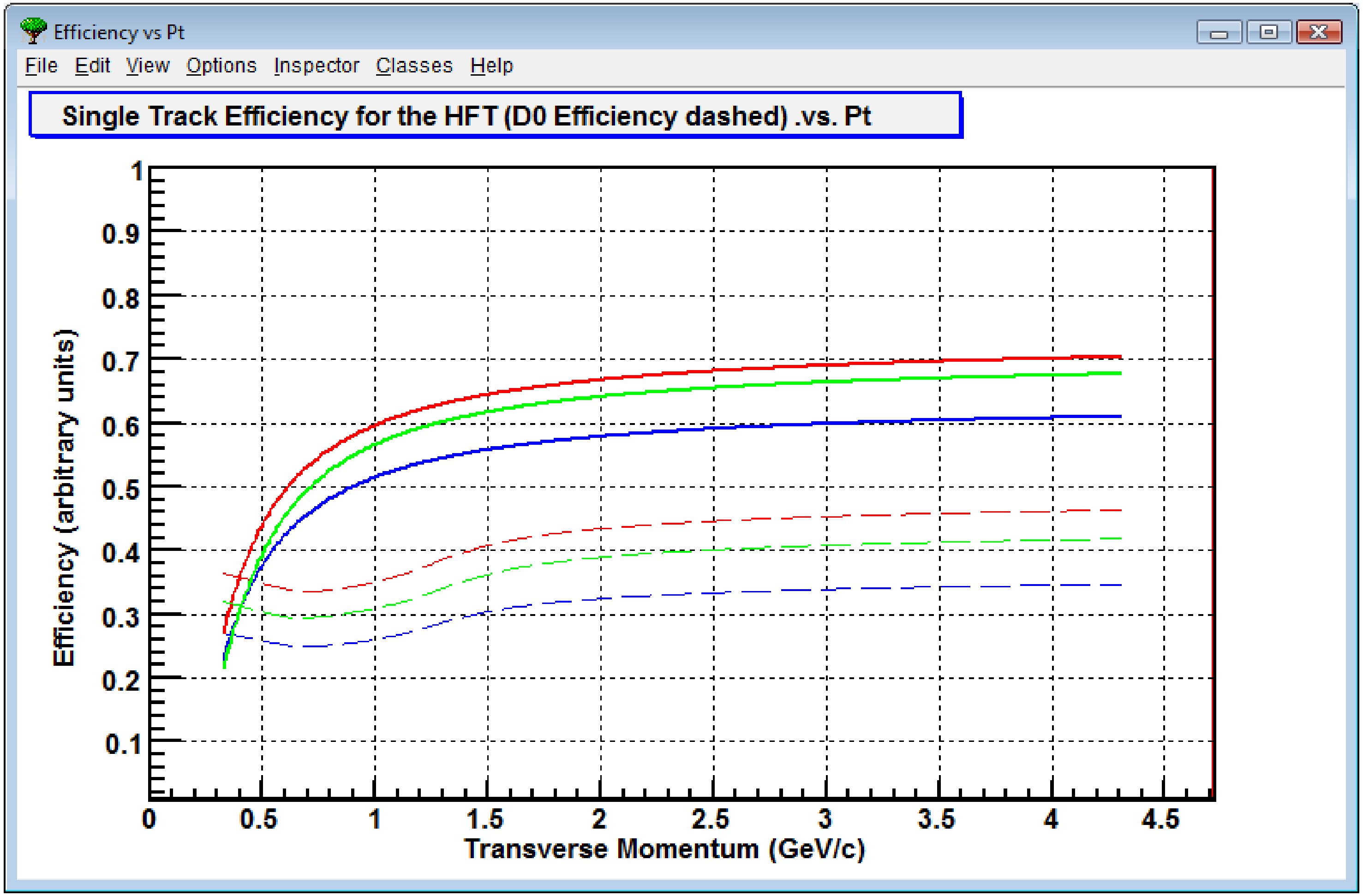
SSD Technology – an existing detector in STAR





- **Technology**
  - **30 μm x 750 μm resolution**
  - **Thin – 1% radiation length**
  - **Crossed strips with charge sharing … no ambiguous hits**
- **DAQ rate currently limited to 200 Hz**
- **Upgrade is possible ala ALICE Si Strip Detector**

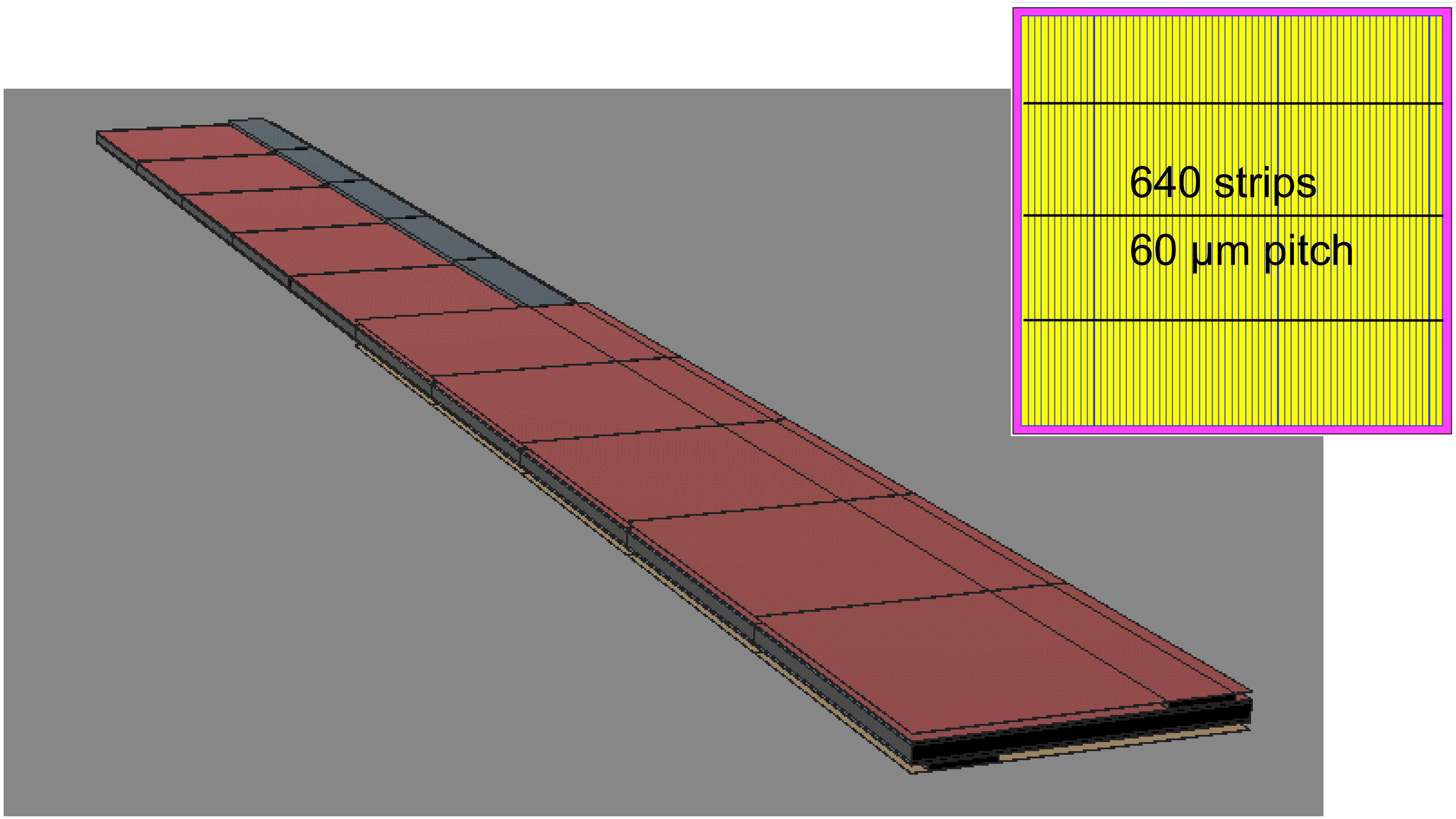
SSD technology at 12 cm radius (200 μsec HFT)



- vtx+pxl1+pxl2+ssd'+ist2+ssd+tpc (blue)
- vtx+pxl1+pxl2+ssd'+ssd+tpc (red)
- vtx+pxl1+pxl2+ssd'+tpc (green)

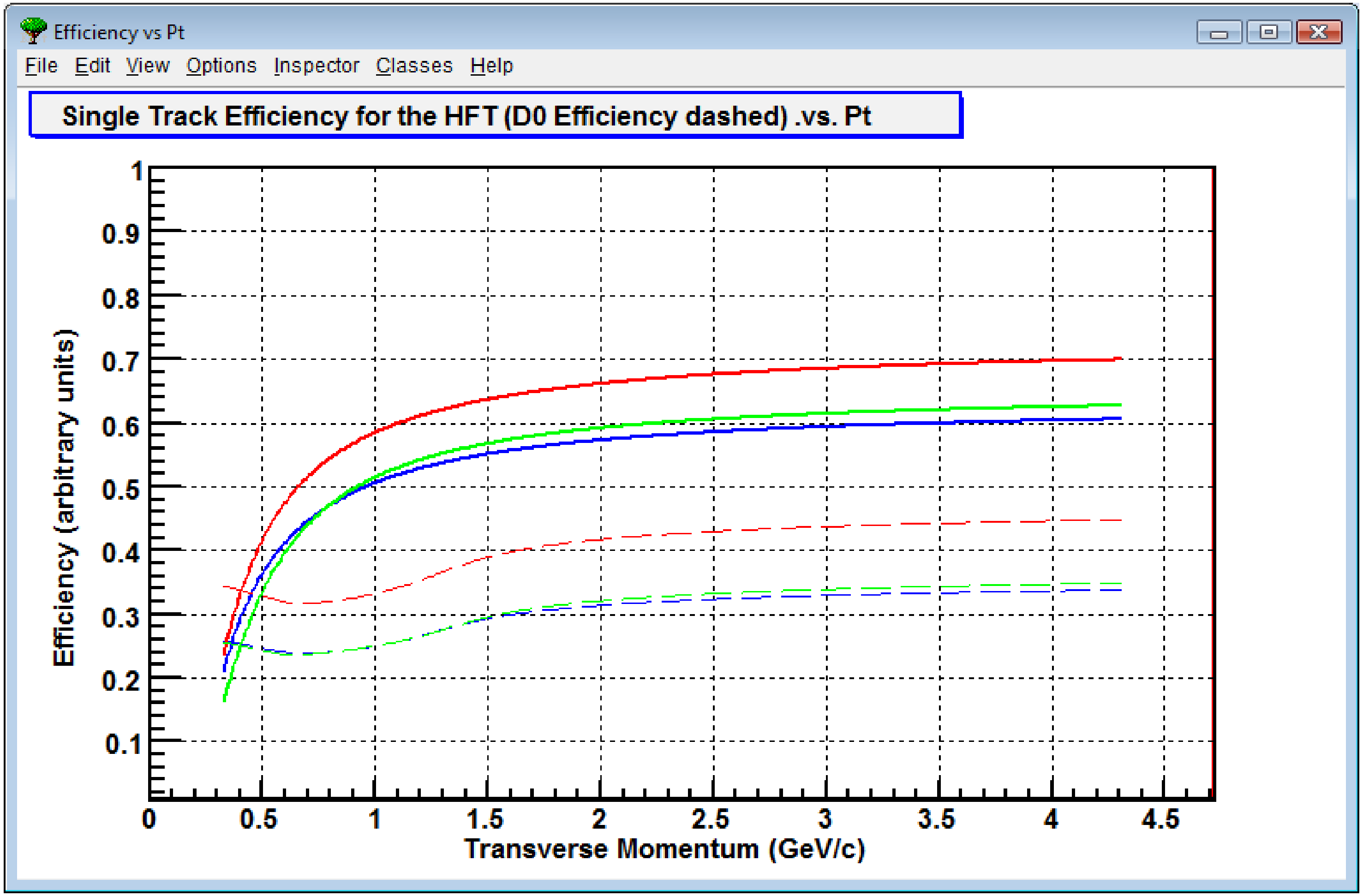
Very Good Redundancy with SSD

PHOBOS Based Technology – extensive use in PHOBOS



- **Technology**
  - **Strip Dimensions : 60 µm x 1 cm**
  - **Thin – 0.75% radiation length per layer, only one required**
  - **Orient for best resolution in R-ϕ direction. No crossed strips.**

PHOBOS technology at 12 cm radius (200 μsec HFT)



- vtx+pxl1+pxl2+phb+ist2+ssd+tpc (blue)
- vtx+pxl1+pxl2+phb+ssd+tpc (red)
- vtx+pxl1+pxl2+phb+tpc (green)

Pretty Good Redundancy with SSD

Comments and Conclusions

- Several technologies are very appealing and are well motivated
- Conventional Strips 60 μm x 1 cm look pretty good
- ¼ length strips are good.   Best binary divisor of 4 cm.
  - ½ length strips are not so good
- Radial location can still be optimized between 12 and 17 cm
- Only one layer required
  - Drop IST2-Z … it never was an efficient layer and never will be
  - Drop IST2-Rϕ … it can't compete with the SSD
  - Replace old IST1 with one layer of 1 cm long strips at an optimized R
    - Orient to give good resolution in the Rϕ direction
- Rumors of heat load problems … can they be overcome?
  - A challenge for the experts

A good combination

Backup Slides

Efficiency Calculations in a high hit density environment

The probability of associating the right hit with the right track on the first pass through the reconstruction code is:

P(good association) $= 1 / (1+S)$

where $S = 2\pi \, \sigma_x \, \sigma_y \, \rho$

P(bad association) $= (1 - \text{Efficiency}) = S / (1 + S)$

and when S is small

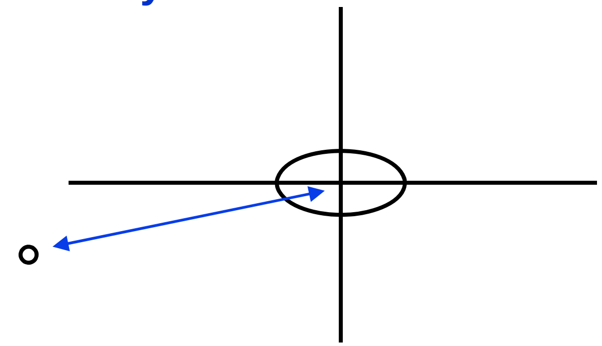
P(bad association) $\approx 2\pi \, \sigma_x \, \sigma_y \, \rho$

σ_x is the convolution of the detector resolution and the projected track error in the 'x' direction, and ρ is the density of hits.

The largest errors dominates the sum

$$\sigma_x = \sqrt{(\sigma^2_{xp} + \sigma^2_{xd})}$$

$$\sigma_y = \sqrt{(\sigma^2_{yp} + \sigma^2_{yd})}$$



Asymmetric pointing resolutions can be very inefficient

TPC Pointing at the PXL Detector

- **The TPC pointing resolution on the outer surface of the PXL Detector is greater than 1 mm …** **but lets calculate what the TPC can do alone**
  - **Assume the new radial location at 8.0 cm for PXL-2, with 9 μm detector resolution in each pixel layer and a 200 μsec detector**

Radius	**PointResOn (R-ϕ)**	**PointResOn (Z)**	**Hit Density**
8.0 cm	1.4 mm	1.5 mm	6.0
2.5 cm	90 μm	110 μm	61.5

  - **Notice that the pointing resolution on PXL-1 is very good even though the TPC pointing resolution on PXL-2 is not so good**

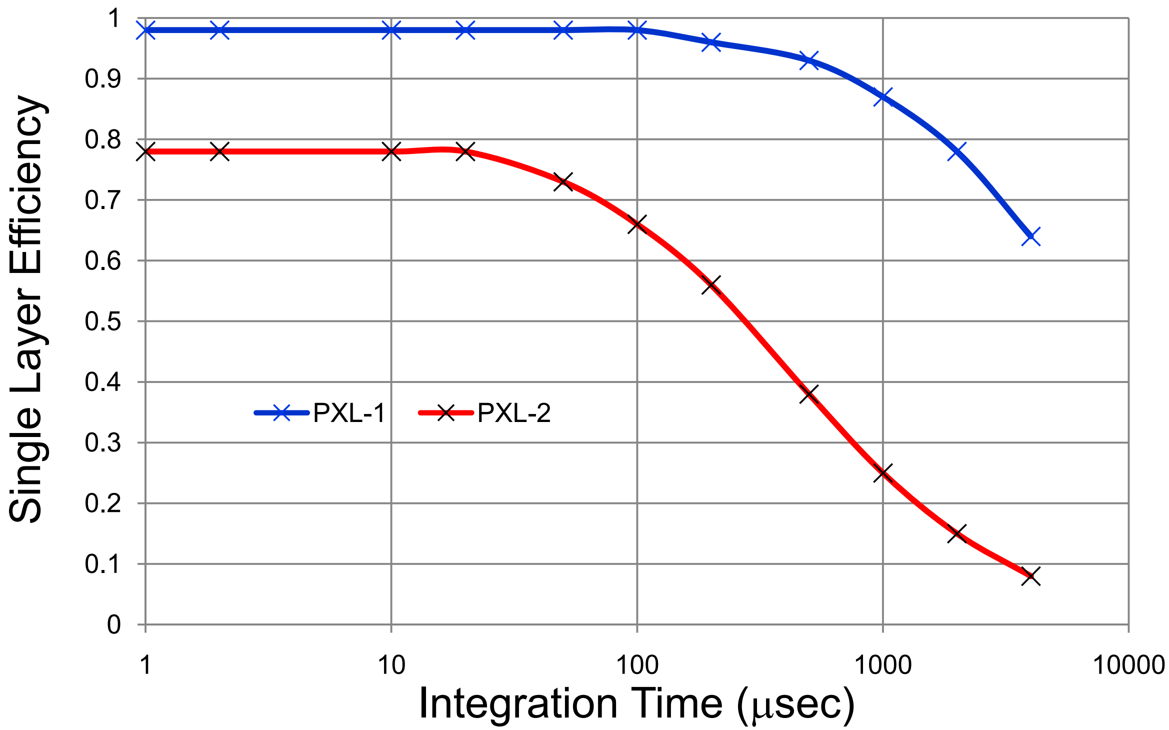
- **The probability of a good hit association on the first pass**
  - **56% on PXL2** The purpose of the intermediate tracking layers is to make 56% go up to ~100%
  - **96% on PXL1** All values quoted for mid-rapidity Kaons at 750 MeV/c

This is a surprise: The hard work gets done at 8 cm!

The performance of the TPC acting alone

- **The performance of the TPC acting alone depends on the integration time of the PXL chip**

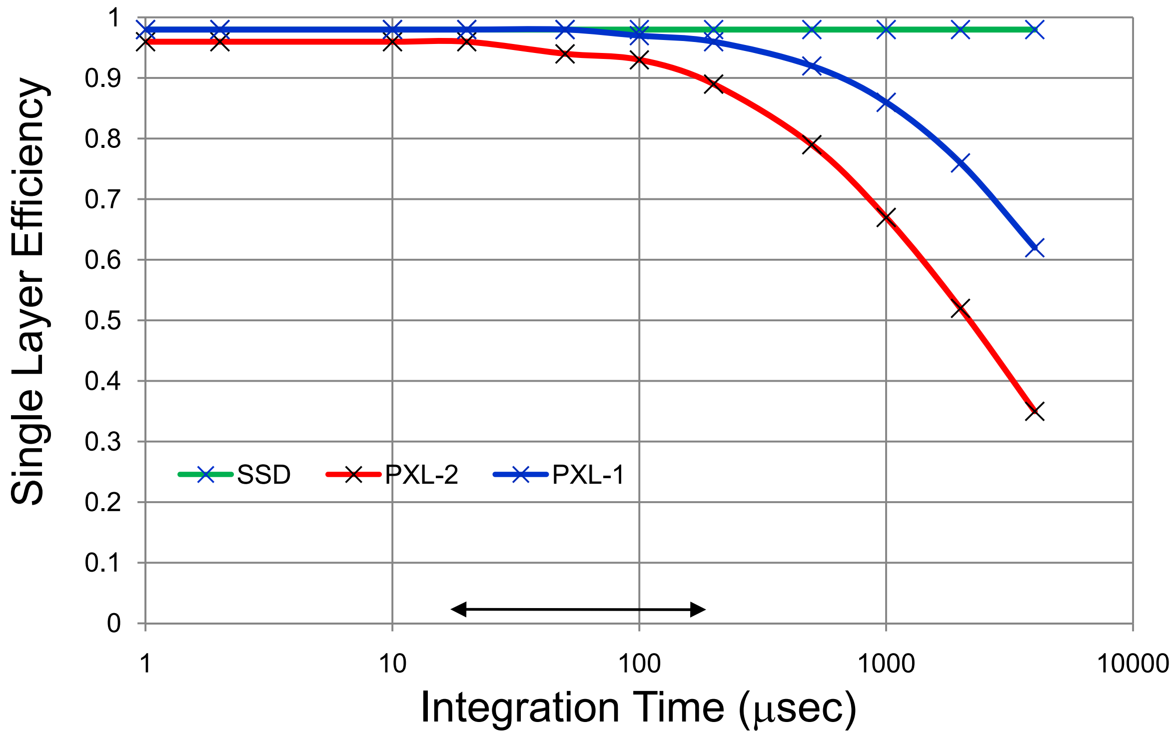
P(good association) = 1 / (1+S) **where S = $2\pi\, \sigma_x\, \sigma_y\, \rho$**



The performance of the TPC + SSD

- **The performance of the TPC + SSD acting together depends on the integration time of the PXL chip … and its very good**

P(good association) = 1 / (1+S) **where S = $2\pi \sigma_x \sigma_y \rho$**



The purpose of additional intermediate tracking layers is to make 94% go up to ~100%