CD0 Proposal Presentation
Intermediate Silicon Tracker (IST)

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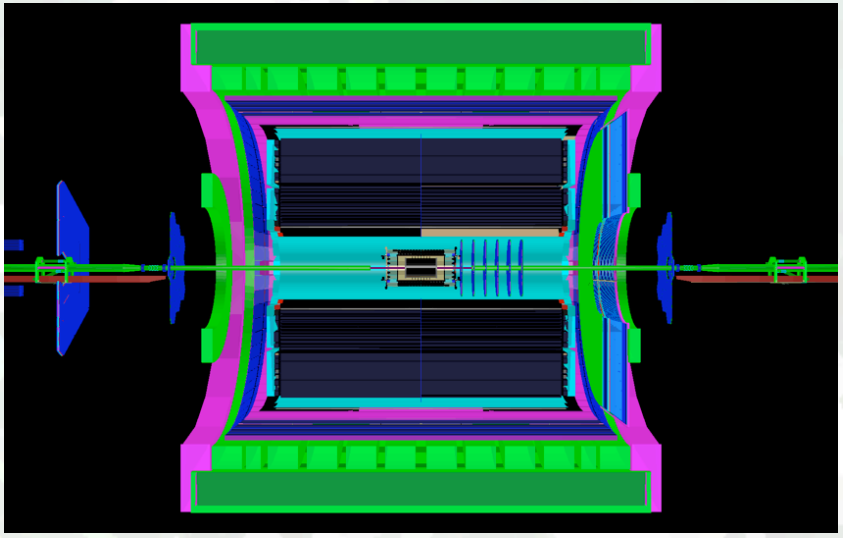
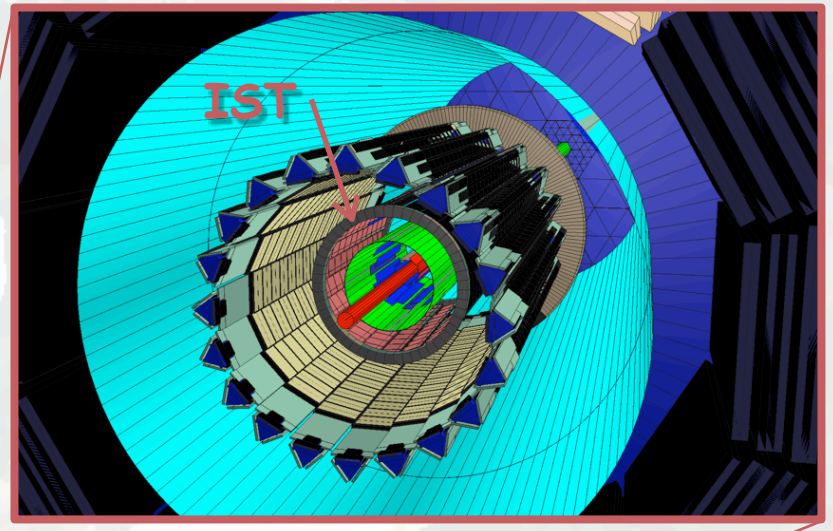
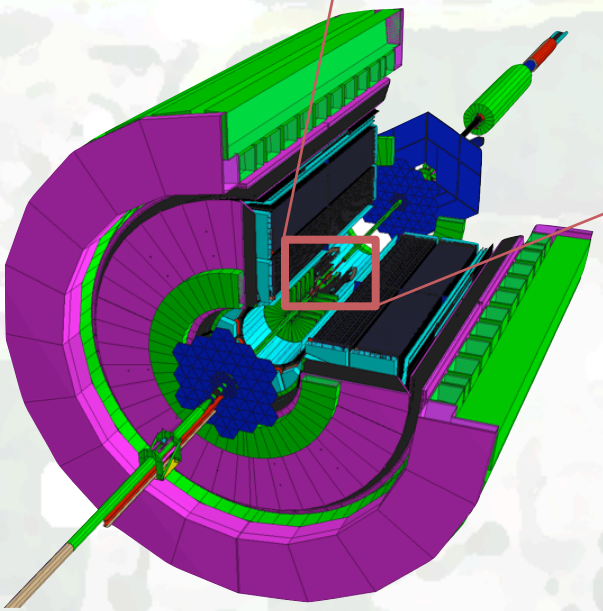


Outline

- Requirements
- Layout
- Technical realization
  - Ladder design
  - Silicon pad sensors
  - Readout system
- R&D plans
- Summary





Requirements

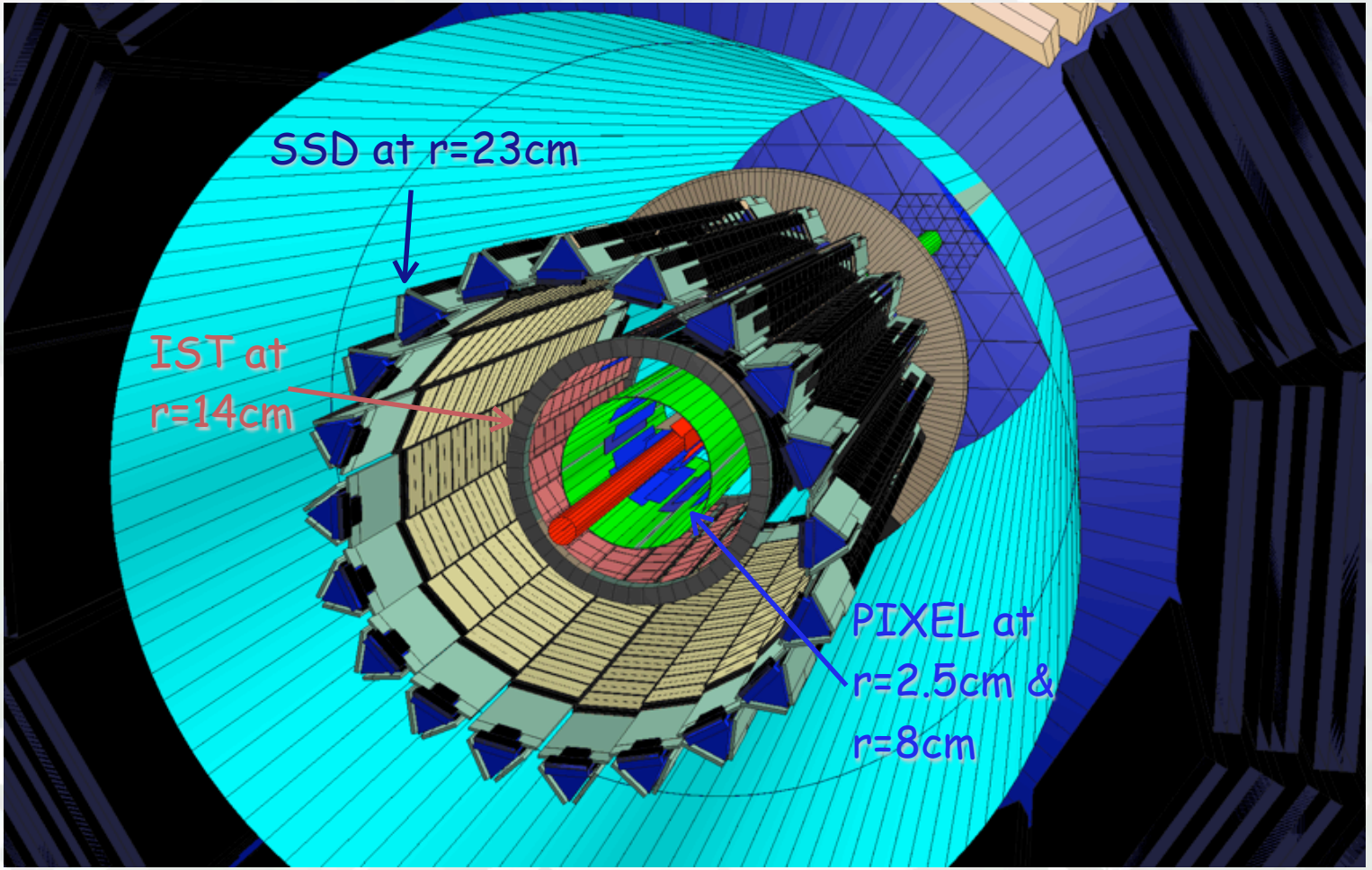
- Location: Between PIXEL and SSD covering -1 < η < +1
- Material budget: <1.5% X_0 per layer (-1 < η < 1) and <10% X_0 (1 < η < 2)
- Occupancy: <10% for central Au+Au events at 200GeV CME
- Tracking efficiency / purity: Meet physics requirements for efficient D^0 reconstruction

  $(D^0 \rightarrow K + \pi)$
- Rate capability: Handle RHICII peak luminosities for Au+Au and p+p
- Sampling speed: Resolve individual beam bunches (107ns - bunch crossing time)

Layout

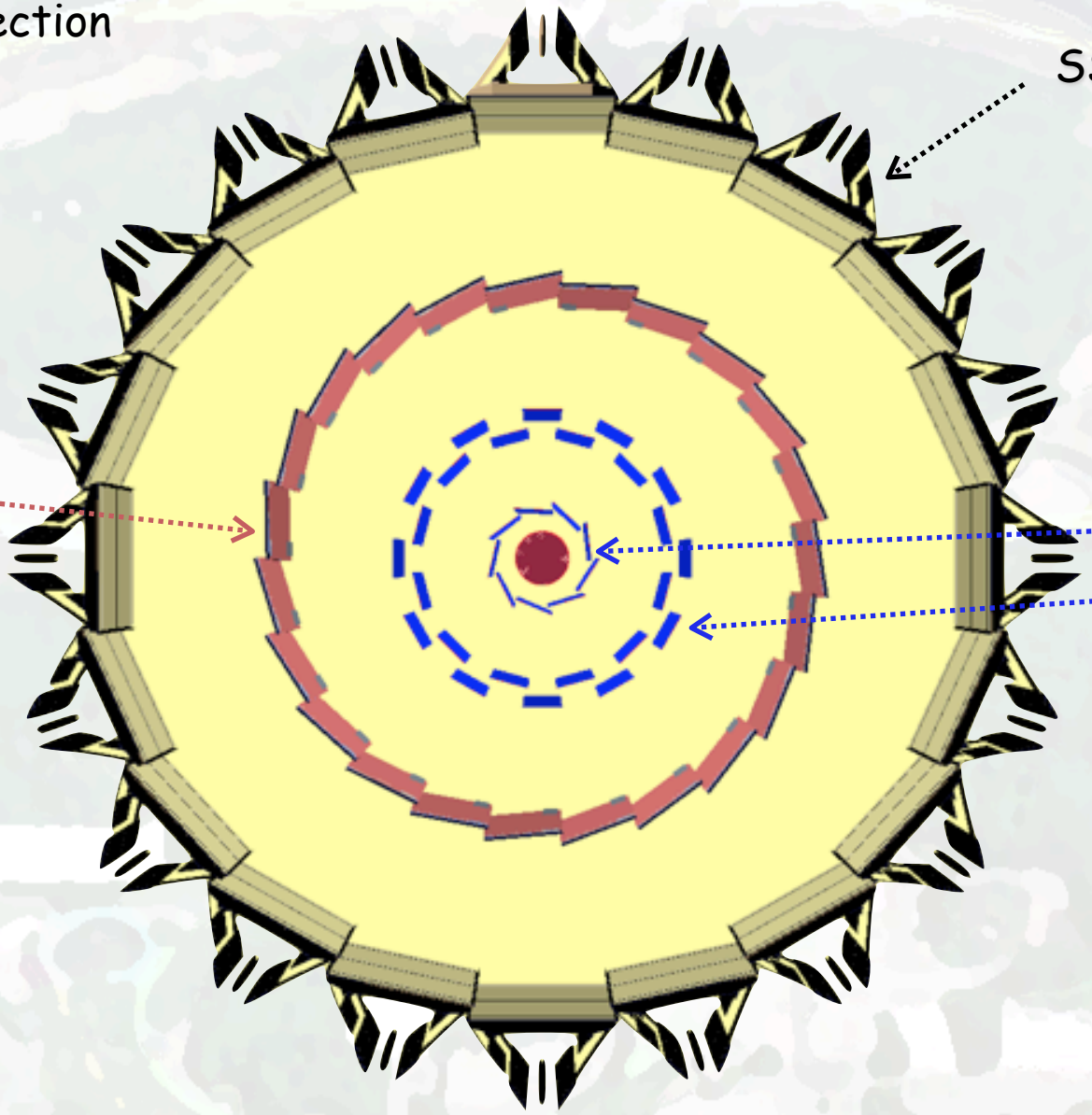
Overview - HFT

- Features of 1 layer IST layout:
  - Fast tracking with 2 layer IST is limited
  - Focus on IST as pointing device
  - Good efficiency with and without SSD
  - Lower dead material budget and heat dissipation
  - Reduced cost and time for construction



Layout

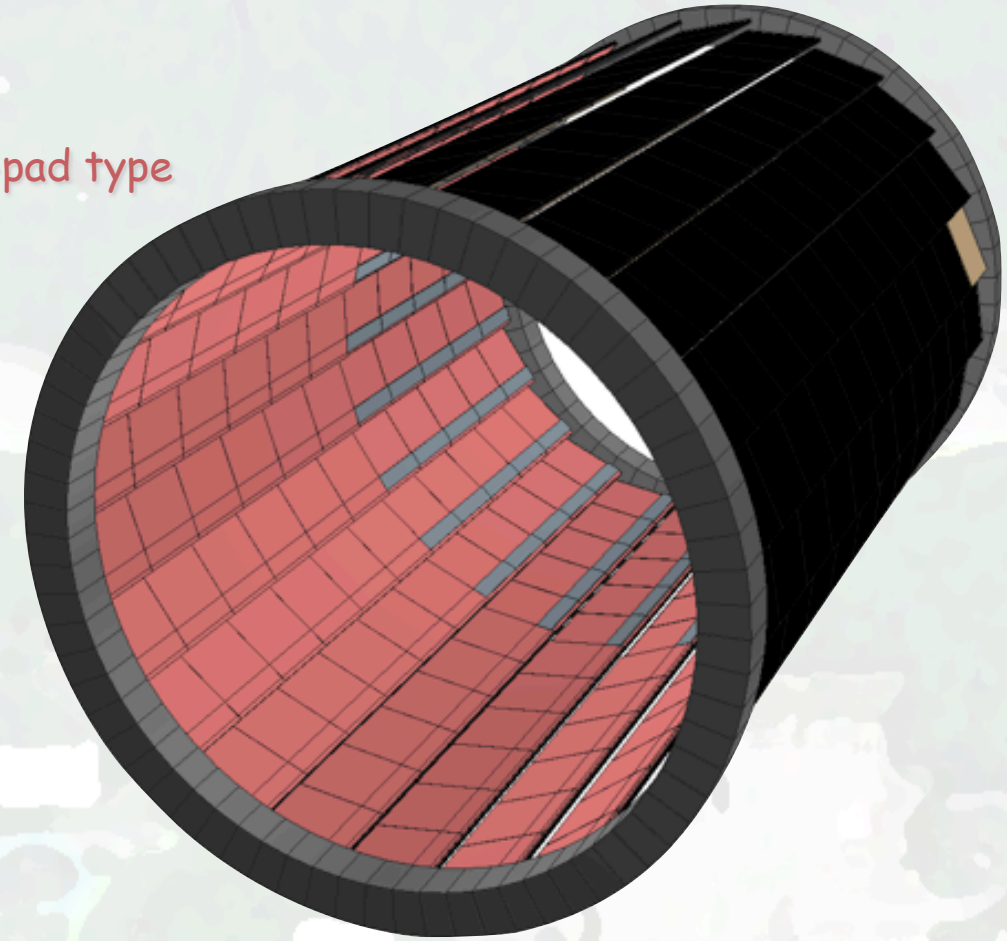
- IST - Cross-section



Layout

- IST - 3D view

IST
1 sensor layer: Silicon-pad type



Layout:

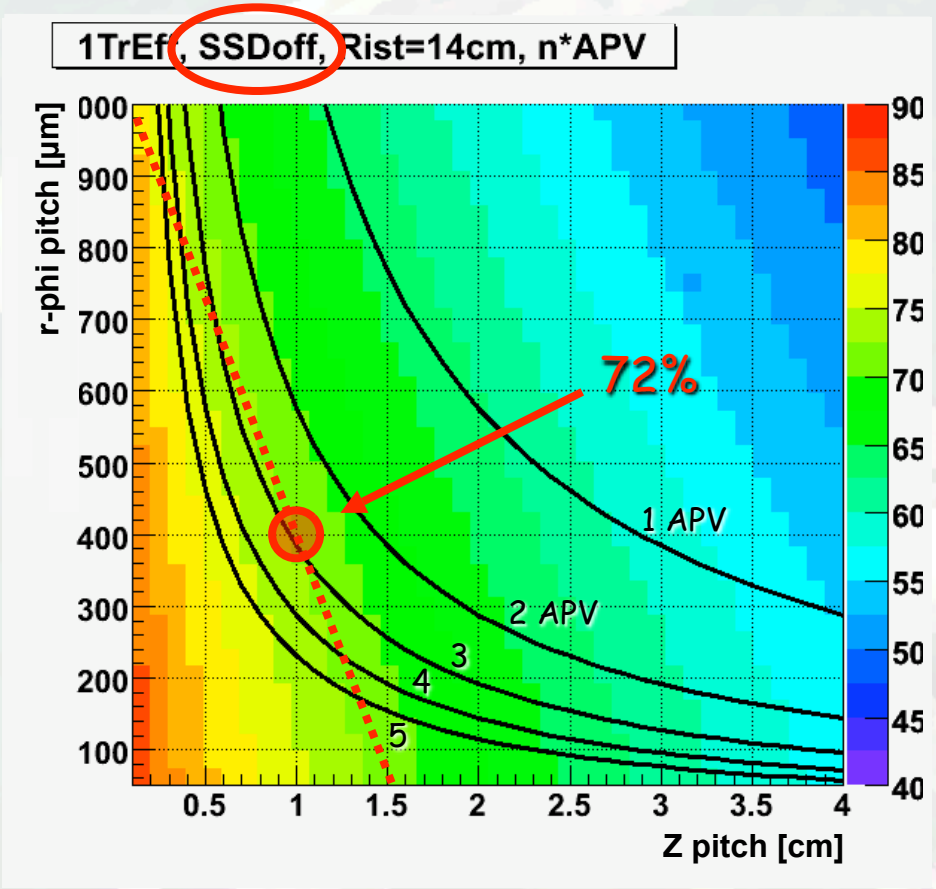
- r = 14 cm
- 23 ladders
- 11 units (Modules) per ladder (44cm)

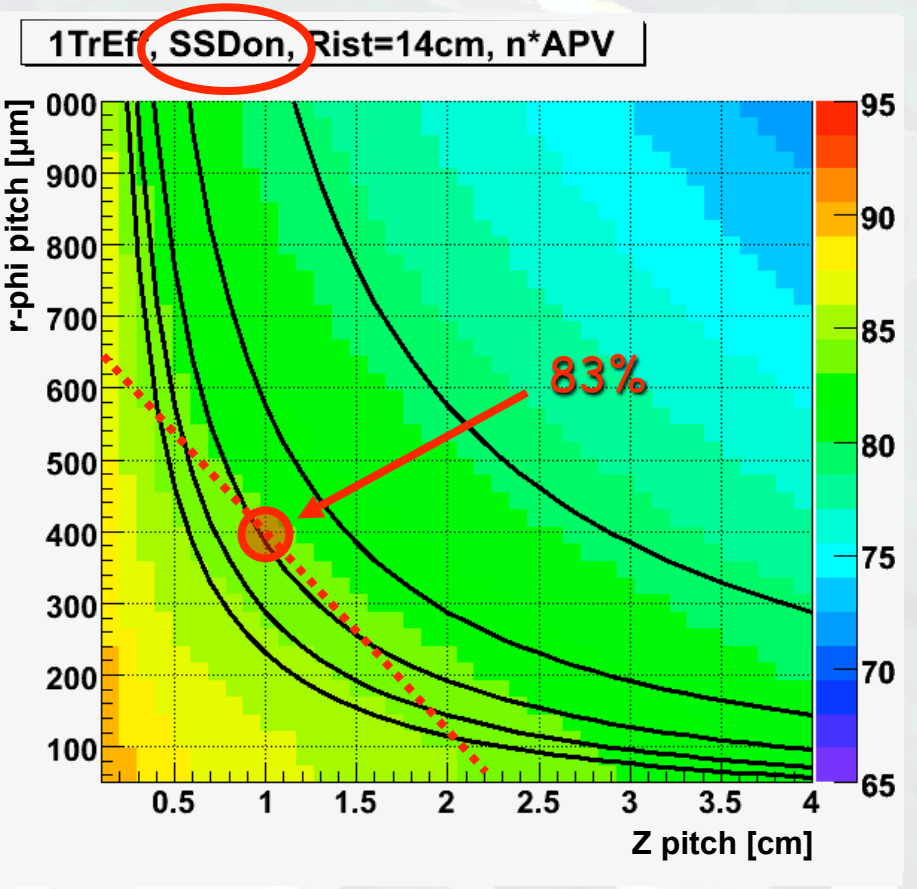
IST Simulations:

- Realistic ladders, support and cables
- No utilities yet

Layout

- Optimization of IST layout



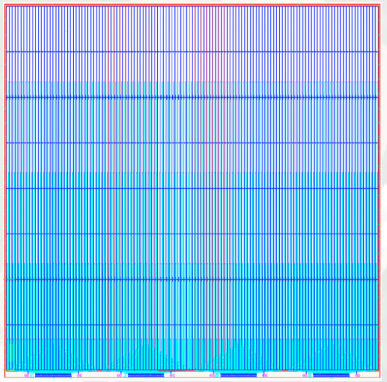


- 3 APV chips per sensor (384 channels) yields excellent efficiency with (without) SSD of 83% (72%)
- In comparison: 54% (85%) for TPC (TPC+SSD)
- Efficiency relatively insensitive to changes in number of readout chips and layout of silicon pad sensors

Technical realization

- IST - Ladder design - Overview

Location: Silicon-pad sensor



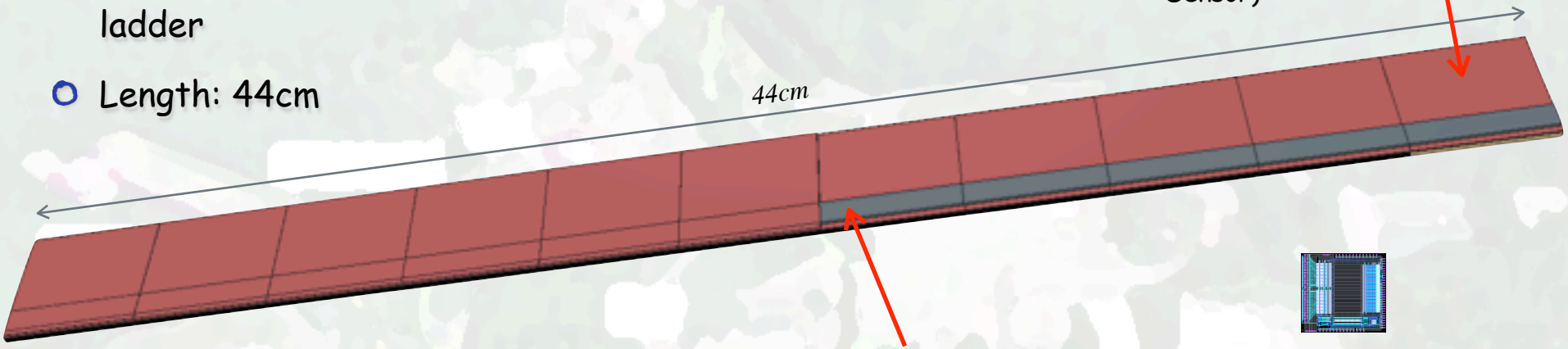
(Example: PHOBOS Inner Vertex Sensor)

Module:

- Silicon-pad sensors: Dimensions: 4cm X 4cm
- Light-weight Hybrid (e.g. Kapton based)
- Readout Chip: APV25-S1

Ladder:

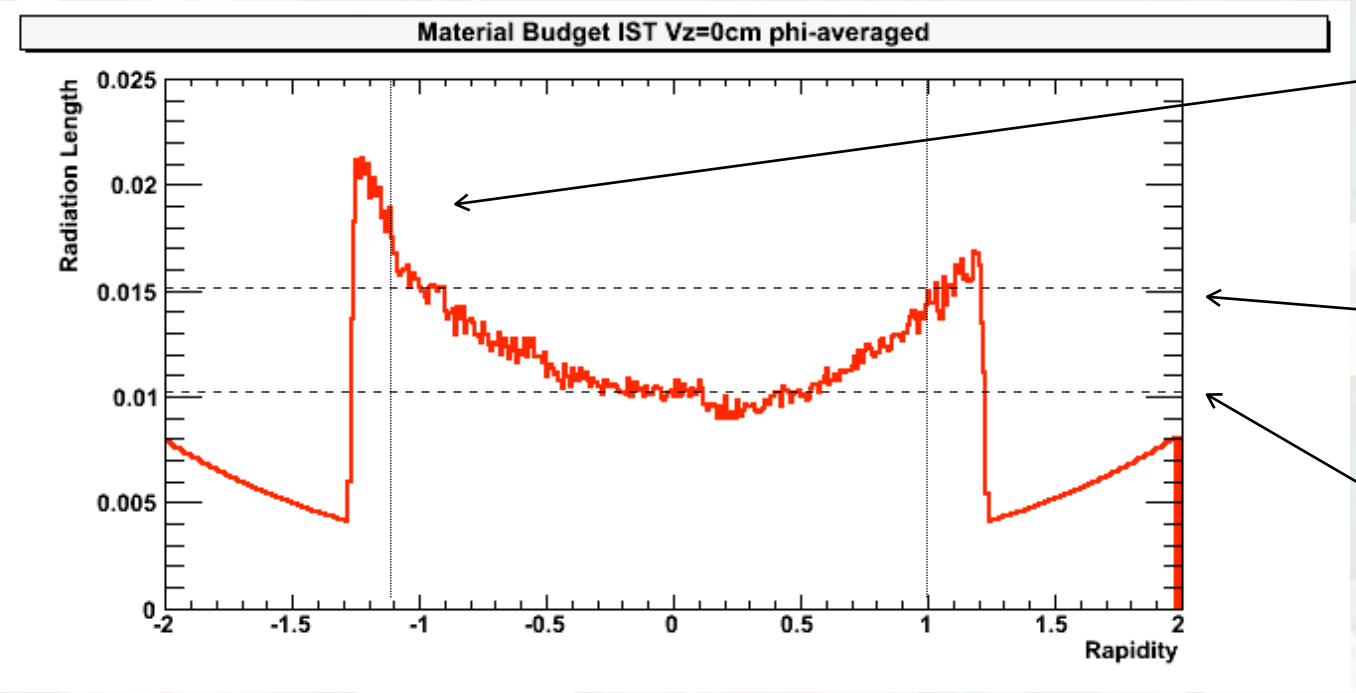
- Carbon fiber base material
- 11 modules per ladder
- Length: 44cm



Location: APV25-S1 Readout Chips

Technical realization

- IST - Dead material distribution



Asymmetry due to cable runs (η < 1)

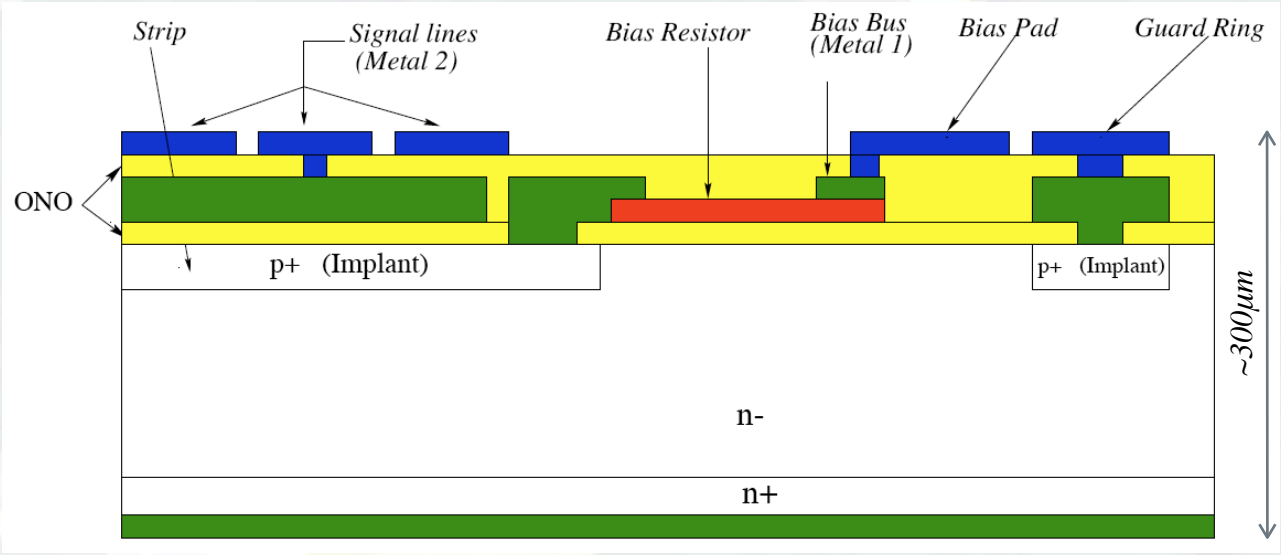
<1.5% X_0 per layer (-1 < η < 1)

Minimum: ~1% X_0 per layer on average

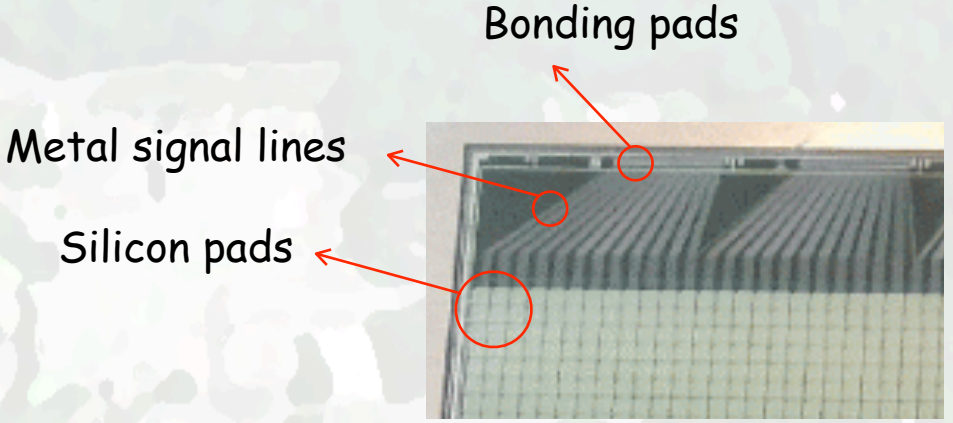
Technical realization

- IST - Technology choice: Silicon pad sensors

- Conservative approach to minimize risk
- Build upon existing expertise
- Silicon pad-sensors from commercial vendor (Hamamatsu)
  - Proven to be a reliable technology with numerous applications
  - MIT-LNS silicon lab (Successful PHOBOS silicon system)



(Cross-section: Double-metal silicon pad sensor, AC coupled)

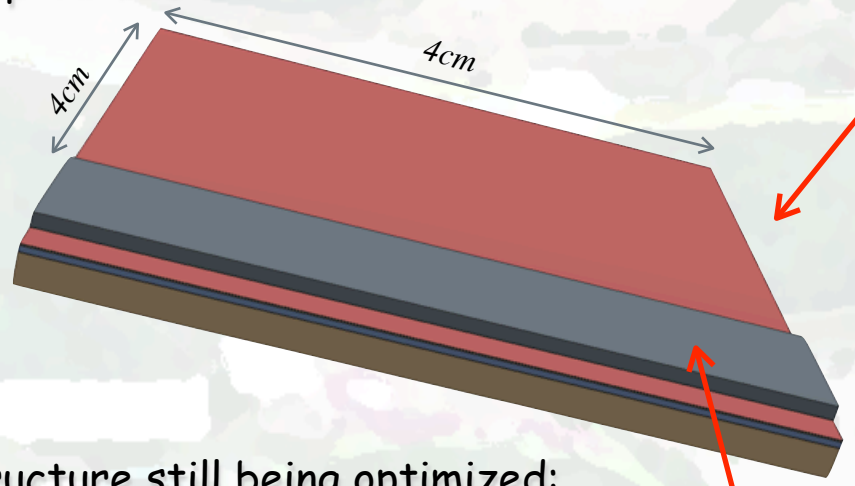


Technical realization

- IST - Silicon module

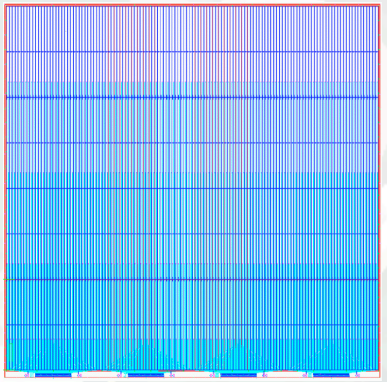
Module:

- Silicon-pad sensors (Double-metal layer, AC coupled): Dimensions: 4cm X 4cm
- Light-weight Hybrid (e.g. Kapton based)
- Readout Chip: APV25-S1

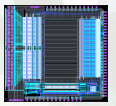


- Pad size structure still being optimized: 400μm X 1cm with 3 APV-S1 chips good compromise!

Location: Silicon-pad sensor



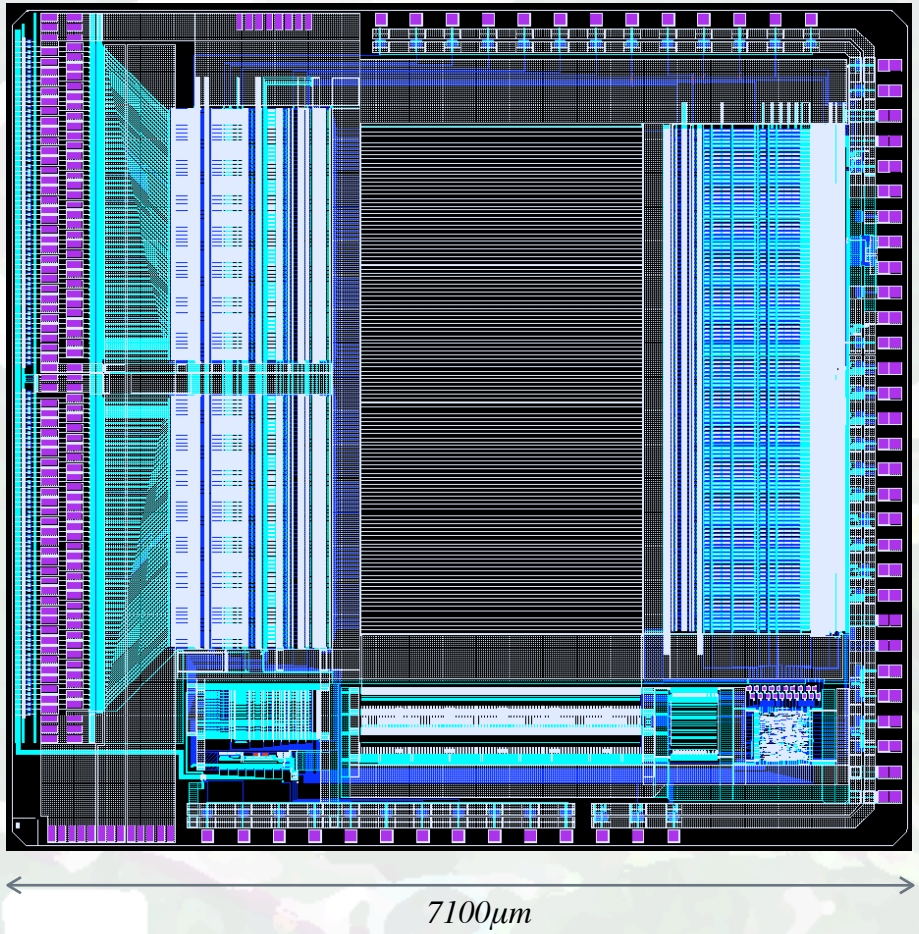
(Example: PHOBOS Inner Vertex Sensor)



Location: APV25-S1 Readout Chips

Technical realization

IST - Readout chip: APV25-S1 (1)

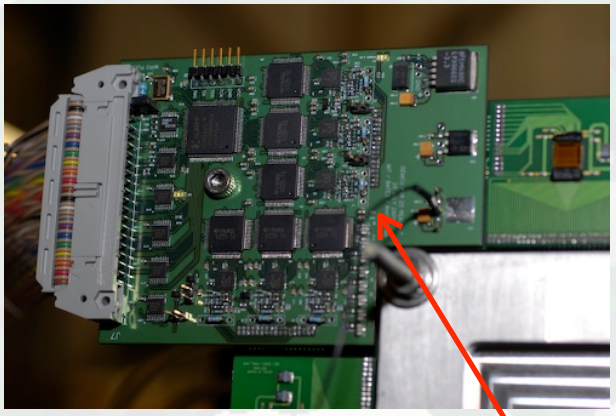


- Off-the shelf readout chip: APV25-S1
- Used for STAR IST and FGT (1 readout system)!

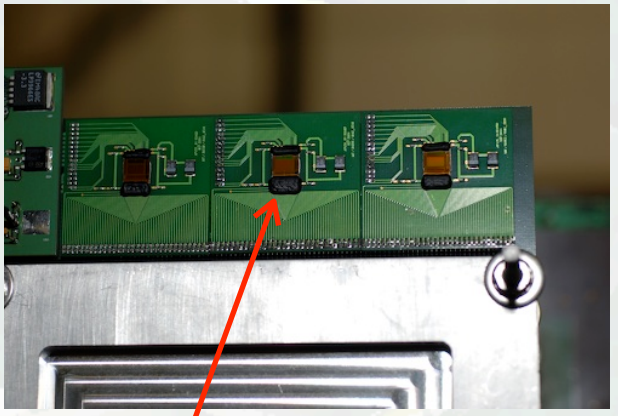
- Developed for CMS (75000 in CMS tracker) and also used by COMPASS for triple-GEM detector readout
- 0.25μm CMOS
- 128 channels
- 40 MHz sampling rate
- 4μs analogue pipeline
- 11:1 Signal / Noise
- 0.25Watt/chip
- Radiation hard

Technical realization

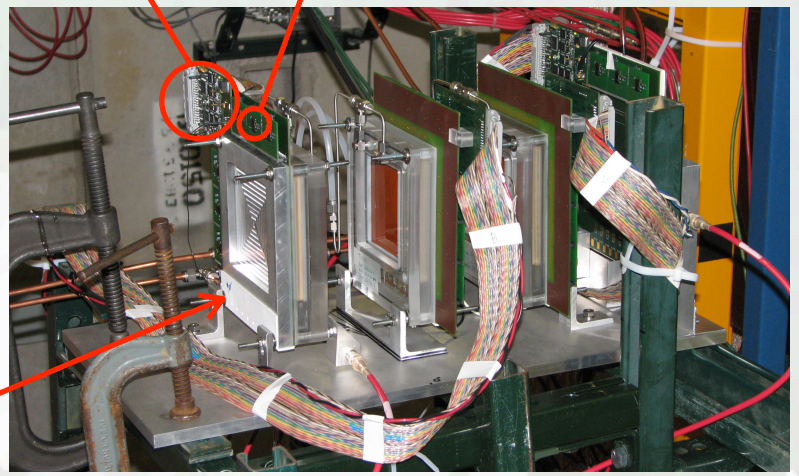
- IST - Readout chip: APV25-S1 (2)
  - Full Front-End and DAQ prototype system developed for APV25-S1 system for STAR Forward GEM Tracker (FGT) prototype
  - Successful bench test and FNAL testbeam experiment of FGT prototype detectors incl. chip readout



FPGA based Control Unit



APV25-S1 Hybrid



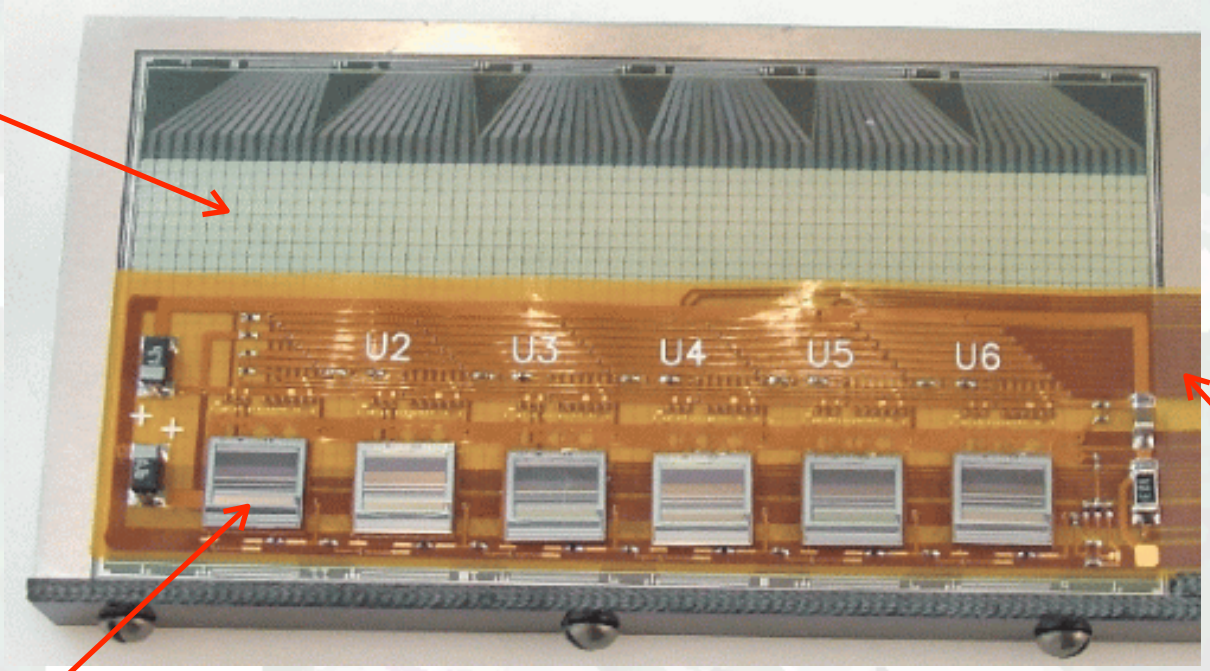
FNAL testbeam setup of Triple-GEM prototype detectors

hep/physics.ins-det/0711.3751

Technical realization

- IST - Prototype module

Silicon pad sensor (Available PHOBOS Type I test sensor)



Kapton Cable/ Hybrid

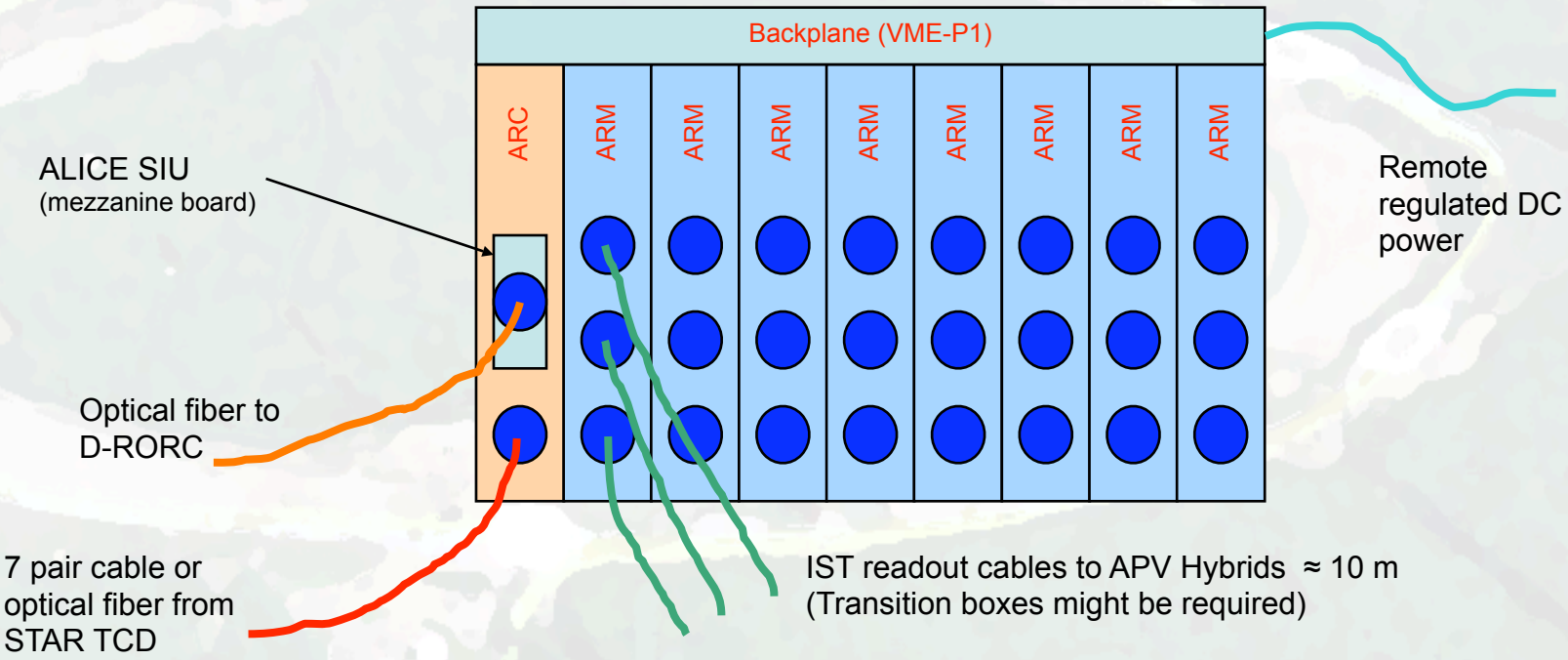
APV25-S1 readout chip

Functionality test (e.g. Bonding/ Heat transfer) underway!

Technical realization

IST - Data Acquisition System

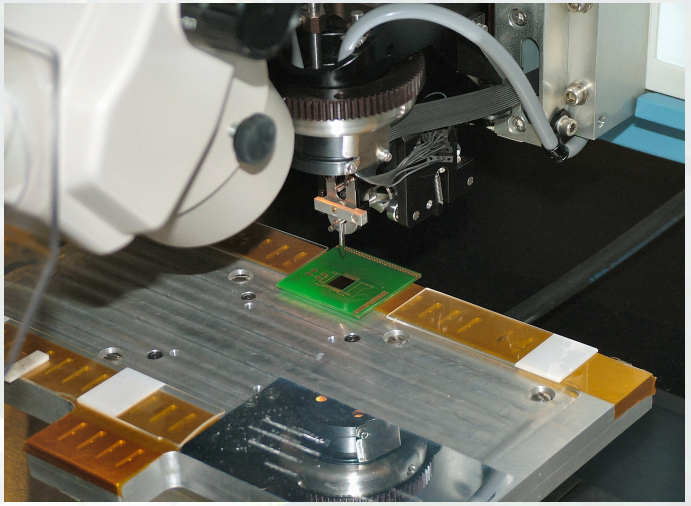
- Conceptual design of STAR specific DAQ system for APV25-S1 readout of FGT developed



- Focus on similar design for STAR DAQ system for IST
  - ARM (APV Readout Module): 18 ADC channels and data processing FPGA's (Zero suppression, Pileup rejection, Common mode noise correction)
  - ARC (APV Readout Controller): Control FPGA's, STAR clock/trigger interface and ALICE SIU (data/control link)
  - 6 Crates sufficient to read out 110,000 IST channels (current design) based on STAR Forward GEM Tracker (FGT) DAQ design!

Technical realization

- Existing infrastructure at MIT
  - Fully equipped silicon laboratory (Former PHOBOS production facility) at MIT-LNS:
    - Clean room
    - Silicon sensor probe station
    - Bonding machine
  - Research and Engineering (R&E) Center at MIT-Bates



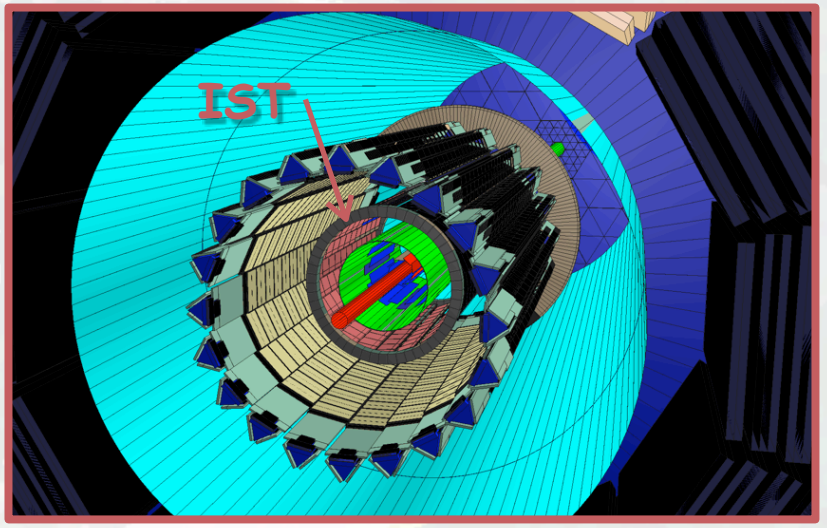
- Experienced technical personnel at MIT
  - MIT-LNS Silicon laboratory: Sensors testing, module & ladder assembly, bonding and test (1 Technician)
  - MIT-Bates R&E center: Readout design (1 Electrical engineer) and mechanical design (1 Mechanical engineer)

R&D plans

- Required R&D activities in 2008
  - Goal: Develop a fully functional IST ladder with necessary readout electronics and cooling
    - Develop ladder structure based on carbon fiber material (Produce 2 full ladder cores for tests)
    - Purchase 11 prototype silicon pad sensors to equip one full ladder
    - Purchase 100 APV25-S1 readout chips
    - Design and test of Kapton based cable/hybrid prototype including two readout control units
    - Develop assembly and manufacturing procedures based on PHOBOS experience

Summary

- IST - 1 layer silicon pad detector
  - Performance:
    - Efficient tracking and D^0 reconstruction ($D^0 \rightarrow K+\pi$)
    - Dead material <1.5% for $-1 < \eta < 1$
    - Internally fast detector and readout system
  - Technology choice: Silicon pad sensors
    - Conservative approach to minimize risk
    - Build upon existing expertise



- Readout system: Off-the shelf readout chip APV25-S1 - Profit from parallel STAR Forward GEM Tracker (FGT) readout design effort and tests
- Existing infrastructure and experience: MIT-LNS silicon laboratory and expertise / MIT-Bates R&E center (Readout and mechanical design work)
- R&D goal 2008: Develop a fully functional IST ladder