LG 03/07/2007

HFT Ultimate Detector Requirements and Readout

Representatives of the LBNL RNC group met with Marc Winter's IHPC group in Strasbourg in late January of 2006 to discuss the detector development and plan for the future direction of sensors to be used in the final HFT detectors. (Marc Winter's summary can be found at http://www.lbnl.leog.org/StrasbourgTrip_summary.pdf). At that meeting it was agreed that there would be two coupled development programs. The first program would lead to an analog readout chip, MIMOSTAR4, which would be used to build a prototype detector with a 4 ms readout time. The second program would build on the MIMOSTAR4 and culminate in the "ULTIMATE" chip, which was proposed to be a 200 µs integration time, triggered, on-chip CDS, digital threshold device with digital LVDS outputs. While several possible configurations were discussed, no final set of parameters were agreed to. I hope to restart the discussion by proposing the following as a set of "ULTIMATE" chip parameters and also proposing a possible readout and data reduction architecture. The parameters discussed should be validated by initial testing and simulations arising from the HFT telescope test.

Ultimate Sensor Parameters as discussed in Strasbourg.

Physical

- 640 x 640 pixels with 30um pitch.
- Minimum of 3 fiducial marks / chip for optical survey purposes.
- All bonding pads located along 1 side of chip
- Two bonding pads per I/O of the chip to facilitate probe testing before sensor mounting.

Electronic

- Continuous cycling 100-200 µs integration time.
- Trigger input reads out the previous 200 µs integration window.
- On chip CDS for the pixels.
- On chip JTAG programmable discriminator thresholds, biases, etc.
- 4 LVDS readout channels / chip with a full readout time of less than 1 ms.
- JTAG programmable testing modes.
- Appropriate flags for readout synchronization, e.g. MXfirst.
- Synch input to start chip function.
- Signal / Noise > 9 at operating temperature of 30 degrees C.
- Maximum average power dissipation of 100 mW / cm2.

Triggering and it's Implications for Efficiency.

The STAR trigger delivered to the HFT has the following associated characteristics and latency[1]:

- From the time of the interaction to the Trigger Level 0 trigger decision (at backplane of TCD crate) is 1.65 µs
- Our expected latency in receiving, latching and distributing the trigger to the sensors is ~220 ns
- Thus the total latency from the particle interaction to the time a trigger is delivered to the sensors is ~1.87 µs
- Triggers are delivered randomly with a minimum period of 1 ms between accepted triggers.

Based on discussions with Michal and information in the MIMOSA8 articles, the most likely scenario for the present design of the ultimate sensor would involve clocking through parallel sub-arrays of pixels sized such that 200 µs gives a full pass through each sub-array. The CDS value of each pixel would be stored and the pixel reset once every 200 µs in each sub-array. When a trigger was received, the sensor would stop the cycling through pixels and enter a readout mode where the pixel CDS values would be read out and the amplifier biases removed by a second CDS performed at the column readout. The final pixel CDS value would then be presented to a dual threshold discriminator and the resulting two bit (high and low threshold) values would be serialized and readout via LVDS. We will have four LVDS readout ports per sensor and the total readout time is specified to be 1 millisecond giving a LVDS clock of 1 millisecond / [((640 * 640 pixels) / 4 readout lines) * 2 bits] = 4.9 ns period or 204 MHz.

One feature of this scheme is that the ultimate sensor will continue to reset pixels until it receives a trigger, which it will receive 1.87 µs after the particles transit the sensor. This corresponds to a randomly located loss of 1.87 µs / 200 µs = 0.94 % of pixel information. If we require a hit in each layer of the HFT to define a track, the number doubles to ~1.9 % for tracks. This may or may not be an issue. It should be added to our simulations to see what effect it has.

If this is a problem, a possible solution would be to add another capacitor to each pixel to store the previous pixel CDS value. This would effectively add a two refresh period memory to each pixel. The trigger latency is known and the decision as to which pixel level CDS value to read when the sensor enters the readout mode would be based on this known latency (hopefully a parameter that can be configured via JTAG).

In any case, the readout for either configuration would be the same.

Readout

The readout scheme derives closely from the existing readout scheme of the MIMOSTAR2-4 sensors[2]. A block diagram is presented below.

---

[1] http://www.star.bnl.gov/STAR/html/trg_l/TSL/Schematics/Trigger_L0_Timing_2003.pdf is the old documentation. Discussions with Eleanor Judd of the STAR trigger group have given the numbers shown.

[2] http://www.lbnl.leog.org/RDO_section_HFT_proposal.pdf

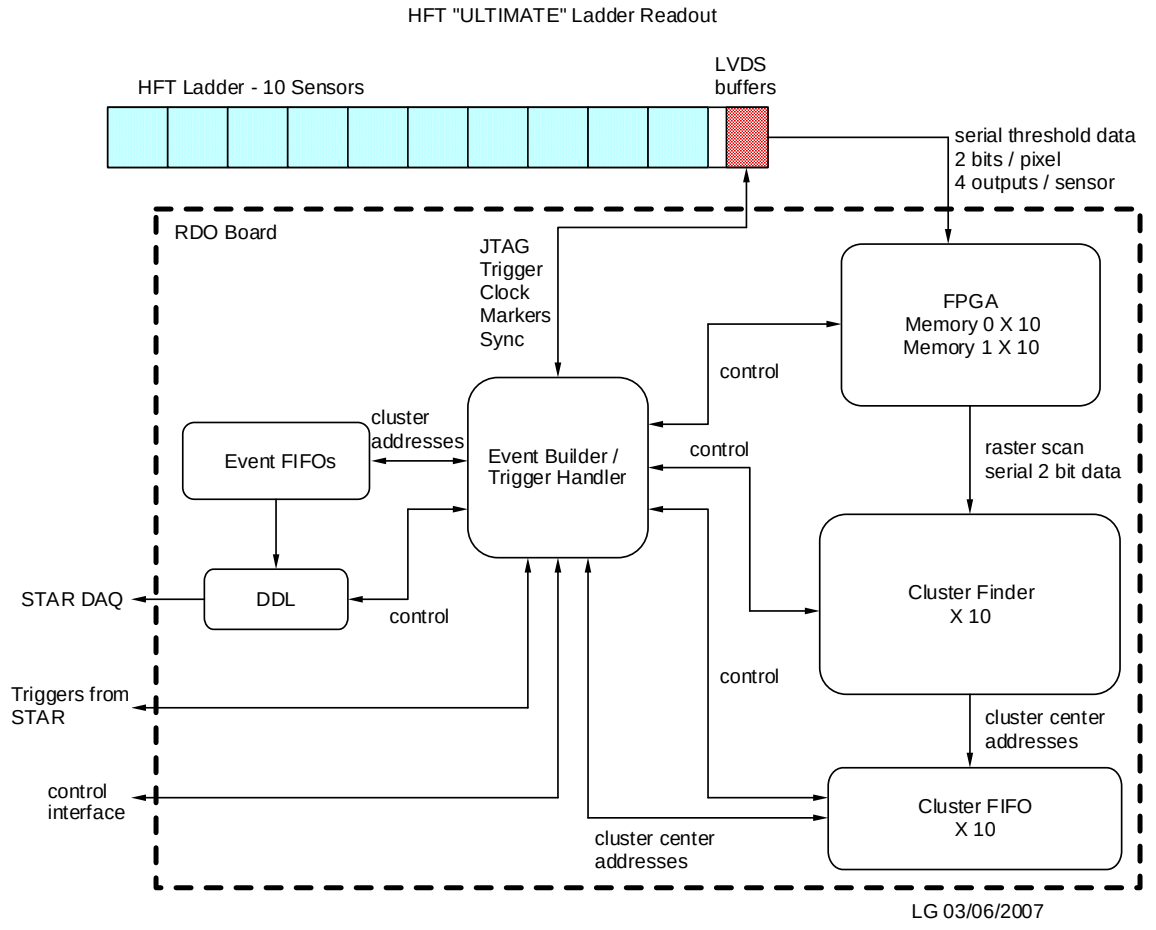

Figure 1 – Block diagram for the HFT Ultimate detector readout.

Data Flow

The full HFT readout system is a parallel system of 33 ladders, each with the same readout, thus the readout system for a single ladder is presented as the basic building block of the system. In this readout design, the sensors are as described above and are triggered. Triggers, clock, JTAG, Synchronization and markers are provided from the Readout board. After receiving a trigger, the sensors perform a high / low threshold compare to the CDS value for each pixel and send a serial stream of the logic values results of this threshold comparison through LVDS buffers located at the end of the ladder (out of the low mass region) to the Readout board via low mass twisted pair cable. On the Readout board the data is transferred into high speed memory located in an FPGA. This memory now contains the full contents of each pixel on the sensor represented by a 2 bit string with the hot pixel map implemented as a mask. The sensor threshold data is then run through a cluster finder with the same form as previously described in our readout system and the resulting center address is passed to a cluster FIFO. The contents of these cluster FIFOs are built into an event with header and event ID information and the resulting event is passed to DAQ via the DDL.

Timing and Implementation

The proposed time structure of the readout is shown in the diagram below.

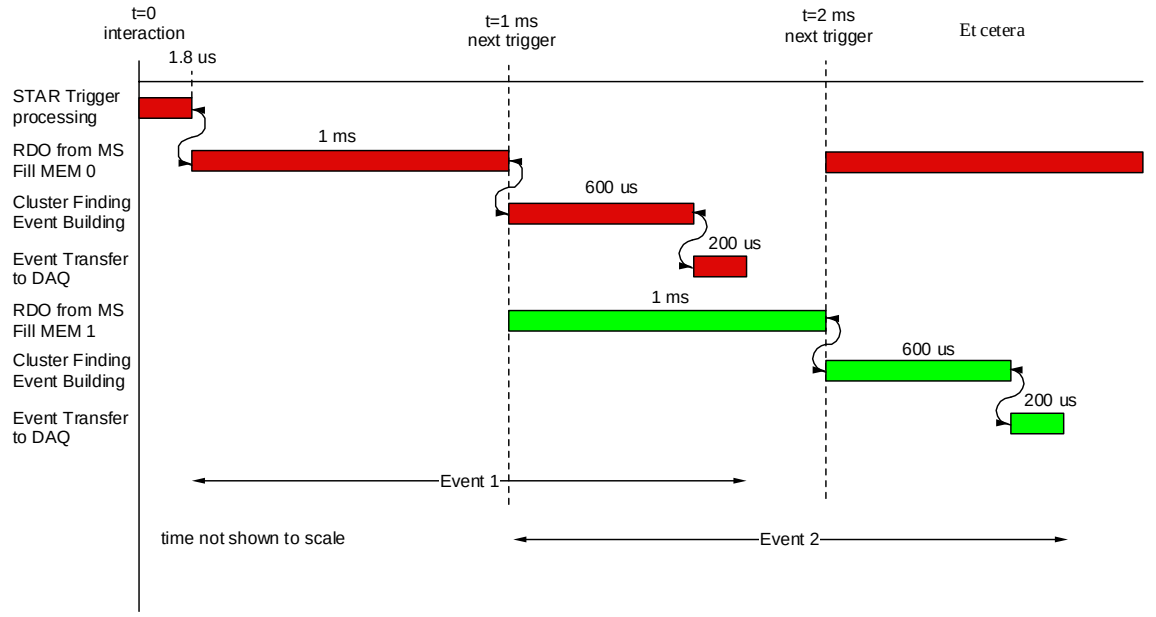

Figure 2 - Proposed time structure of the Mimostar Ultimate readout. To meet the 1 KHz trigger requirement, we require two memory buffers to allow for immediately retriggered readout of the sensor.

The requirement of servicing a 1 KHz trigger combined with the 1 ms readout time of the sensors drives us to implementing two full sensor readout buffers in a ping-pong configuration. Data resorting, if required, will be implemented in the memory controller to give a raster scan data image in the memory. The hot pixel map will also be implemented as a mask in the memory. Unlike the synchronous analog readout cluster finder, which operates on the readout clock (50 MHz), the cluster finding for the ultimate sensor can run at implementation speed in the FPGA which is significantly faster. The event building readout into the event buffer similarly will run at FPGA implementation speed. Data transfer through the DDL is fast and additional event FIFO buffers can be implemented if needed.

It is important to note that current FPGAs are fast and have significant memory block resources. The Xilinx Virtex-5 can be purchased in configurations that have 11.664 Mbit of block memory and 550MHz internal clock distribution[3]. We could implement the entire RDO system for one ladder on two Xilinx Virtex-5 FPGAs in the current technology. The projected time frame for producing this readout system is 3 years away, during which time we expect to see further improvements in FPGA technology.

[3] Please see http://direct.xilinx.com/bvdocs/publications/ds100.pdf