Ultimate / DAQ System Interface - Normal readout = Not test modes

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OUTLINE

- Ultimate Steering & Readout
- Hardware required
- Ultimate configuration by JTAG slow control
- IPHC DAQ System for Ultimate Characterization
- Interface Ultimate / General acquisition board

Steering & Readout : Ultimate ?

Ultimate ?

- **Matrix of 890 880 pixels : 960 columns x 928 lines – 19,872 mm x 19,210 mm – 20,7 µm pitch – 185,6 µs integration time**
  - **Normal digital data stream after Zero Suppression (ZS)**

Steering

- **Configuration (operating modes, bias etc …) by JTAG slow control**
- **Main clock 160 MHz**
  - **On board oscillator (single Ultimate setup)**
  - **Provided by external oscillator (Telescope or ladder setup)**
- **Start command**
  - **By JTAG slow control (single Ultimate setup)**
  - **By external HW signal (Telescope or ladder setup)**

Readout

- **Normal ZS output** - **Full memory size → 2 Outputs at 160 MHz**

Steering & Readout : Signals ?

Readout configuration N° 3 : 2 outputs @ 160 MHz

Summary

- Data generated on rising edge of Ultimate output clock
- Synchronization signal MKD – Duration 4 clocks cycles
- Data LSB first
- First bit of frame = Header LSB

Readout configuration N° 3 : 2 outputs @ 160 MHz

- **Provides the whole states memory size : 1850 W16 (word of 16 bits) – 925 W16 / link**

Summary

- **Data generated on rising edge of Ultimate clock**
- **Header** → **16 bits / output**
- **Frame counter** → **16 bits / output**
- **Data length (useful part of data)** → **16 bits / output (Sum the 2 W16 to get matrix W16 size)**
- **Data (format on next slide)** → **Max = 1850 x 16 bits / output**
- **Trailer** → **16 bits / output**
- **Padding zero** → **32 bits / output**
- **Total stream size per output : 29696 bits = 1856 W16 = 3712 W8**

Steering & Readout : Data Format

Readout configuration N° 3 : 2 outputs (D0, D1) @ 160 MHz

- **If there is at least one hit in one line, the following data stream is generated**
  - **Status/Line word**
    - **Address of line**
    - **Number of States (9 Max, overflow flag if > 9)**
  - **States list – One state = consecutive pixels at 1 in the line**
    - **Column address of the first pixel at 1**
    - **Number of pixels at 1 - Warning : 0 means one pixel at 1 (value → pixel nb : 0 → 1, 1 → 2, 2 → 3, 3 → 4)**
- **For each line with hit : one Status/line followed by up to 9 States**

Status/ line															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit(0-3)				Bit(0-9)											
number of *States*				The address of the line										Not used	OVF

State															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit(0 -1)		Bit(0-9)													
number of hit pixels		the address of the column										not used			

Steering & Readout : Bit stream Mux on D0, D1

Readout configuration N° 3 : 2 outputs (D0, D1) @ 160 MHz

- Each output has one Header, Frame counter, Data length, Trailer as W16 fields
  - It may be wise to build W32 fields
    - Low 16 bits = field on output D0
    - High 16 bits = field on output D1
  - Data length ?
    - The total data length is the sum of the two fields (on D0, D1)

- Useful data multiplexed over D0 and D1
  - The first W16 is on D0, next on D1, and so on
  - What happens if total W16 number is odd ?
    - Same W16 number / output – Total is always even !
    - A dummy W16 is added at end of D1 stream

Hardware : Ultimate PCB

Mimosa 26 test boards → Same boards chain for Ultimate

Mimosa 26
Proximity board

Digital
Auxiliary board

JTAG Interface Board
PC // Port ← → LVDS

JTAG
CTRL

JTAG
From DAQ

Start & Speak
From DAQ

Digital Data – Sync – Clock : To Digital DAQ

Analogue Test of Mimosa 26

Digital Test of Mimosa 26

Wojciech.Dulinski@IReS.in2p3.fr

Matthieu.specht@ires.in2p3.fr

Four boards required to test Mimosa 26

- PCB development — W.Dulinski – M.Specht
- Boards assembly by Micro-Technique Team — M.Imhoff – O.Clausse – L.Ankenmann
- Bonding by Micro-Technique Team — C.Wabnitz
- Interface / Micro-Technique & Boards Testing — M.Specht

Ultimate → Make a new " Proximity board "

- Only one new board to design
- Keep all others boards
- But should not forget time needed to produce and test ALL boards

Ultimate configuration : JTAG slow control

Mimosa 26 JTAG → Same software chain for Ultimate

A Windows application to Control the ~ 50 Configuration Parameters of Mimosa 26

- Uses JTAG slow control via PC parallel port
  - Requires a free // port on PC
  - We provide the software as an executable GUI Windows application
- A COM interface allows to control JTAG application by a third party software
  - JTAG can be controlled by DAQ software
  - COM allows access at GUI parameters levels / register levels (library)

Kimmo JAASKELAINEN
Kimmo.jaaskelainend@ires.in2p3.fr

Emulation of Mimosa 26 JTAG Controller

DAQ System : For Ultimate characterization

Mimosa 26 DAQ → Same DAQ chain for Ultimate (HW + SW)

Client / Server : NI - PXI Crate data server + Supervisor PC data client

Supervisor

- PC Windows

PXI DAQ

- Digital acquisition board
- CPU board & HD

Mi26 emulation with pattern generator

Mi 26 / Ultimate

- PXI 6562 2 / 16 Mbits / input – Deserialization by SW
- Mimosa 26 → 2 signals @ 80 MHz – 9216 bits / frame / link
  - Acquire up to 227 / 1816 frames on board → 180 / 1800
- Ultimate → 2 signals @ 160 MHz – 29696 bits / frame / link
  - Acquire up to 70 / 560 frames on board
- Conclusion → No problems for tests at laboratory
  - PXI 6562 max freq = 200 MHz > Ultimate 160 MHz
  - Beam test → Store 1/3 of frames / spill / Mimosa 26
  - But No limitation on new DAQ based on Flex RIO

National Instrument

PXI Crate

PXI 6562 DIO Board

- 16 LVDS inputs up to 200 MHz
- 2 / 16 MBits / input on board memory
- Deserialization done by SW
  - Easy to upgrade from Mi26 to ultimate

Gilles CLAUS
Gilles.claus@ires.in2p3.fr

Ultimate / General acquisition board : Interface ?

For Ultimate normal readout (Not test modes)
→ Beam Telescope - Ladder

- **Ultimate HW Interface**
  - **Need start signal**
  - **Provide : 160 MHz clock, Synchro signal, 2 data links @ 160 Mbit/s**
  - **Maximum frame size = 29696 bits / link ⇔ ~ 40 MB/s**

- **The board must be able to :**
  - **Provide Start signal synchronized on clock falling edge**
    - **It may be easier to provide both : 160 MHz clock & Start**
  - **Acquire two LVDS links at 160 MHz per Ultimate**
  - **Store on board at least one frame → 29696 bits / link**
    - **Better to store consecutive frames → N x 29696 bits**
  - **Sustain a data rate ~ 40 MB/s / Ultimate if we want to avoid dead time**
  - **Deserialize data on board (fw)**
  - **Handle trigger & variable event size (fw)**