Ultimate Test & Characterization resources at IPHC

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OUTLINE

- **Introduction** : MAPS test & characterization protocol
- **Testability** : Ultimate vs Mimosa 26
- **Test** : Functional test & Zero Suppression Test
- **Characterization** : From laboratory → To beam test
- **Test equipments** : Hardware – Firmware - Software
- **Tests schedule** : Example of Mimosa 26
- **Conclusion** : Planning to setup Ultimate tests

MAPS
Functional test

MAPS Test & Characterization Protocol

- Define **Testability** upstream → At beginning of MAPS design
  - At each level : pixel, discriminator, zero suppression logic, data stream

- MAPS **Standard characterization** protocol
  1. Functional test → Smoke test, MAPS " under control " → Provide data
  2. Pixels characterization at lab Fe 55 → Calibration peak, CCE, Noise
  3. Pixels + Discriminators characterization → Noise, Threshold dispersion
  4. Beam test → S/N, Spatial resolution, Detection efficiency

  - Irradiation tests → Redo steps 2, 3, 4 – Latch up tests

MAPS
Calibration

MAPS
Beam test

Mimosa 26 (2009) = ½ Ultimate -- First sensor with zero suppression (ZS)

- Final sensor for EUDET Beam Telescope
  European project FP6 – Detectors R&D toward ILC
- Integration of Digital MAPS & Zero suppression logic
  - Mimosa 22 → Digital MAPS 128 rows x 576 lines (2008)
  - SUZE → Zero suppression logic (2008)
- Key numbers
  - Pixels number : 663 552 pixels
    - 1152 columns x 576 rows
  - Active area : ~ 2 cm² (21,197 mm x 10,598 mm)
  - Pixels pitch 18,4 µm
  - Readout time 115,2 µs → 8680 frames / s
- Data flow with zero suppression (ZS) → ~ 20 MB/s
  - Two serial links @ 80 MHz - ~ 9 kbit / frame
- Bypass ZS for characterization ? → Data flow would be 678 MB/s !
  - It's not the solution to characterize pixels ☹
  - Find another way to characterize Mimosa 26 & Ultimate …

Testability at each level (Mimosa 26) → What does it mean ?

- At pixel level
  - Why → For pixel characterization (Fe55 : Gain, Charge collection)
  - How → Access to 8 column group / 1152 – Scanning by groups of 8 columns
  - Readout at ~ nominal integration time but only 8 columns at a time

    → In fact at 4 x nominal integration time

- Discriminators level in standalone mode = Discriminators only
  - Why → For discriminator characterization (Threshold, Noise)
  - How → Emulate pixel signal with two adjustable DC levels (JTAG)
  - Discriminators control logic at nominal speed but we take 1 sample / 576

- Pixel + discriminator level
  - Why → For pixels + discriminators characterization (Threshold, Noise)
  - How → Access to 1 line / 576 – Scanning whole matrix line by line
  - Pixel at nominal integration time & discri control logic at nominal speed

- Zero suppression (ZS) logic in standalone mode = ZS only
  - Why → To test zero suppression algorithm
  - How → Emulate pixels states of two matrix line → configurable patterns

Testability at each level → We should not forget communication with MAPS !

- Analogue output side → Can we get analogue signal from MAPS ?
  - Configure MAPS via JTAG
  - Analogue signal emulated by two configurable DC levels
  - Check the analogue pattern (with scop)
- Input side → Can we configure MAPS via JTAG slow control ?
  - Write to JTAG registers, read back & compare
  - Test if we can control BIAS via DACs → Measure voltage on test points
- Digital output side → Can we get digital signal from MAPS ?
  - Configure MAPS via JTAG
  - Digital signal emulated by a configurable pattern generator
  - Check the digital pattern (automatic test with DAQ)

Ultimate vs Mimosa 26 → X 2 → Surface – RO Frequency – Data stream

Mimosa 26

Test pads for analogue outputs

Pixel Array

- Area ~ 2 x 1 cm²
- Column number 1152
- Row number 576
- Pitch 18,4 µm
- Integration time 115,2 µs
- Output data stream
  - 2 links @ 80 MHz
  - ~ 9 kbits / link / frame
  - Total ~ 20 MB/s

Column-level Discriminators

Zero suppression

JTAG | Memory 1 | PLL | Seq. Ctrl | Memory 2 | Bias-DAC

Pad Ring … Out 0 Out 1

Ultimate

Test pads for analogue outputs

Pixel Array

- Area ~ 2 x 2 cm²
- Column number 960
- Row number 928
- Pitch 20,7 µm
- Integration time 185,6 µs
- Output data stream
  - 2 links @ 160 MHz
  - ~ 30 kbits / link / frame
  - Total ~ 40 MB/s

Column-level Discriminators

Zero suppression

JTAG | Memory 1 | PLL | Seq. Ctrl | Memory 2 | Bias-DAC

Pad Ring … Out 0 Out 1

The two sensors have the same architecture → Difference = Scaling x ~ 2

Ultimate (2009) → Testability improvements

- **Key** numbers
  - **Pixels** number : **890 880 pixels**
    - **960 columns x 928 rows**
  - Active **area** : **~ 4 cm²** (19,872 mm x 19,210 mm)
  - Pixels **pitch 20,7 µm**
  - **Readout** time **185,6 µs** → 5388 frames / s
- **Data flow** with zero suppression (ZS) → **~ 40 MB/s**
  - **Two** serial **links @ 160 MHz** - ~ 30 kbit / frame
- **Testability** improvements
  - Pixel characterization → Solve Mi26 limitation
    - **8 fixed columns** (middle of matrix) **at nominal integration time**
    - Scanning mode still available (4 x Integration time)
  - ZS logic & Interface / DAQ
    - **Hit emulation** over one full line (or more)
      - By external signal synchronized to Ultimate readout
    - Select columns via JTAG

Functional Test → A process in 2 steps

Functional Test on MAPS reception

Evaluate if MAPS "is alive" ?

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Mimosa 26

Zero Suppression (ZS) logic test

Test ZS algorithm implementation

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Check list

- Power consumption within limits after reset ?
- MAPS responds to slow control (JTAG) ?
  - Write / Read registers – Control DACs
  - Set default bias → Measure power consumption
- MAPS provides analogue & digital signals ?
  - Check pattern & timing with scop
- Check interface with DAQ
  - Acquisition of well known pattern – Count errors
- Pixels respond to Fe 55 → Can we see hits ?

Intensive tests

- Extract relevant tests from simulation
- Perform theses tests on the real MAPS
  - Emulate matrix pattern (configured via JTAG)
  - Get ZS result by DAQ – Compare / Expected result
- Evaluate robustness of logic
  - Run test during one night (~ 20 x 10^6 Frames)
  - Count errors
- Find operating limits → Run test until it fails
  - Varying → Frequency, Vddd, Temperature

Pixel characterization → Pixel only = via analogue test outputs

Calibration at laboratory with Fe ^{55}

Fe ^{55} peak – CCE - Noise

Mimosa 26

MAPS
&
Source

On-line monitoring

Off-line analysis

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Characterization procedure

- **Calibration** peak, **CCE** with Fe 55 & **Noise**
- Measurement done on 8 columns / 1152
  - Not used → Requires too much stat !
- **Scan whole matrix** : 144 x blocks of 8 columns
  - Run of 2000 events – 5 GB – Time ~ ½ Hour
  - Analysis ~ 1H30 → Total time ~ 2H00 / Run
- Study influence of **critical parameters**
  - Temperature
  - Irradiation → Ionizing & Neutrons

Discriminators characterization → Discriminators only (pixel level emulated)

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Characterization procedure

- Scan discriminators threshold to get " S curves "
- One curve / discri → 1152 curves (288 / Matrix)
  - One threshold → Run of 1000 events ~ 3 minutes
- Extract
  - Noise distribution → TPN ~ 0,4 – 0,5 mV
  - 50 % Threshold distribution → FPN ~ 0,2 mV
  - 30 Threshold steps → 1H30 DAQ + 1 H Analysis
  - Total 2H30
    (Rq : 576 x more stat than needed taken ←→ Pixel mode)
- Study influence of critical parameters
  - Temperature
  - Irradiation → Ionizing & Neutrons

Pixel + Discriminator characterization → The whole chain …

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Characterization procedure

- Scan discriminators threshold to get " S curves "
- One curve / pixel → 663 552 curves (165888 / sub matrix)
  - One threshold → Run of 1000 events ~ 3 minutes
- Extract
  - Noise distribution → TPN ~ 1 mV
  - 50 % Threshold distribution → FPN ~ 0,3 – 0,4 mV
  - 30 Threshold steps → 1H30 DAQ + 1 H Analysis
  - Total 2H30
- Study influence of critical parameters
  - Temperature
  - Irradiation → Ionizing & Neutrons

" Crocodile pixels " → The KKJ & HP definition

What is a pixel croco ?

- It happens on one or two threshold scan steps
- Threshold shifts back from few steps → ~ 0,5 – 1 mV
- Connected to number of pixels which switch 1 / 0

« Crocodile pixels team »

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Pixel « crocodile pixel » definition by K.Jaaskelainen & H.Pham

The « croco » phenomenon corresponds to a shift of ~1mV of threshold value

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" Crocodile pixels " → Seems to be a consequence of test procedure

Context which produce " croco "

- Characterize pixels + discriminators
- Doesn't appear on discriminators only
- Connected to number of pixels which switch 1 / 0

Context which suppress " croco "

- Limit the number of " pixels " for the test
- Done by disabling discriminators

Conclusion → As far as we know …

- It's not at discriminator level
- Should not be a problem on normal mode → Less pixel activated → No bad behaviour seen on beam tests results
- Problem has been studied in details → No simple / evident conclusion → shall we continue to investigate ?

Beam test → Test MAPS with a reference Telescope

MAPS (Mimosa 26)

Mimosa 26 Telescope
Resolution ~ 3 um

On-line monitoring

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Beam test campaigns

- Measure detection characteristics
  - CE with MIP
  - Detection efficiency + Spatial resolution
- Tests done at
  - CERN → Pion 120 Gev
  - DESY → Electron 5-6 Gev
  - Beam test campaigns ~ 4-6 weeks / year
- Study influence of critical parameters
  - Temperature
  - Irradiation → Ionizing & Neutrons

What do we need to test & characterize Mimosa 26 → Ultimate

2 – Slow Control (JTAG) for Mimosa 26 Configuration

JTAG via PC // Port

1 – PCB for Mimosa 26 Proximity & Auxiliary boards

3 – Analogue DAQ for Pixels Test

5 – Analysis software

Fe^{55} charge collection

4 – Digital DAQ

- Normal ZS output
- Discriminators + Pixel Test

Discriminators transfer functions

We need …

1. PCB on which Mimosa 26 is bonded & Signals buffer boards
2. Slow control to configure Mimosa 26
3. Analogue DAQ for pixels characterization
4. Digital DAQ for normal ZS output & discriminators characterization
5. Analysis software

Mimosa 26 test boards → Same boards chain for Ultimate

Four boards required to test Mimosa 26

- PCB development — W.Dulinski – M.Specht
- Boards assembly by Micro-Technique Team — M.Imhoff – O.Clausse – L.Ankenmann
- Bonding by Micro-Technique Team — C.Wabnitz
- Interface / Micro-Technique & Boards Testing — M.Specht

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Ultimate → Make a new " Proximity board "

- Only one new board to design
- Keep all others boards
- But should not forget time needed to produce and test ALL boards

Mimosa 26 DAQ → Same DAQ for Ultimate

3 – Analogue DAQ for Pixels Test

4 – Digital DAQ

- Normal ZS output
- Discriminators + Pixel Test

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DAQ constraints

- **Analogue DAQ**
  - IPHC A/D board 4 Inputs – 12 bits – 40 MHz – USB2.0
  - Mimosa 26 → 8 signals @ 10 MHz – 165888 samples
  - Ultimate → 8 signals @ 10 MHz – 222720 samples
  - No heavy constraint Mimosa 26 → Ultimate
- **Digital DAQ**
  - NI PXI 6562 board – 16 Inputs 200 MHz – PXI
  - Data deserialization → Done by SW
  - Mimosa 26 → 2 signals @ 80 MHz – 9216 bits / frame
  - Ultimate → 2 signals @ 160 MHz – 29696 bits / frame
  - No heavy constraint Mimosa 26 → Ultimate

Timing

- Mimosa 26 back from foundry 02/18/2009
  - First, it must be bonded on PCB and after tests can start
- Operational on 02/20/2009 → Do + 3 Days !
  - Readout 26 OK & See Fe 55 hits on pixels
- Base characterization ~ 6 months
- Beam test at CERN beginning September
- Question !
  - When do they test their test benchs ???

→ Mimosa 26 emulation

Mimosa 26 JTAG controller emulated on a FPGA Virtex 4

Mimosa 26 interface to DAQ parts

- Slow control
- Output data stream

had been emulated in order to check DAQ before we get Mimosa 26 from foundry

Mimosa 26 data stream emulated via a pattern generator

Is there something to improve in characterization protocol → Always !

- On MAPS Standard characterization protocol
  - Functional test – Pixel characterization – Beam test
  - Define & measure key parameters to establish a " gabarit" for functional tests
    - IVddd, IVdda current (after reset, configured, normal running)
    - Common current reference value
    - DAC transfer curves (→ slope, offset, non linearity)
- Increase resources involved in Electronic characterization protocol
  - What does it mean ?
    - Study power supply influence on → Pixel - DAC, discri reference threshold, real threshold
    - Digital parts → Power supply, frequency limit, clock & data stream integrity
  - We should run this protocol in parallel with standard protocol

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(uTech) Micro Technics Team (M.Imhoff & Co)

Planning to setup Ultimate test equipments → Tasks running in ~ //

- **Board** design + Production → 6 weeks
  - Design 2 weeks (WD)
  - Buy components & Production 2 weeks (MS & uTech)
  - Assembly 1 week (uTech) – Testing 1 week (MS)
- **Slow control** (JTAG) → 4 weeks
  - SW development 2 weeks (KKJ) – Ultimate emulation + Tests 2 weeks (KKJ)
- **Digital DAQ** → 3 weeks
  - Ultimate emulation (160 MHz) → 1 week (MS)
  - SW upgrade (Ro, GUI, Monitoring) + Tests → 3 weeks (GC)
- **Analogue DAQ** → 1 week
  - Ultimate emulation + check DAQ (upgrade needed ?) → 1 week (MS)
- **Analysis SW** upgrade → 4 weeks
  - Analogue (Fe^{55} calibration) → Not needed
  - Digital (Pixel + discri "S" curves) → 2 weeks (MG^1) + 2 weeks (MG^2)

Conclusion
Total = ~ 6 weeks
Get Ultimate from foundry ~ 8 weeks

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(uTech) Micro Technics Team (M.Imhoff & Co)

Backup slides

- Ultimate readout protocol
  - star_dr_120610__test_1_gc__ultimate_normal_readout_protocol_hw__v1.pdf
- Ultimate test data link
  - star_dr_120610__test_2_gc__ultimate_test_data_link__v1.pdf
- Ultimate analog test modes
  - star_dr_120610__test_3_gc__ultimate_pixel_analog_charact_modes_v1.pdf
  - mimosa26_analog_daq_hw_sw_v1.0.pdf
- Ultimate digital test modes
  - star_dr_120610__test_4_gc__ultimate_pixel_discri_digi_charac_modes_v1.pdf
- What about Mimosa 26 / Ultimate probe testing ?
  - star_dr_120610__test_5_gc__probe_testing_at_iphc_v1.pdf

Conclusion 4/4 – Test team

HW & SW Development
ASIC Emulation

Matthieu SPECHT

MAPS Designer & Test

* Guy DOZIERE

MAPS Characterization
Beam test analysis

Marie GELIN

Slow Control - FW development
Conception – Characterization
PLL – Fast serial links

Kimmo JAASKELAINEN

Test bench definition - Coordination
DAQ SW development & Monitoring

Gilles CLAUS

MAPS Designer & Test

* Hung PHAM

MAPS Designer & Test

* Wojciech Dulinski

Plume ladder tests
Beam test analysis

Nathalie CHON-SEN

MAPS Characterization
Beam test technical support

Mathieu GOFFE

** MAPS designers also involved in testing*