Ultimate

IV- Optional blocks

(Preliminary version)

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Document history		
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1.0	November 2010	Ultimate design review: the optional blocks

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Introduction

Two optional blocks are implemented in the Ultimate sensor for test purpose to prepare the future developments. Therefore, these blocks are designed as individual blocks with their own padring.

The first block is a PLL designed by Quan Sun and implemented in the MIMOSA-26 sensor. An improved version has been implemented in the MIMOSA-22TER prototype. The architecture of the PLL is presented in the paragraph 1-1 and the preliminary measurement results are shown in the paragraph 1-2.

The second block is a voltage regulator which allows providing the analogue voltage supply from the digital voltage supply. This block has been designed by Jia Wang and the simulation results will be presented in the paragraph 2.

1- The PLL

1-1-The PLL design

Quan Sun

The PLL architecture and feature

The proposed charge pump PLL architecture is illustrated in Fig. 1. A conventional PLL loop which contains a phase frequency detector (PFD), a charge pump, a loop filter, a VCO and a frequency divider is the core of the design. A power-on reset (PoR) block generates a reset signal when power is applied to the PLL. This reset signal is provided to the frequency divider and loop filter to ensure that the device starts operating in a known state. A bias generator provides reference current to the charge pump and the VCO respectively.

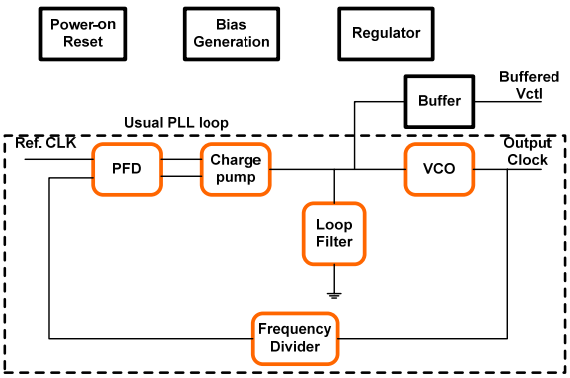


Fig. 1 charge pump PLL architecture

Main noise contributions of a charge pump PLL consist of an external reference noise, PFD and charge pump noise, loop filter noise, and VCO internal noise. Each of these noise contributions includes device-inherent noise and power supply noise. Power supply noise of each component could be converted to VCO control voltage noise with a transfer function $H_n(s)$, as shown in the PLL noise model of Fig. 2.

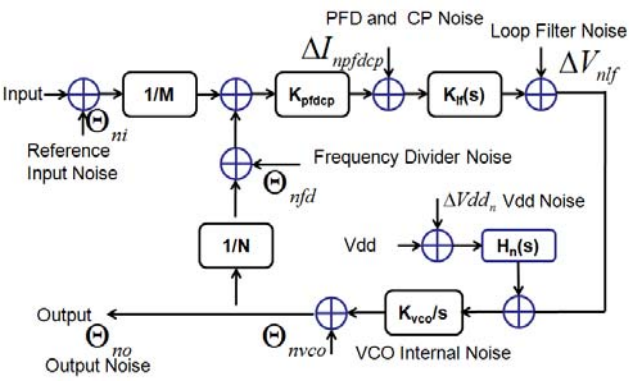


Fig. 2 Simplified PLL noise model including supply noise

In the locked condition, the output noise Θ_{no} of the PLL could be expressed as:

$$\Theta_{no} = \left\{ \left[\left(\frac{\Theta_{ni}}{M} - \frac{\Theta_{no}}{N} - \Theta_{nfd} \right) \cdot K_{pfdcp} + \Delta I_{npfdcp} \right] \cdot K_{lf}(s) + H_n(s) \Delta Vdd_n \right\} \cdot \frac{K_{vco}}{s} + \Theta_{nvco}$$

where

Θ_{ni}	Reference clock noise of the PLL
ΔI_{npfdcp}	Noise attributed to the phase frequency detector and charge pump
Θ_{nfd}	Noise of the frequency divider
ΔVdd_n	Noise of voltage supply
$H_n(s)$	Equivalent transfer function from the power line to the VCO control voltage

In our case, the pixels and digital subsystem integrated on the same substrate steer hundreds of milli-ampere current between supply and ground, thereby the power supply noise from digital circuits and the pixels are the major noise sources.

From the block point of view, the VCO is the most significant noise source in a PLL. Noise generated from VCO includes 1/f noise, thermal noise, and power supply noise. The noise manifests itself as jitter at the output of the VCO. The contribution of the device electronic noise to jitter is typically less then that due to supply and substrate noise. For this reason, a clean power supply for the VCO is necessary to implement a low jitter PLL. Moreover, stable dynamics and VCO range could also be obtained so long as the regulated power supply is process, voltage and temperature (PVT) insensitive.

Being analog circuit, charge pump is also sensitive to supply noise. The supply noise would directly introduce ripples on control voltage of the VCO through charge pump. Therefore, providing a stable supply voltage to charge pump is also imperative. In addition, in order to get better current matching and provide wide enough control voltage range, charge pump requires relative larger headroom than VCO.

As discussed above, two regulated voltage supplies are necessary in our PLL, as shown in Fig. 3. The first one with good stability and large headroom supplies the charge pump. The second one with better PSNR performance provides power supply to the VCO and the bias generator. The VDDD is the digital power supply which supplies the PoR, the Buffer, the PFD, a Level Shift (an internal block in the VCO), the Frequency Divider and the first Regulator. The value of each regulated supply is designed according to the supply requirement of charge pump and VCO respectively.

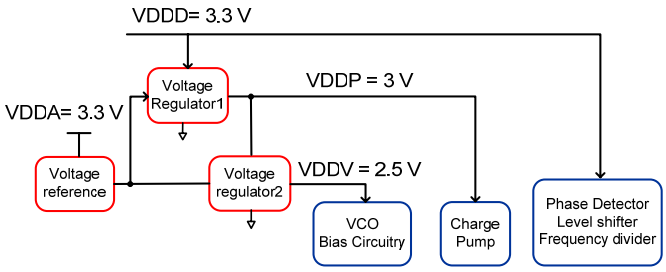


Fig. 3 Block diagram of low-jitter PLL power supply distribution

The voltage regulator design

Fig. 4 shows the block diagram of a typical linear voltage regulator consisting of a voltage reference, an error amplifier, an output transistor, and a load capacitor, which sets up output pole. R1 and R2 are served as divider resistors to provide a feedback voltage, determining output regulated voltage.

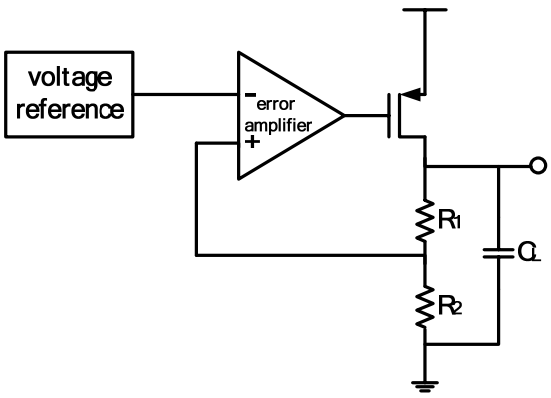


Fig. 4 block diagram of a linear voltage regulator

There are several specifications that determine the performances of a linear voltage regulator. In charge pump PLL supply application, PSNR which is defined as ripple voltage on Vout over ripple voltage on Vdd is one of the most important characteristic.

$$PSNR = \frac{v_{Rout}}{v_{Rdd}}$$

The analysis of PSNR follows from the power supply rejection ratio (PSRR) analysis of operational amplifier, which has been analyzed in many texts. A simple model for analyzing the PSNR of linear voltage regulators over a wide range of frequencies was proposed. Fig. 5 shows a typical PSNR curve of the internal miller compensation linear voltage regulator.

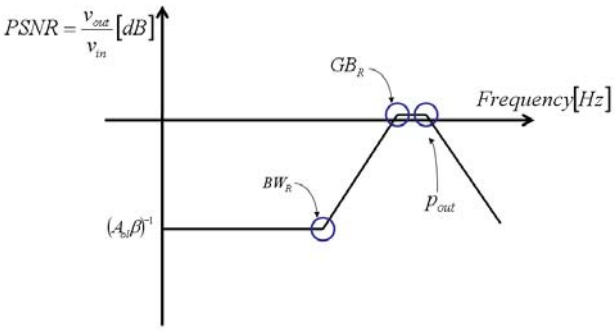


Fig. 5 typical PSNR curve of voltage regulator

As the model predicted, the PSNR at low frequencies, its zero, and two poles correspond to the DC open loop gain $A_{ol}\beta$ (β is the feedback factor determined by two resistances), the bandwidth BW_R, the unity-gain frequency GB_R, and the output pole dominated by output capacitor (p_{out}), respectively. The curve indicates that the worst case of the PSNR occurs at frequency nearby GB_R. Intuitively, the regulator provides good PSNR at low frequency according to high loop gain, and then it would degenerate along with the decreasing of loop gain at middle frequencies, while the output capacitor shunts ripple at output node to the ground at high frequencies. That means, serving as the power supply, the regulator would introduce noise at middle range of frequencies, which is around 20MHz in our technology. Following portion of the section describe circuit realization of voltage regulator.

The voltage reference

The Bandgap of silicon determines both the voltage drop and the current-voltage curve of a forward biased PN-junction. These values are predictable and are not subject to process

variations. So, they are suitable for generating a generally stable voltage reference. A schematic of CMOS Bandgap voltage reference is shown in Fig. 6.

The PSNR of the Bandgap reference is significant as any fluctuations at the output of reference whose frequencies is lower than gain bandwidth of the regulator, could appear at the output of the regulator. In the Bandgap reference, as long as the open-loop gain of the op-amp is significantly high, the output voltage would be relatively independent of the supply voltage. In addition to this, the PSNR of the reference could be enhanced by placing a relatively large capacitor at the output node to shunt ripple to ground at high frequency. Fig. 7 shows the simulated PSNR of the Bandgap reference.

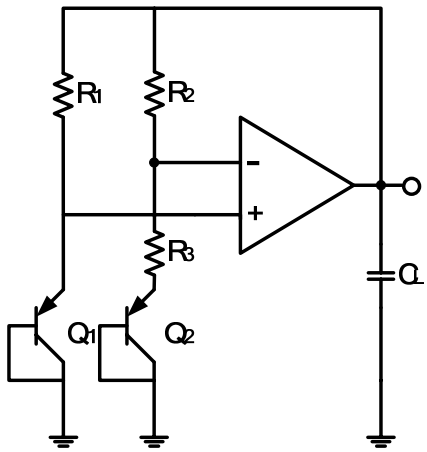


Fig. 6 Simplified schematic of Bandgap voltage reference

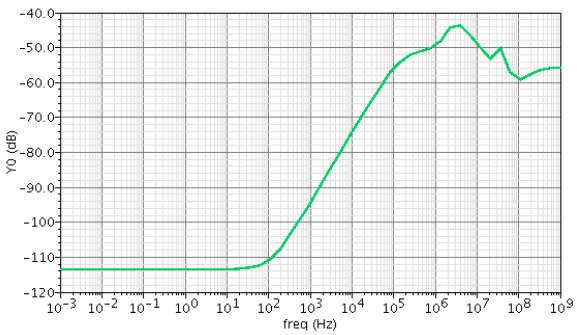


Fig. 7 Supply noise rejection of Bandgap reference

The regulators

As discussed before, the PSNR of regulator suffer from a peak in the neighborhood of GBR. This peak is caused by complex poles in the transfer function of the LDO (Low Dropout Regulator), and could be reduced substantively by increasing load capacitor. In order to achieve good stability of regulated voltage, load capacitor should be placed close to LDO.
Generally speaking, the power supply noise rejection in the regulator could be improved by increasing power supply rejection ratio (PSRR) in op-amp. In the closed-loop configuration, the output ripple, saying V_{OR}, in the regulated output voltage can be estimated in accordance with

$$V_{OR} \approx \frac{1}{\beta} \cdot \left(\frac{V_{DDR}}{PSRR} + V_{BGR} \right)$$

where β is the feedback factor determined by the two resistances, and VDDR and VBGR represent the ripple voltage on the power supply line and the band-gap reference output respectively.

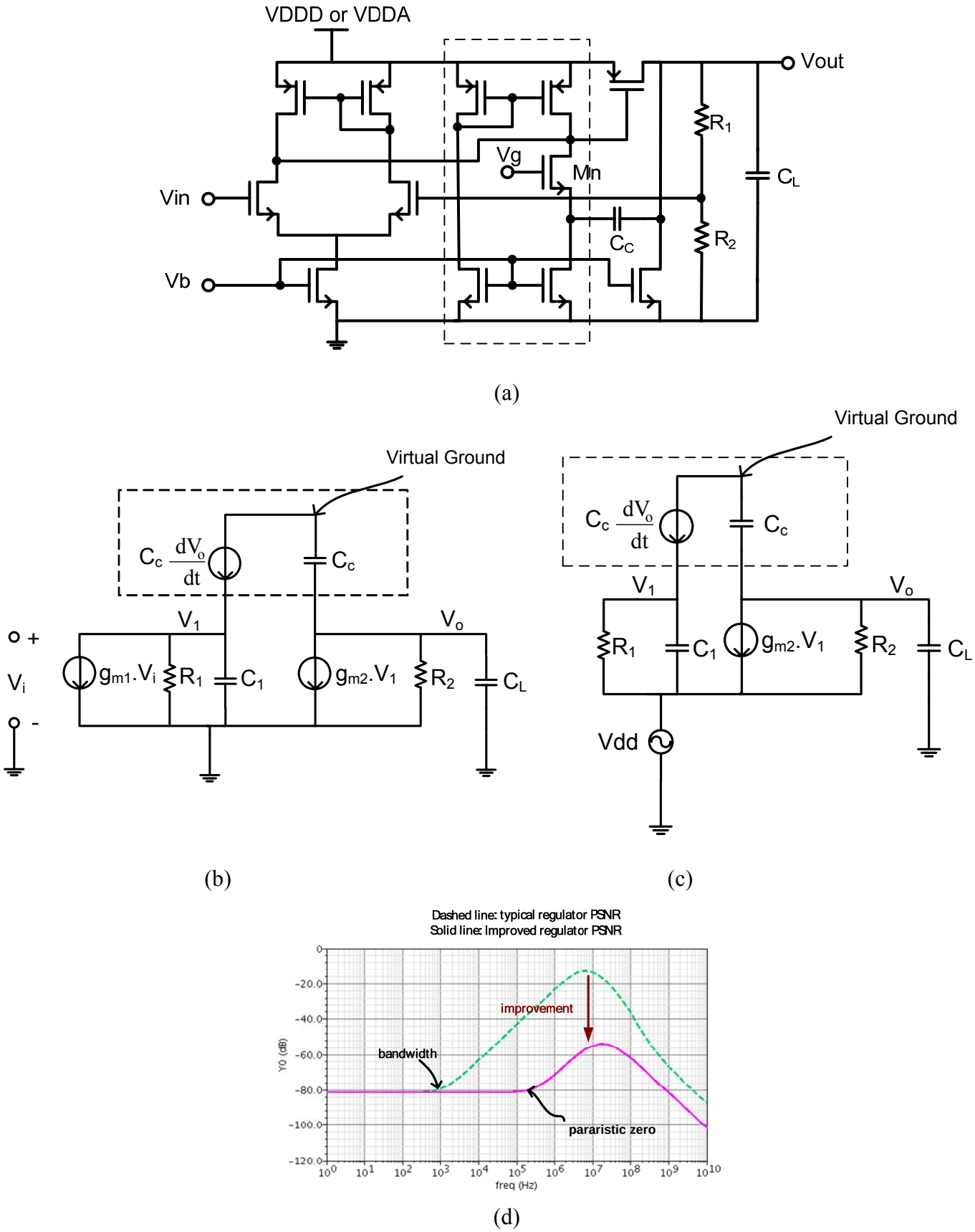


Fig. 8 (a) Schematic of regulator with enhanced PSNR, (b) AC small signal model for open-loop transfer function analysis, (c) AC small signal model for open-loop PSNR analysis, (d) conceptual PSNR improvement with and without virtual grounded cascode compensation technique.

The PSRR at high frequency of two stage amplifier could be improved by using of the virtual grounded cascode compensation technique (VGCC), as shown in Fig. 8 (a). Intuitively, since the gate of transistor Mn is virtual grounded, the source of the transistor, namely, the left terminal of the compensation capacitor, is insensitive to power supply noise. The displacement current from the capacitor flows into source of Mn. In effect, this feed-back path cancels the feed-forward path that could degenerate the positive PSRR at high frequency. The transistor Mn should be biased in the saturation region and so as to isolate the capacitor from the power supply noise. In order to analysis this circuit, a conceptual open-loop ac small signal model is demonstrated in Fig. 8 (b). Here the compensation capacitance is shown to be connected between the output node and a virtual ground, while the controlled current source having the value of $C_C dV_o/dt$ charges the first-stage output. It can be proofed for such an arrangement the open-loop transfer function of the circuit is given by:

$$A = \frac{A_1 A_2}{1 + s[R_1 C_1 + R_2(C_C + C_L) + A_2 R_1 C_C] + s^2 R_1 R_2 C_1 (C_C + C_L)}$$

where $A_1=g_{m1}R_1$, is the dc gain of the first stage, and $A_2=g_{m2}R_2$, is the dc gain of the second stage. Assuming two poles are widely spaced, two poles are given by:

$$p_1 \approx -\frac{1}{g_{m2} R_2 C_C R_1},$$

$$p_2 \approx -\frac{g_{m2} C_C}{C_1 (C_C + C_L)}$$

Assuming the parasitic capacitance C_1 being much smaller than the compensation capacitor C_C or the load capacitance C_L, the unity gain frequency GBW is given by g_{m1}/C_C which is the same as of a two stage op amp with miller compensation and a nulling resistance. The conceptual ac small signal model for open-loop positive PSNR analysis of Fig. 8 (a) is shown in Fig 8 (c). It can be shown that open-loop positive PSNR is given by:

$$\frac{V_o}{V_{dd}}\Big|_{open-loop} = \frac{1 + sC_1 R_1}{1 + s[R_1 C_1 + R_2(C_C + C_L) + A_2 R_1 C_C] + s^2 R_1 R_2 C_1 (C_C + C_L)} \approx \frac{1 + sC_1 R_1}{(1 - \frac{s}{p_1})(1 - \frac{s}{p_2})}$$

This equation indicates that it has the same poles as the open-loop gain and a zero which is created by the parasitic capacitance at the first-stage output. Thus, in the unity gain configuration, the PSNR is given by:

$$\frac{V_o}{V_{dd}}\Big|_{unitygain} = \frac{1 + sC_1 R_1}{(1 - \frac{s}{p_1})(1 - \frac{s}{p_2})} \cdot \frac{1}{1 + A_1 A_2 \beta / (1 - \frac{s}{p_1})(1 - \frac{s}{p_2})} \approx \frac{1 + sC_1 R_1}{A_1 A_2 \beta (1 - \frac{s}{p_1'})(1 - \frac{s}{p_2'})}$$

$$p_1' = -GBW\beta$$

$$p_2' = p_2$$

$$z' = -\frac{1}{C_1 R_1}$$

The equations imply a flat response at $-20\log A_1 A_2 \beta$, until parasitic zero frequency of the first stage where it starts to degrade at 20 dB/decade rate, then flat again at GBW and decreases at -20 dB/decade rate since the second pole frequency. This is demonstrated in Fig

8 (d) assuming β=1. At frequency nearby unity gain frequency, PSNR performance is improved a lot by using VGCC technique. The improvement of the PSNR is -20log ($g_{m2}R_2C_C/C_1$) which mainly results from multiple of the zero frequency by a factor of $g_{m2}R_2C_C/C_1$ with respect to bandwidth. By using VGCC technique, at the cost of a slight increase in complexity, noise and power dissipation, the PSNR at high frequency is greatly improved.

The PLL blocks implementation

The detailed architecture of the PLL is shown in Figure 9.

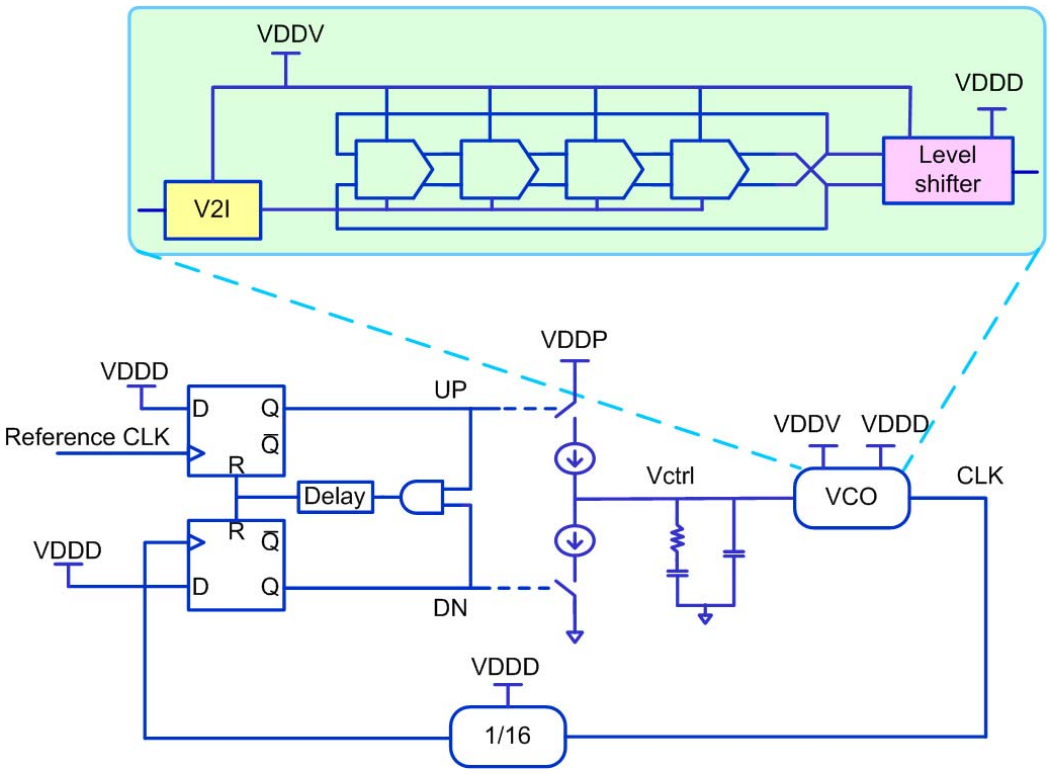


Figure 9: PLL core

The Phase-Frequency Detector and Charge Pump

The phase-frequency detector uses a tri-state logic block (see Figure 9). The UP and DN signals controls the charge pump. Two D flip-flops with D=1 are triggered by two clock signals which are compared. Ideally, the three states are UP, DN and high impedance. If the reference clock leads the feedback clock, the UP state is generated while DN state is produced for the opposite condition. The filter is in high impedance state at steady state. In order to avoid the dead-zone around zero-phase error leading to increased noise, the forth state where the UP and DN pulses are "high" simultaneously is enlarged by inserting a delay in the reset path. This ensures that the switches in the charge pump could be opened even if a tiny phase error exists between the reference clock and the feedback clock.

The delay time has been optimized in order to minimize the dead zone and to limit the perturbation on the control voltage in the steady state of the PLL.

The charge pump schematic, depicted in Figure 10, uses a dummy switch structure to limit the charge injection and clock feedthrough mismatch.

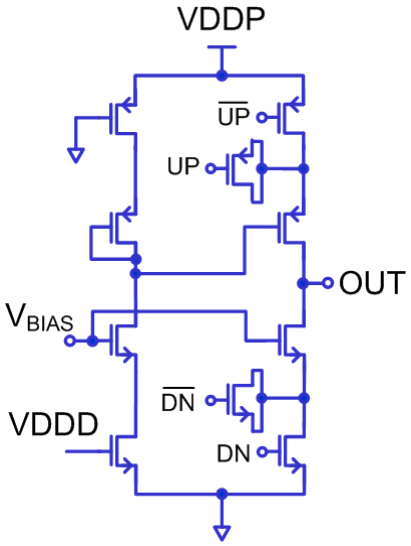


Figure 10: Charge pump schematic

The simulation result of the charge pump phase-detector presented on Figure 11 shows that the dead zone is eliminated and a phase difference (systematic offset) of -2.5 degree exists between reference and feedback clock.

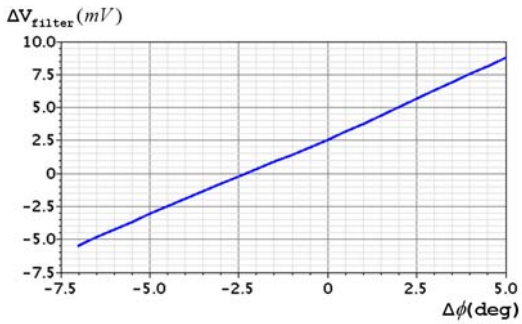


Figure 11: Simulation of charge pump phase-detector

The voltage controlled oscillator

The PLL uses a 4 stage differential ring oscillator for the VCO. The design of the VCO was optimized for low noise, low common-mode sensitivity and low power dissipation.
The delay cell, shown in Figure 12 (a), contains a source coupled pair with resistive load elements called symmetric loads. Their I-V characteristics are symmetric around the centre of the voltage swing. Linear controllable resistor loads are desirable to achieve supply noise rejection in differential delay cell because the common-mode noise is converted into differential-mode noise by the non-linearity of the load. The differential-mode would affect the cell delay and then produce timing jitter. By using symmetric loads, the first order noise coupling terms are cancelled out, and then reducing the jitter caused by the common-node noise present in the supply line. The cell delay changes with the VBIAS since the effective resistance of the load elements vary as the VBIAS. With the power supply VDDV as the upper swing limit, the lower swing limit is symmetrically opposite to the VBIAS. The VBIAS is generated dynamically by a replica bias circuit depicted in Figure 12 (b). A controllable tail current in the delay cells and the bias circuit is used to adjust the cell delay. The output voltage swing is relatively maintained constant by varying the active resistance of the loads in such a manner that the variation is inversing to the observed current change. The voltage to

current converter is shown on Figure 12 (c). This circuit provides a first-order linear relationship between the oscillation frequency and the control voltage. An additional current in the converter make the tuning of the VCO more flexible.

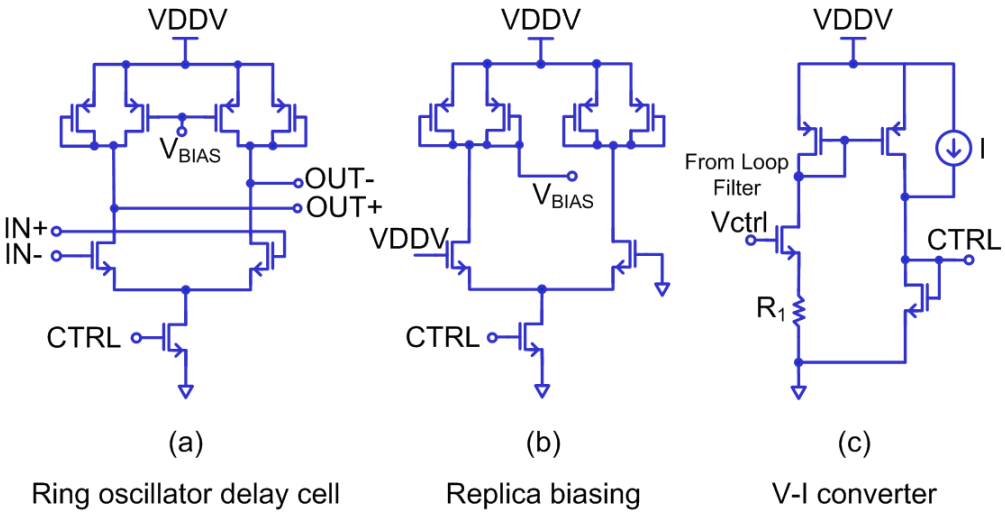


Figure 12: VCO topology

The level Shifter

In order to generate an output clock of 50% duty cycle, PLL is typically designed to operate at twice the desired frequency so as to be divided by two. This practice is particularly wasteful if the delay elements generate differential signals. Fig. 13 shows the level shifter including a differential-to-single converter.

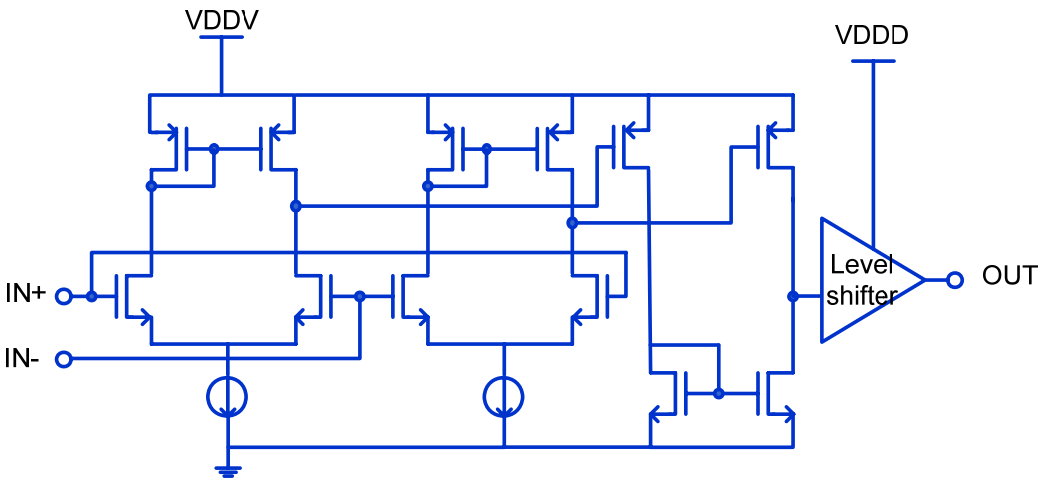
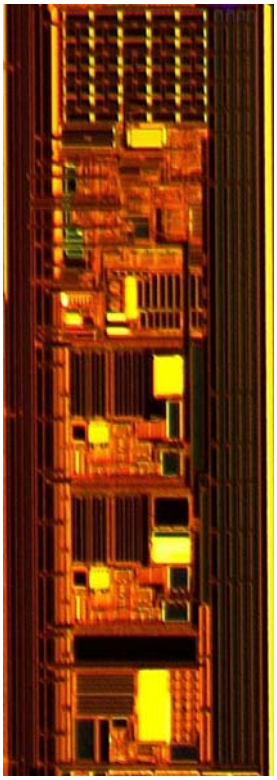


Fig. 13 differential-to-single converter and level shift

The differential-to-single converter is made up of two opposite phase NMOS differential amplifiers driving two PMOS common-source amplifier connected by a NMOS current mirror. Single end clock is generated at the output of the common-source amplifier. A clock buffer following the differential-to-single converter shifts the swing amplitude of VCO to digital-rails.

1-2- The preliminary measurement results of the MI22Ter PLL



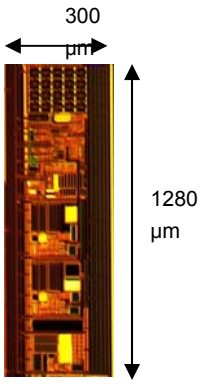
Preliminary measurement results of the MI22Ter PLL test structure

- FEATURES
- VCO FREQUENCY RANGE
- VCO CONTROL VOLTAGE
- JITTER PERFORMANCE
  - PERIOD JITTER PkPk (Pj) IN PERSISTENCE MODE
  - TOTAL JITTER (Tj) IN TIE MODE (BER=10^{-12})
  - TOTAL JITTER (Tj) IN TIE MODE (BER=10^{-12}) WITH NOISE MODULATED POWER SUPPLY
- POWER CONSUMPTION
- LOCKING TIME
- DUTY CYCLE RATIO
- CONCLUSION

Quan SUN, Kimmo JAASKELAINEN

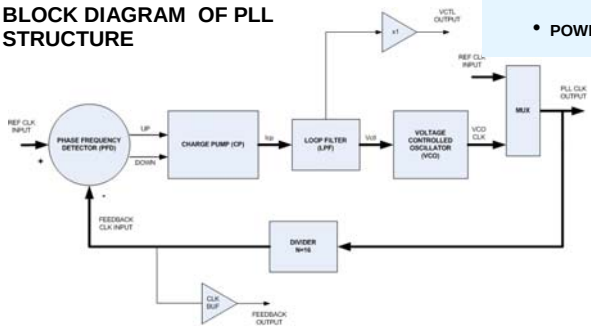
Preliminary measurement results of the PLL test structure of MI22Ter, Quan SUN, Kimmo JAASKELAINEN

FEATURES



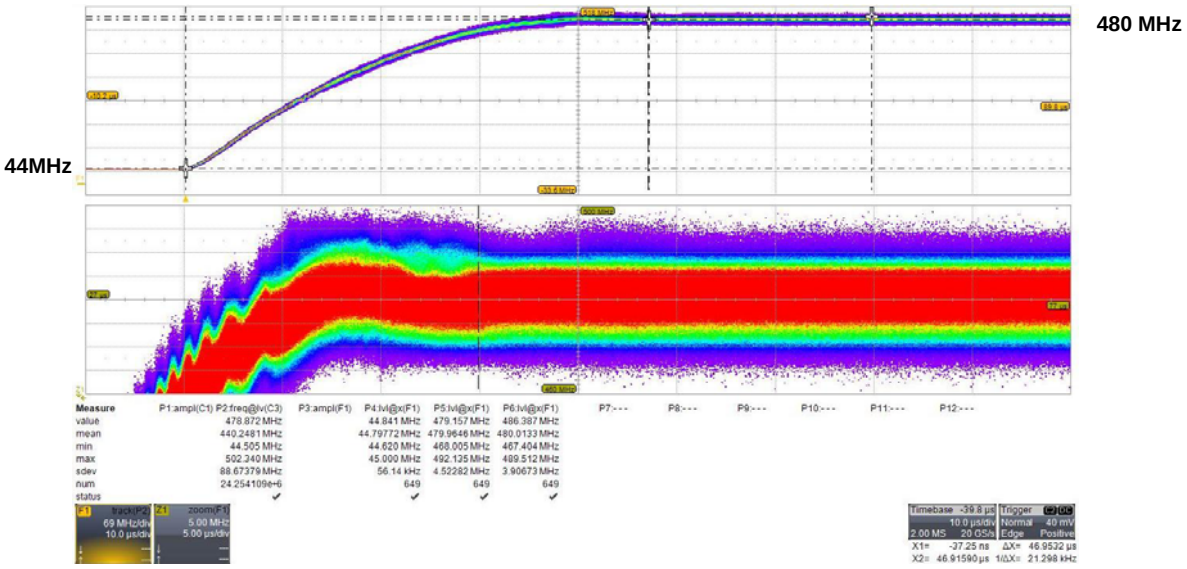
- CONSTANT MULTIPLYING CLOCK GENERATOR PLL
- MULTIPLICATION FACTOR: 16
- NATURAL FREQUENCY: 43.7 MHz at 20 °C
- LOCKING TIME (FROM 44MHz TO 480 MHz): 47 µs
- LOOP BANDWIDTH: 600 kHz (measured 400kHz)
- AMS CMOS 0.35 µm (AMS C35)
- PLL DIE AREA: 1280 x 300 μm^2 (0,384 mm^2)
- INTEGRATED VOLTAGE REGULATOR WITH 2 OUTPUTS: 2.5V, 3V
- POWER SUPPLY RANGE 3V - 3.6V, TESTED AT 3.3V
- POWER CONSUMPTION: 15 mW at 160 MHz (3.3V)

BLOCK DIAGRAM OF PLL STRUCTURE



VCO FREQUENCY RANGE

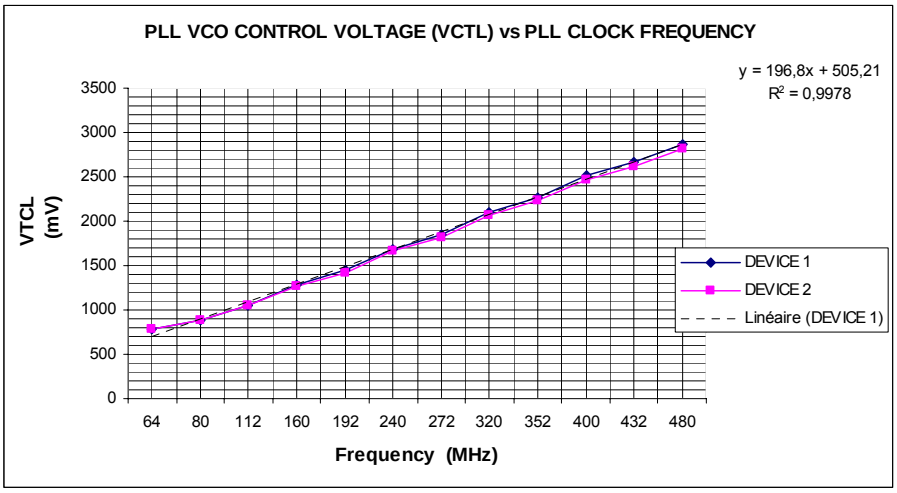
FREQUENCY RANGE: 44 MHz – 480 MHz



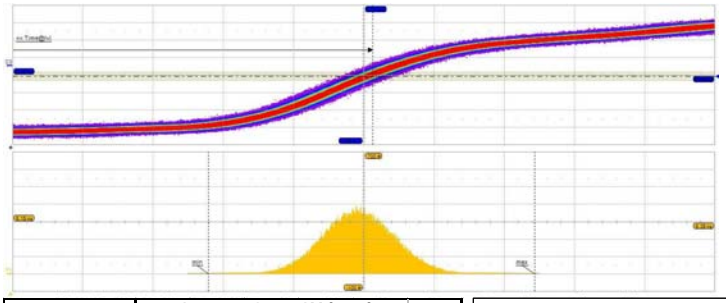
Preliminary measurement results of the PLL test structure of MI22Ter, Quan SUN, Kimmo JAASKELAINEN

VCO CONTROL VOLTAGE

There is no saturation of VCO output frequency

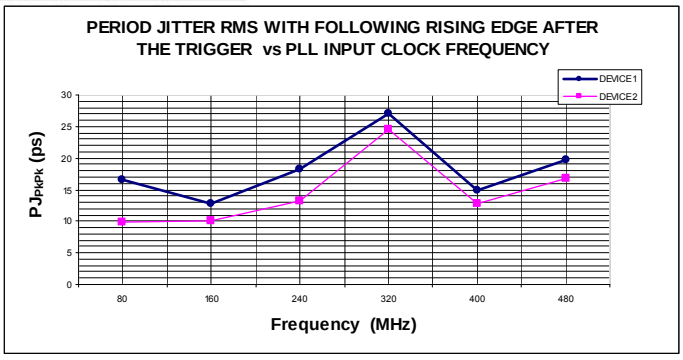


JITTER MEASUREMENT: PERIOD JITTER Peak-to-Peak (Pj_{pkpk}) IN PERSISTENCE MODE



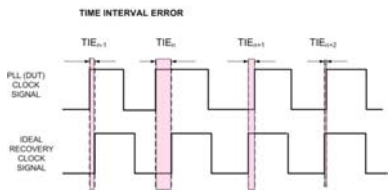
- A Classical way to measure jitter
- Dependent of number of samples acquired

	PLL CLK FREQUENCY (MHz)					
	5	10	15	20	25	30
DEVICE	80	160	240	320	400	480
N°1						
Pj pkpk(ps)	143	103	153,7	203	135	146
Pj rms (ps)	16,5	12,7	18,2	27,1	15	19,7
N°2						
Pj pkpk(ps)	87	93	112	172	87	106
Pj rms (ps)	9,9	10,1	13,2	24,5	12,8	16,7

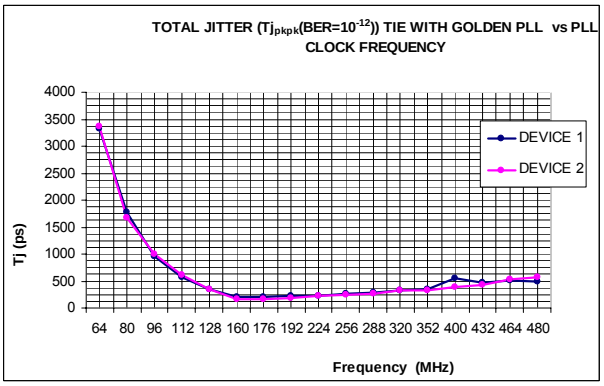


Preliminary measurement results of the PLL test structure of MI22Ter, Quan SUN, Kimmo JAASKELAINEN

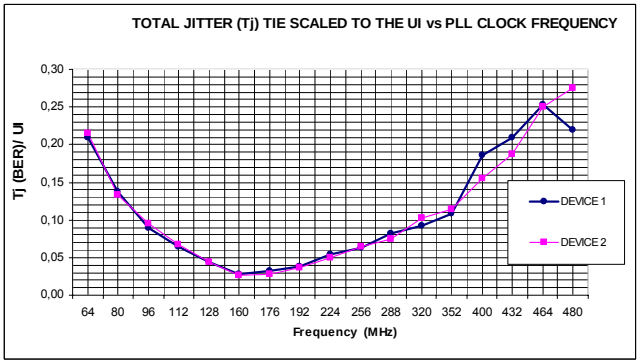
JITTER MEASUREMENT: TOTAL JITTER IN **TIE** MODE WITH BER = 10^{-12} (TJ(BER))



- TIE = Time Interval Error
- Extrapolation of Total Jitter (pk-pk) as a function of Bit Error Ratio(10^{-12}) in reasonable measurement time interval (10^6 samples)

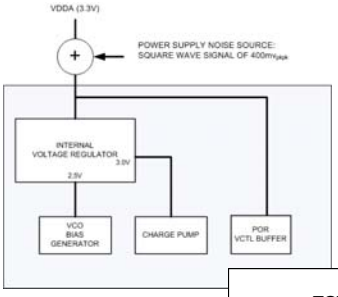


MI26 PLL
TJ_{pkpk} =3.78 ns @ 160 MHz

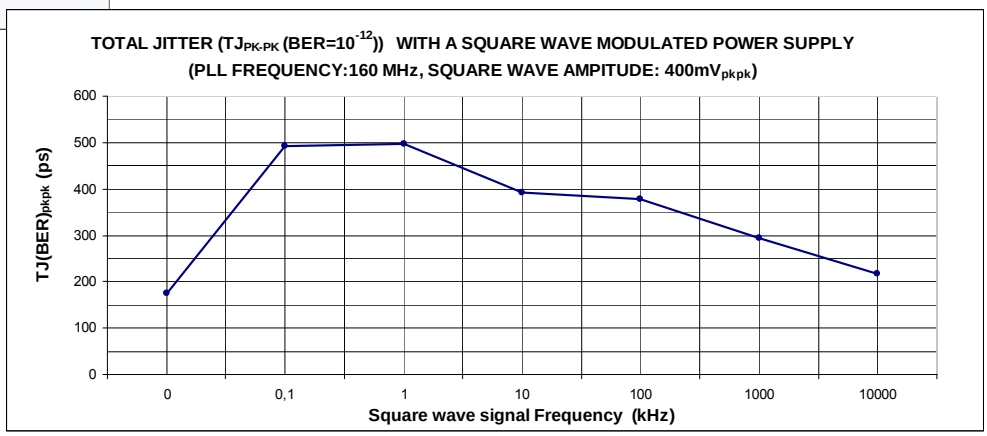


MI26 PLL
TJ_{pkpk} =0.6 UI @ 160 MHz

JITTER MEASUREMENT: TOTAL JITTER (Tj) TIE WITH BER=10^{-12} WITH NOISE MODULATED POWER SUPPLY

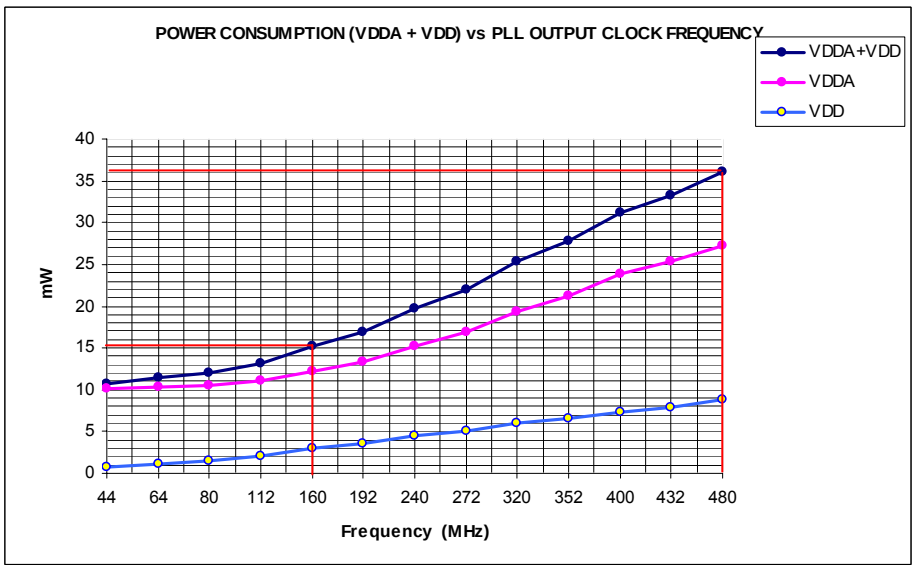


	SQUARE WAVE SIGNAL FREQUENCY (kHz)						
DEVICE	0	0,1	1	10	100	1000	10000
N°1							
Tj(BER10^{-12}) (ps)	174	493	497	392	379	294	217



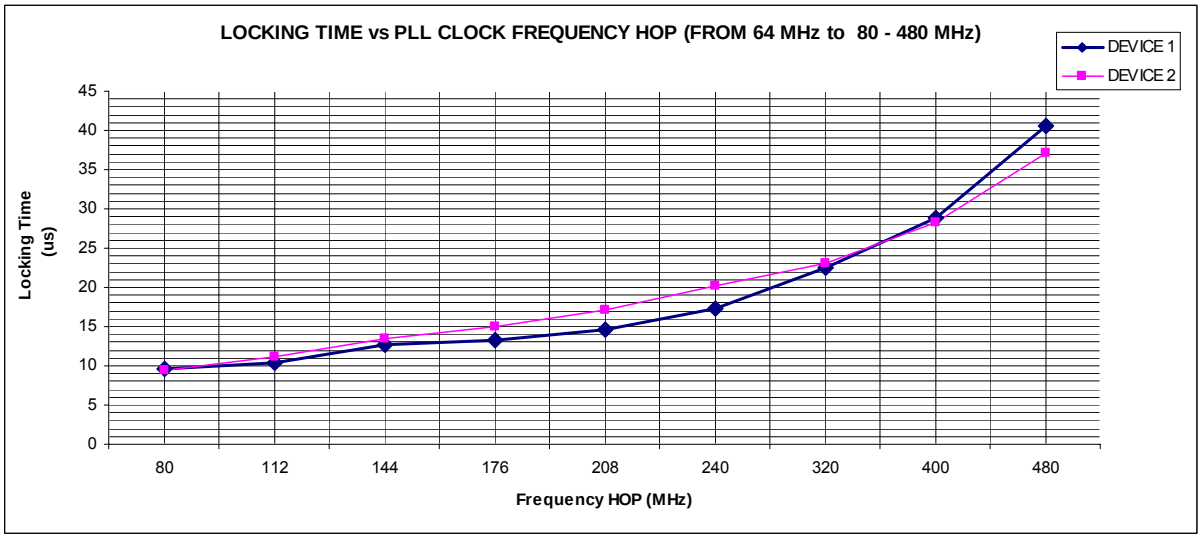
POWER CONSUMPTION vs. PLL INPUT CLOCK FREQUENCY

- Total Power Consumption without LVDS PAD: 15 mW @ 160 MHz
  37 mW @ 480 MHz
- Major part of digital power consumption is contributed by the output MUX



LOCKING TIME vs. FREQUENCY HOP

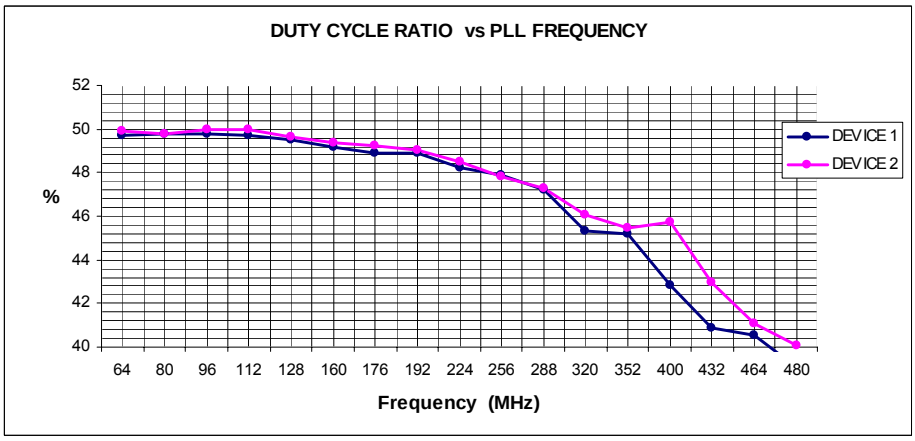
- Maximum Locking Time (44 MHz – 480 MHz): 47 µs



Preliminary measurement results of the PLL test structure of MI22Ter, Quan SUN, Kimmo JAASKELAINEN

DUTY CYCLE RATIO

- DUTY CYCLE RATIO: 49.2 % @ 160 MHz (pulse active time/total cycle time)
  39,2 % @ 480 MHz



Conclusion

These results are preliminary! (2 tested devices only).

The PLL performances have been improved significantly compared to the MIMOSA-26 PLL.

DEVICE	**TJ_{pk-pk} (BER=10^{-12}) at 160 MHz**	**Locking range**
MI-26 PLL	3.78 ns	137 MHz - 297 MHz
MI-22Ter PLL	170 ps (20x)	44 MHz – 480 MHz

2- The voltage regulator Jia Wang

1. Introduction

The vdda_regulator is designed for supplying analogue power voltage (3 V) from external voltage (3.3 V). This circuit is composed of two parts named TOP_REFC_LDO and TOP_LDO2. TOP_REFC_LDO contains reference current, bandgap and LDO1. TOP_LDO2 only contains the LDO2. The two LDOs are same. They share the reference current and bandgap. However, have different enable signals. The goal of dividing the LDO into two is to decrease the IR drop induced by the limited power supply width. In addition, this can also be the redundancy design.

The load currents are proximately 1.6 mA, 110 mA and 170 mA when the sensor works in different states. The load capacitor is about 200 nF because of the parasitic.

2. Pad description

	Name	Type	I/O	Function Description
TOP_REFC_LDO	en_bandgap	Digital enable signal	I	Enable/disable the bandgap(BG05A) and the reference current. 0: disable (**default**) 1:enable (connected to 3.3 V for test)
	dis_vdda1	Digital enable signal	I	Enable/disable the LDO1 0: enable (connected to 0V for test) 1: disable (**default**)
	vdd_reg	Power supply	IO	External power supply (3.3 V)
	vdd_reg			
	vdd_reg			
	vdd_reg			
	vss	Power supply	IO	External power supply (0 V)
	VBG	Test PAD	IO	Test and measure the output voltage of the bandgap. (Provide the external reference if the bandgap isn't good. Typical value:1.21 V)
	VB_REG	Test PAD	IO	Test and measure the output voltage of the reference current. (Provide the external reference if the reference current isn't good. Typical value: 1.98 V)
	Reg_vdda	Output of the vdda_regulator	O	The output voltage of the vdda_regulator, which is the analog power voltage in future. Its value designed is 3 V. The output voltages of the two LDOs are connected on board level.
	Reg_vdda			
	Reg_vdda			
	Reg_vdda			
TOP_LDO2	vdd_reg	Power supply	IO	External power supply (3.3 V)
	vdd_reg			
	vdd_reg			
	vdd_reg			
	vss	Power supply	IO	External power supply (0V)
	dis_vdda2	Digital enable signal	I	Enable/disable the LDO2 0: enable (connected to 0V for test) 1: disable (**default**)
	Reg_vdda	Output of the vdda_regulator	O	The output voltage of the vdda_regulator, which is the analog power voltage in future. Its value designed is 3 V. The output voltages of the two LDOs are connected on board level.
	Reg_vdda			
	Reg_vdda			
	Reg_vdda			

3. Circuit schematic

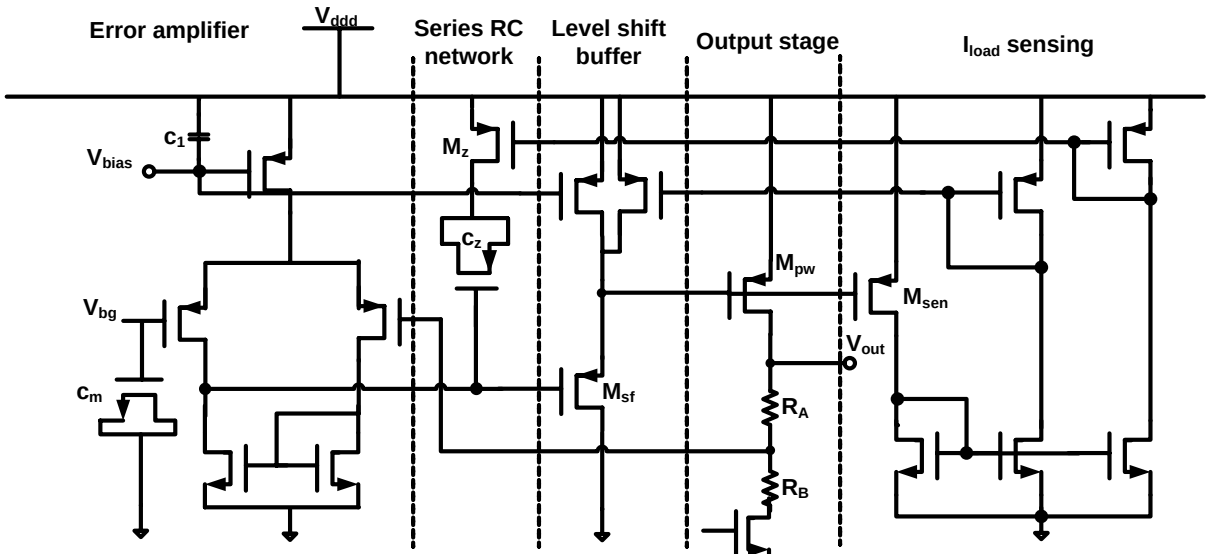


Figure.1 The schematic of the vdda_regulator

The compensation strategy is based on the pole-zero cancellation and buffer impedance attenuation. The locations of poles and zeros are adapted by feedback to maintain stability in the entire load current range. The compensation capacitor is significantly decreased.

The implementation of vdda_regulator is illustrated in Fig.1. It is composed of three stages. The first stage is a differential amplifier employing PMOS as input transistors for the PMOS transistors have less contribution to the flicker noise.

The second stage is a level shift buffer. It is realized as a source follower biased by two current sources. One current source is constant. The other current source is adaptive with load current by feedback. In addition, a series RC network is connected between power and the input transistor M_{sf}. The resistor is realized by a PMOS transistor biased by the sensing circuit of load current. Therefore, the resistance is also adaptive. In order to decrease the circuit area, the compensation capacitor is realized by PMOS transistor, instead of Poly-insulator-Poly capacitor or Metal-insulator-Metal capacitor.

The last stage is the same as that of the traditional LDO. However, the pass transistor successively works in subthreshold, saturation and linear regions when the load current varies from light to heavy. This configuration can save the power and chip area. Since the feedback resistors contribute to the thermal noise, small value feedback resistors are employed. The tradeoff between noise and power dissipation is considered to choose the proper resistor value. In this design, the values of R_A and R_B are 15KΩ and 10KΩ, respectively.

The sensing circuit of load current is realized by a simple current mirror. The transistor M_{sen} senses the drain current of the pass transistor M_{pw} and then the current is mirrored to the variable resistor and bias current.

4. Simulation results

4.1 Load regulation

The output voltage of one LDO is simulated when load current is swept from 0 to 0.2 A. The process corner is nominal and the temperature is 27 °C.
→The error voltage is 17.5 mV as shown in figure 2.

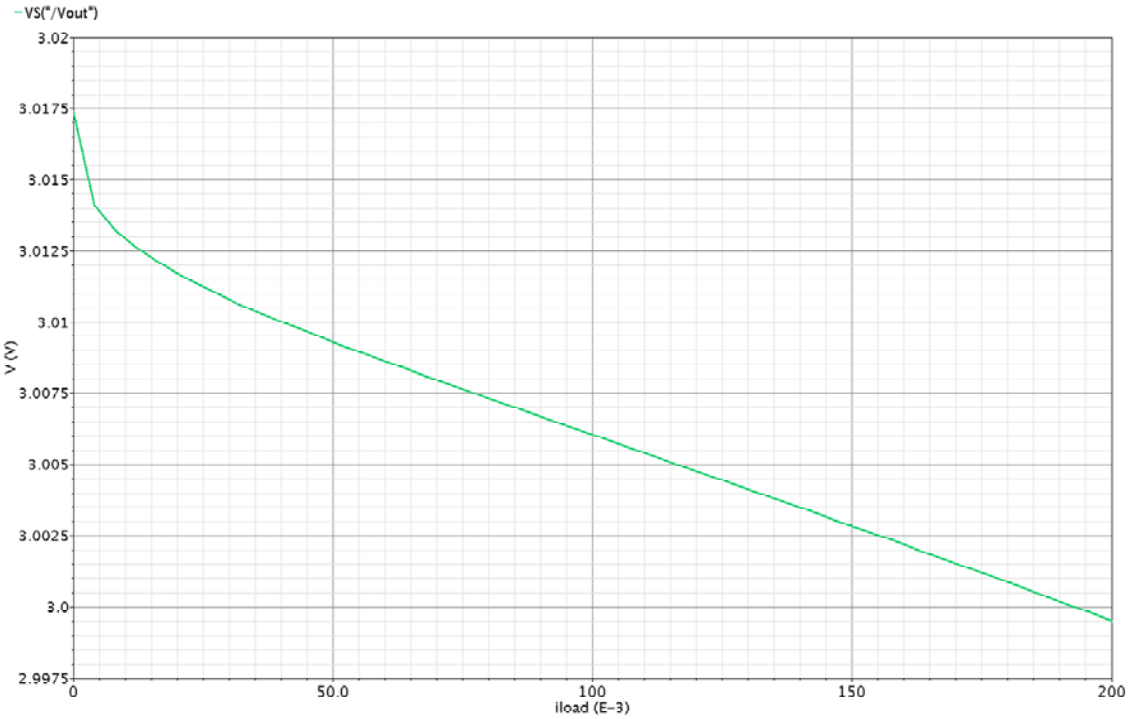


Figure 2. The output voltage versus load current

Monte Carlo: iteration=400, considering both of the Process and Mismatch.
→The average value is 2.998 V, when the load current is 0.2 A.

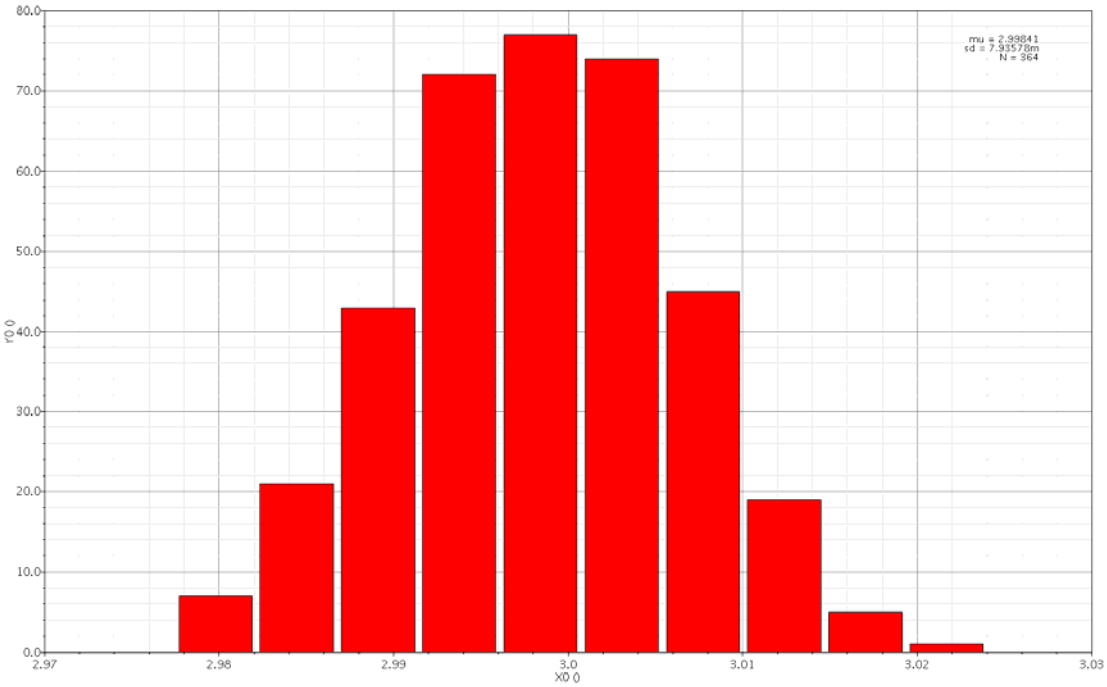


Figure 3 The monte carlo results of the output voltage at load current of 0.2 A.

4.2 Phase Margin

Phase margin is simulated when load capacitor and load current are swept in different processes. The results are shown in figure 4-6. Figure 7 gives the phase margin at the full range of load current when the load capacitor is 200 nF.

- Process: nominal, Temperature: 27°C, C_{load}: 100 nF (red), 200 nF (blue), 300 nF (pink), i_{load}: 0A, 1.6 mA, 110 mA, 170 mA, 200 mA

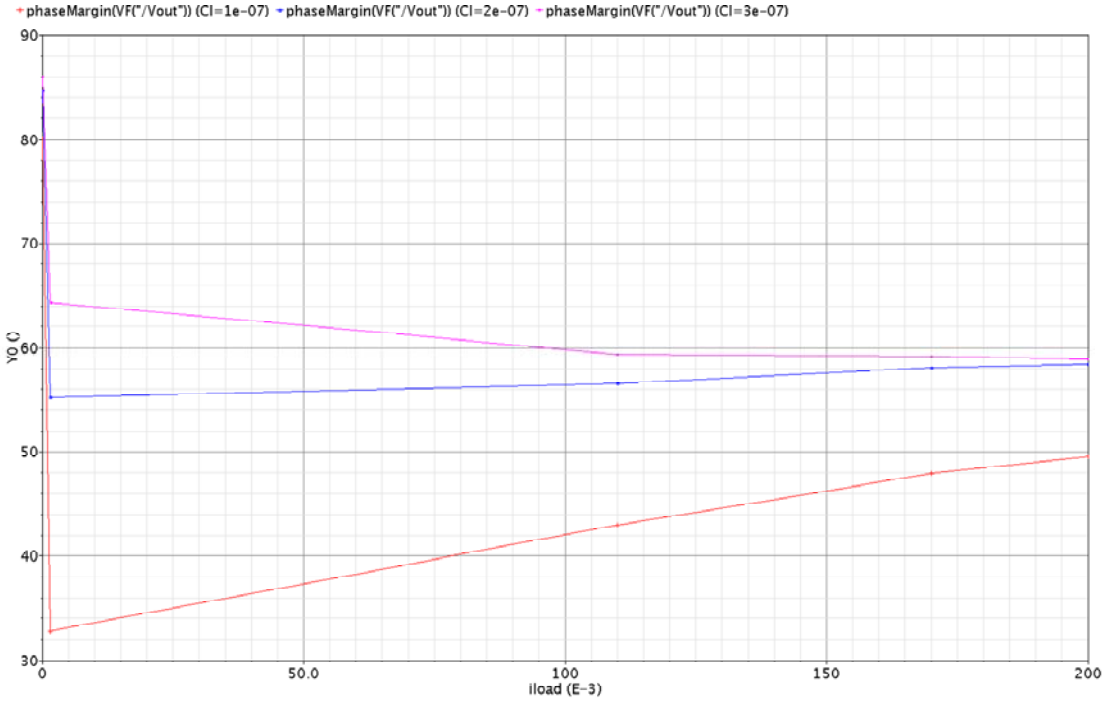


Figure 4. The phase margin simulated (Y0) in the nominal process.

- Process: wp, Temperature: 0°C, C_{load}: 100 nF (red), 200 nF (blue), 300 nF (pink), i_{load}: 0A, 1.6 mA, 110 mA, 170 mA, 200 mA (The LDO works in wrong state when the load current is 0 so the results doesn't appear.)

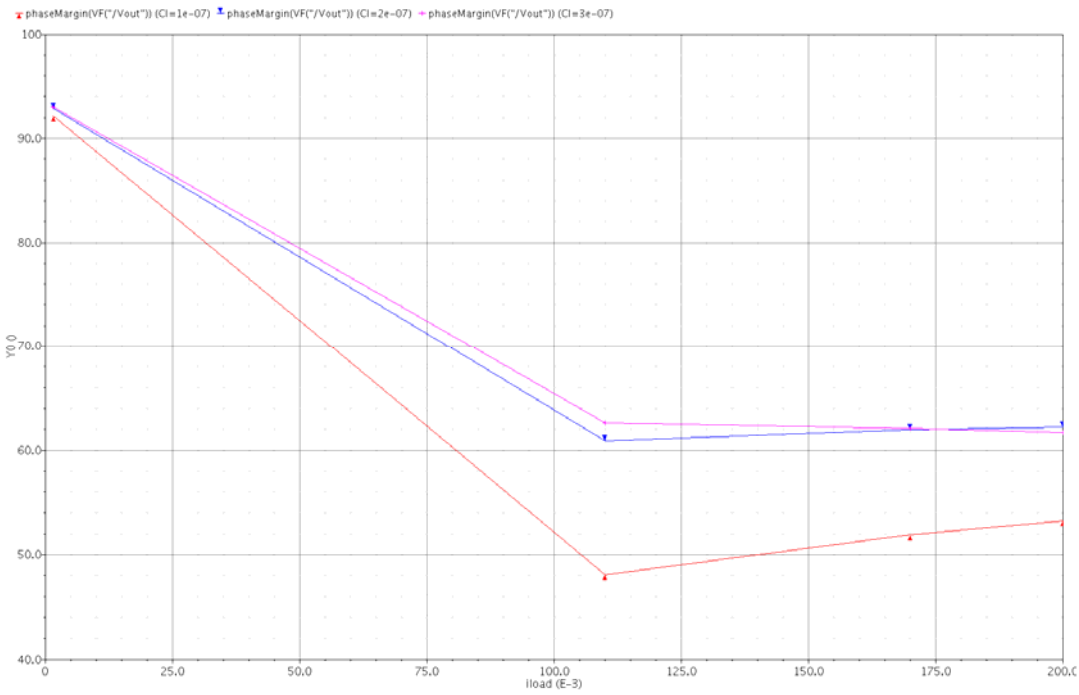


Figure 5. The phase margin simulated (Y0) in the wp process.

- Process: ws, Temperature: 40°C, C_{load}: 100 nF (red), 200 nF (blue), 300 nF (pink), i_{load}: 0A, 1.6 mA, 110 mA, 170 mA, 200 mA

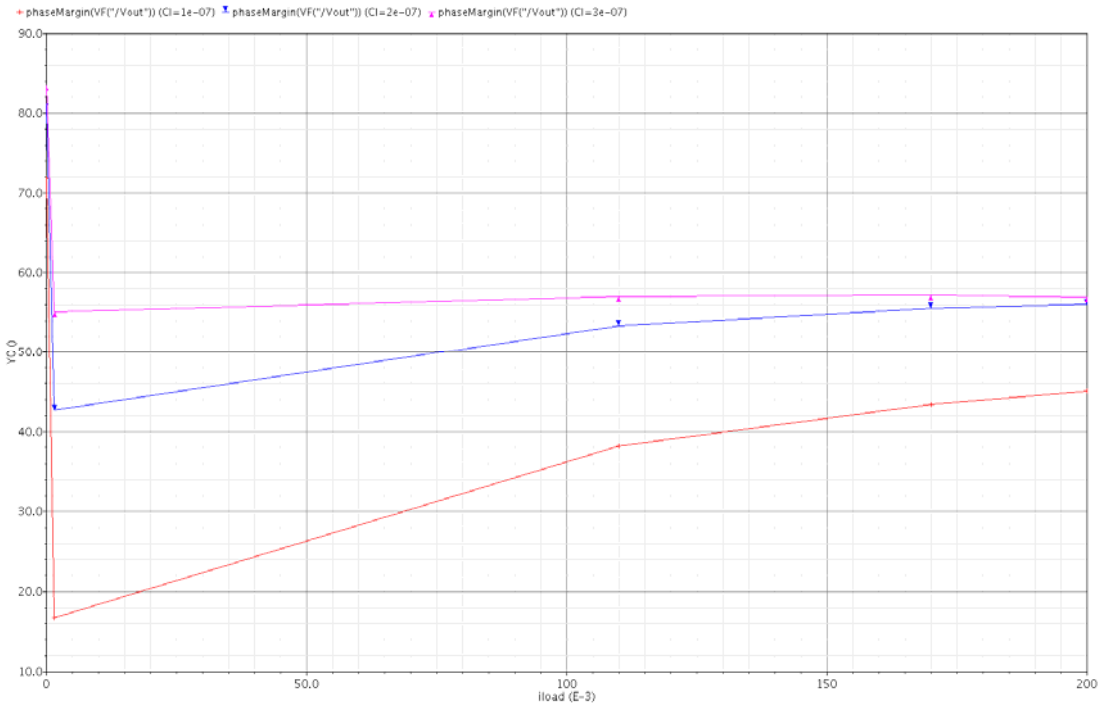


Figure 6. The phase margin simulated (Y0) in the ws process.

➢ Process: nominal, Temperature: 27°C, C_{load}: 200 nF, i_{load}: 0A ~ 200 mA (step size: 0.2mA)

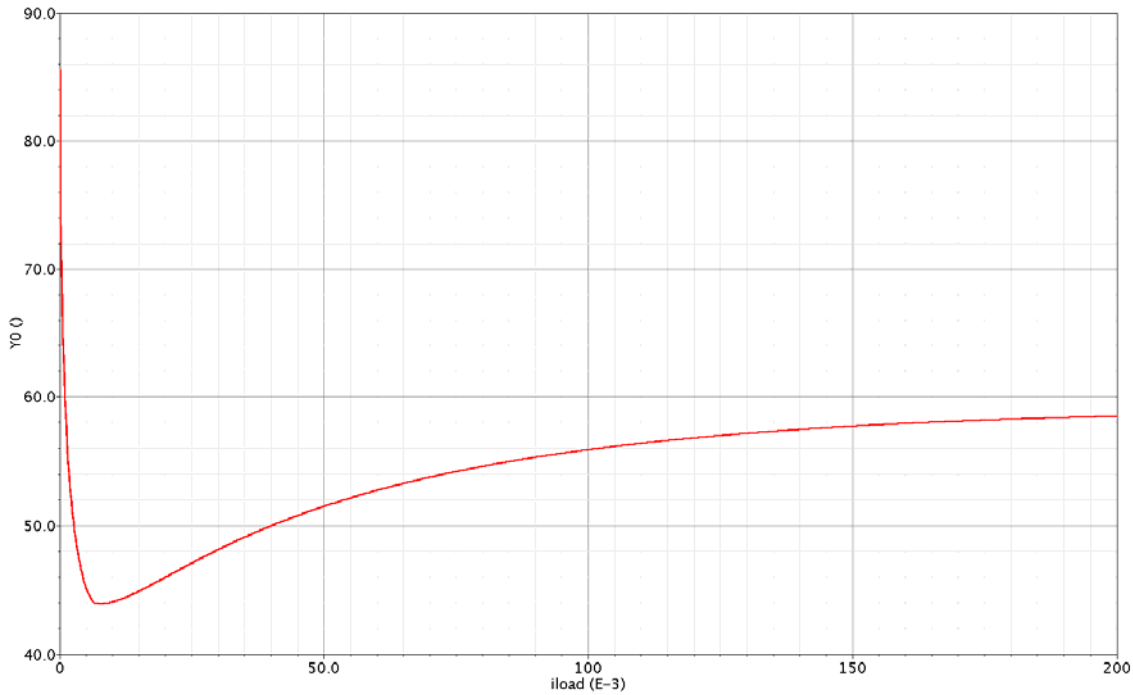


Figure 7. The phase margin (Y0) at the full range of load current in the nominal process.

We can conclude these simulation results as follows. The phase margin is larger than 45° in the full range of the load current when the process is nominal, the load capacitance is 200 nF and the temperature is 27°C. It is still larger than 42° when the load capacitors are 200 nF and 300 nF. But the phase margin is very small when the load capacitor is 100 nF and the load current is 1.6 mA.

The minimum phase margin occurs when the load current is 1.6 mA. The reason is that the gate capacitor of the pass transistor significantly increases due to its saturation state but the feedback current isn't large enough to push the pole at the gate far away from the unit-gain bandwidth.

Moreover, the LDO doesn't work in right state when there is no load current and the process is wp. The threshold current is large so the output voltage rises.

4.3 PSRR (Power Supply Reject Ratio)

PSRR is simulated when load capacitor and load current are swept in different processes. The results are shown in figure 8-10.

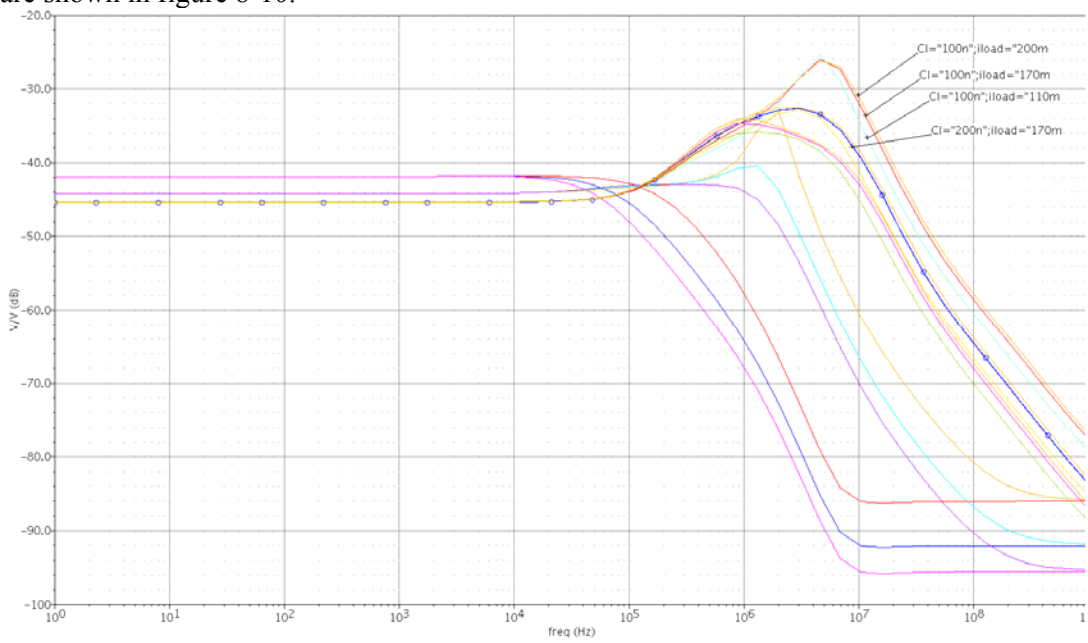


Figure 8. The PSRR in the nominal process and the temperature is 27°.

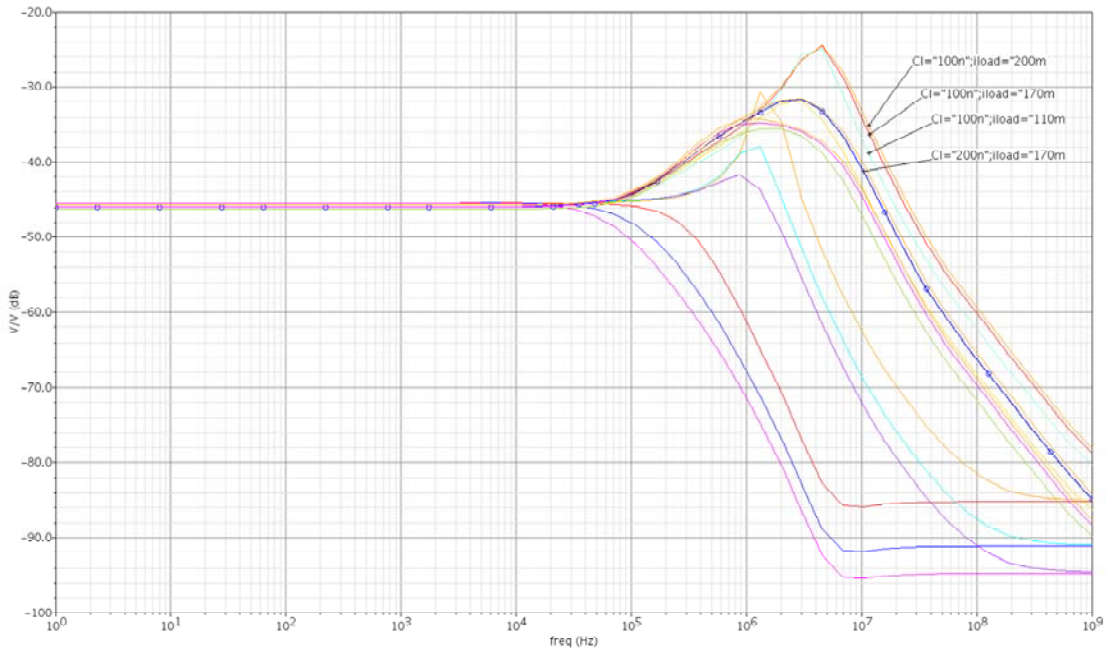


Figure 9. The PSRR in the ws process and the temperature is 40°.

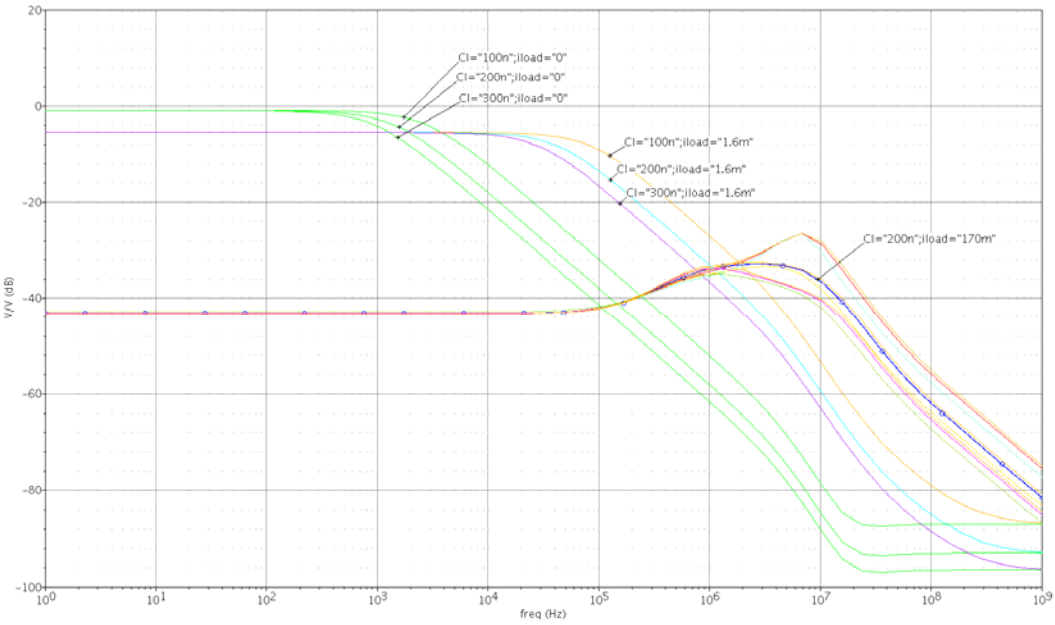


Figure 10. The PSRR in the wp process and the temperature is 0°.

We can conclude from the simulation results. The PSRR is lower than -40dB in most conditions. The PSRR is lower than -36 dB in the typical working state (Cl=200 nF, iload=170 mA and Frequency=5 MHz).

The PSRR is near 0 dB, when the iload is 0 A and 1.6 mA, corner is wp and temperature is 40° or 27°. The reason is:

- The input transistor of the operational amplifier will not work in saturator region.
- The pass transistor works in threshold region and its threshold voltage is lower when the corner is wp and temperature is higher. The gain is very low in this case.

4.4 Noise analysis

The equivalent output noise is simulated when load capacitor and load current are swept in different processes. The results are shown in figure 11-12.

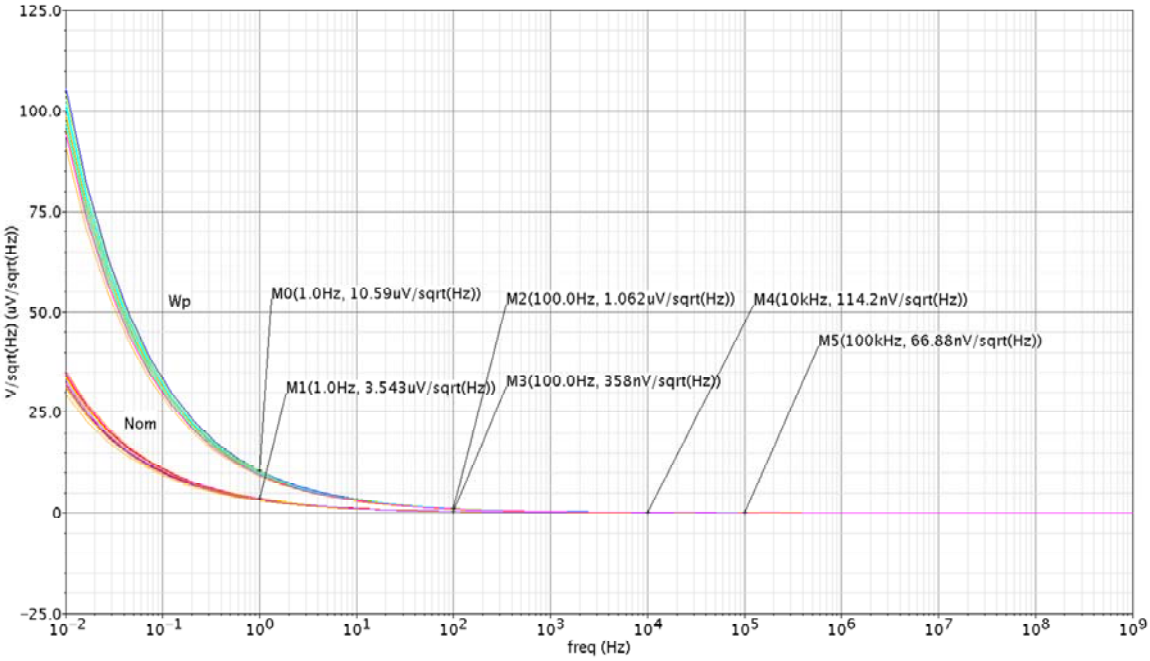


Figure 11. The equivalent output noise in the nominal (bottom) and wp (top) process and the temperatures are 27° and 0°, respectively.

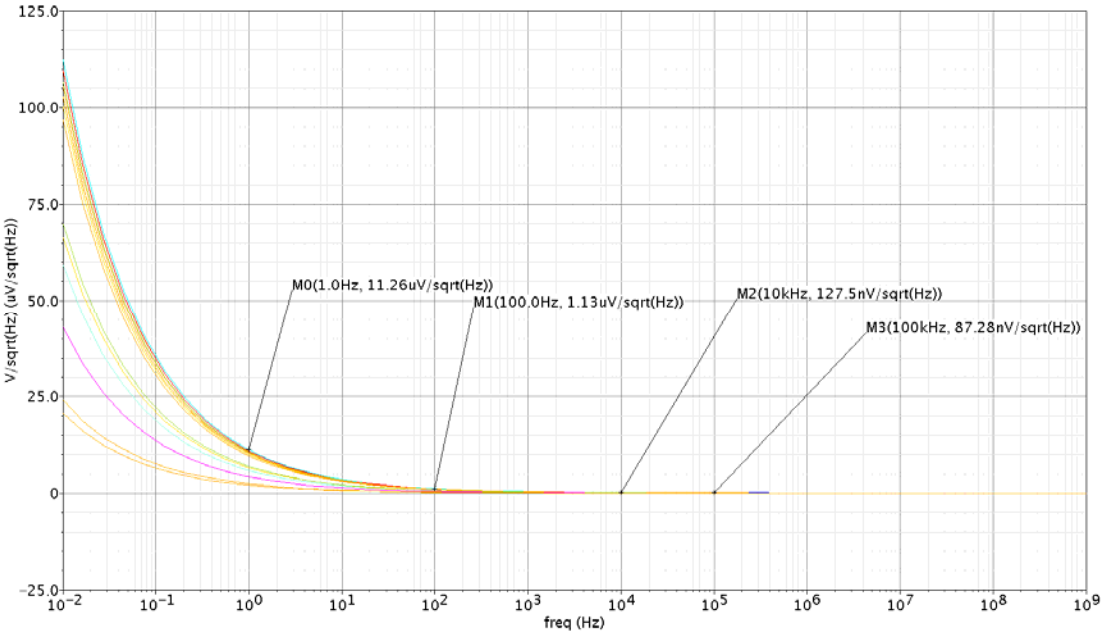


Figure 12. The equivalent output noise in the ws process and the temperature is 40°.

We can conclude from the simulation results. The noise is lower than 35 µV/sqrt(Hz) in the nominal process. It rises to 100 µv/sqrt(Hz) in the wp and ws process. However, the noise drops lower than 128nV/sqrt(Hz) when the frequency is higher than 10 kHz. The noise mostly comes from the operational amplifier. (The flicker noise of its input transistors and the current mirror load. 80%)