Ultimate

II- Optimization of discriminator design

(Preliminary version)

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Introduction

The original architecture of the discriminator was designed and validated in the small prototype MIMOSA-16 fabricated in AMS 0.35 µm process by our collaborators at CEA IRFU-SACLAY[1]. The measurement results showed that a resolution of ~ 1 mV can be achieved at a clock frequency of 40 MHz (5 MHz operating frequency).

The discriminator architecture is based on pre-amplifying stages followed by a latch and it is adapted to readout the active pixels. It is challenging to reach a few hundreds µV sensitivity for the comparator at high readout speeds. The signal of the pixel must be amplified before the comparator. This can be accomplished at column level or/and in the pixel. Closed-loop amplification with auto-zeroing allows at column level reducing gain mismatches. The number of amplifying stages is chosen as a function of the requested resolution.

Afterwards, the discriminator has been implemented in the successive MAPS prototypes.

In 2008, PHASE-1 was the first full scale sensor (~ 4 cm^2) consisting of 640 column-level discriminators working at low readout speed (1 MHz operating frequency). The test results showed threshold dispersion as a function of the discriminator position in the row. This dispersion has been studied and reproduced in the simulation. It can be explained by the effects due to the length of the row (~ 2 cm) which modify the ideal timing diagram of the discriminator.

PHASE-2 has been submitted at autumn 2009 to improve the PHASE-1 design with minimum modification (only 3 layout masks changed). The width of the transistor pair applying the clamping voltage has been reduced (w=6µ => 1µ) in order to minimize the threshold dispersion but the timing diagram was not corrected.

In 2008, MIMOSA-26 was designed for the EUDET beam telescope. MIMOSA-26 is a half reticle size sensor which includes 1152 discriminators (~ 2 cm long) working at the readout frequency of 5 MHz. As the readout frequency is higher than that of PHASE-1, it necessitates stable reference and clamping voltages during the sample periods. Therefore, the row of discriminators has been divided into 4 groups. Four bias DAC allow to compensate the process dispersion for each group. The timing diagram of the discriminator is the same as PHASE-1 chip. The test results showed that the ramp effect still appears on the threshold dispersion but it is limited at an acceptable level.

In April 2010, the MIMOSA-22AHR prototype has been submitted to validate the pixel design for Ultimate. In this circuit, a basic logic has been implemented to optimize the discriminator timing diagram.

Now, the Ultimate sensor has a readout frequency of 5 MHz (like MIMOSA-26). The discriminators row is divided into 4 groups of 240 discriminators each and the timing diagram is optimized to eliminate the systematic offset.

[1] Low-Power Autozeroed High-Speed Comparator for the Readout chain of a CMOS Monolithic Active Pixel Sensor Based Vertex Detector, Yavuz Degerli and al, IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL.50,N°.5,OCTOBER 2003

1- Principle

To perform the analog to digital conversion, we have integrated in the MAPS a column-based, low power, high precision discriminator to read out the active pixel. The "double sampling" technique is used at pixel and column levels to correct the offset. The figure 1-a presents the simplified schematic of a pixel with its local memory (moscap) enabling the individual pixel offset correction and the first stage in the column readout circuitry. The figure 1-b shows the timing scheme of the readout sequence.

- The difference between the present (after the integration time) and the previous values of the pixel (in the previous readout cycle) is the pixel signal, Vsig.
  This value (Vsig +Vclp) is sampled and stored on a capacitor at the column level (V_{RD}). It comprises the offset of the source follower in the pixel (SF) and the first stage in the column circuitry.
- The pixel reference level is stored on the in-pixel memory. By substracting it from the signal, the spatial noise (FPN) of the pixel is suppressed.
- The pixel clamping voltage Vclp is sampled and stored on a capacitor at a column level (V_{CALIB}). It comprises the offset of the SF and the first stage in the column circuitry.
- The useful signal is the difference between the two levels (V_{RD}-V_{CALIB}) free of the offset mismatches of the SF and of the first stage.

Note that the "double sampling" process doesn't suppress the temporal noise and the 1/f noise is only partially reduced. Other noise such as pixel gain non-uniformity is not reduced.

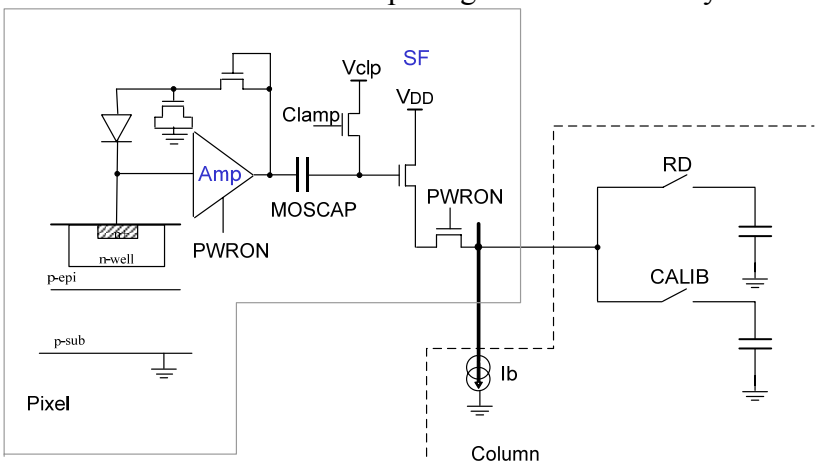


Figure 1-a: schematic of pixel and first stage in the column circuitry.

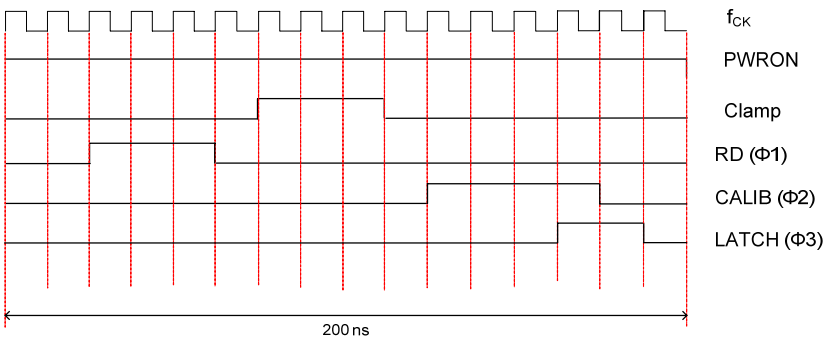


Figure 1-b: Readout sequence

The figure 1-c presents the architecture of the discriminator. It is based on a cascade of differential low-gain amplifiers followed by a dynamic latch. Auto-zero technique is used in every amplification stage of the read-out path. In this way, we can obtain a very high gain and compensate the offset.

The cascade of offset-compensated low-gain amplifiers increases the dynamic range and the bandwidth (reduced response time).

Due to its large bandwidth, the temporal noise of the discriminator is mostly white. So, the auto-zeroing process increases the noise power.

To overcome the issues related to substrate coupling in the mixed-signal environment, to improve the PSRR, and to reduce the effects of the charge injected by the switches used in the comparator, a fully differential architecture is chosen.

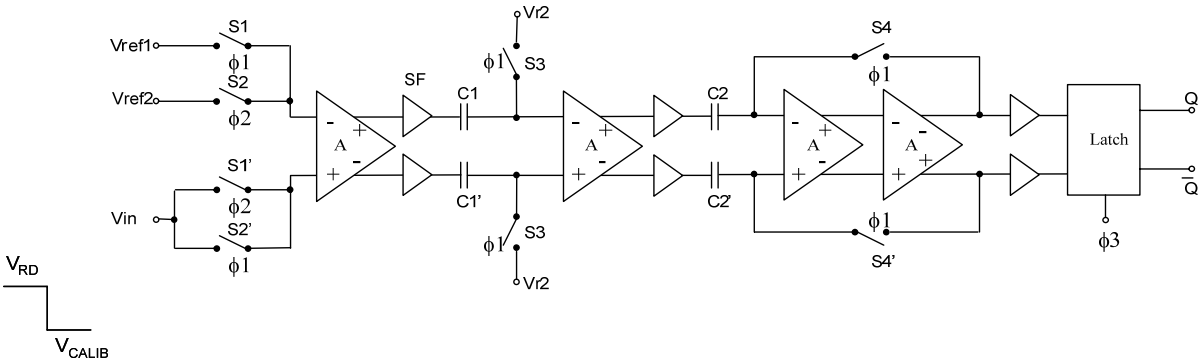


Figure 1-c: Offset compensated comparator architecture

The readout sequence of the pixel is as follow (Fig 1-b):

During the RD phase (Φ1):

- Sample the pixel signal V_{RD} and its offset voltage
- Sample the threshold voltage (VRef1)
- Sample the offset voltages of the other gain stages (both input offset and output offset storage)

During the CALIB phase (Φ2):

- Sample the pixel voltage after clamping V_{CALIB} and correct its offset
- Sample the common-mode voltage of the threshold voltage (VRef2)
- Amplify the signal (V_{RD}-V_{CALIB}) and the threshold level (VRef1-VRef2) and feed to the latch.

During the LATCH phase (Φ3):

- Compare the pixel signal (V_{RD}-V_{CALIB}) to the threshold level (VRef1-VRef2), then give a logic level

Detailed schematic of the discriminator:

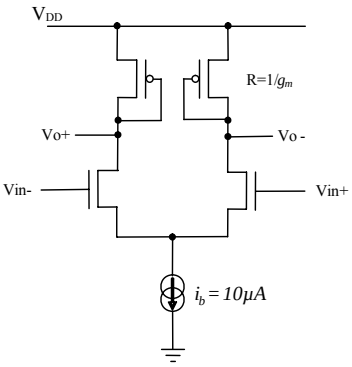


Figure 1-d: Amplifier stage

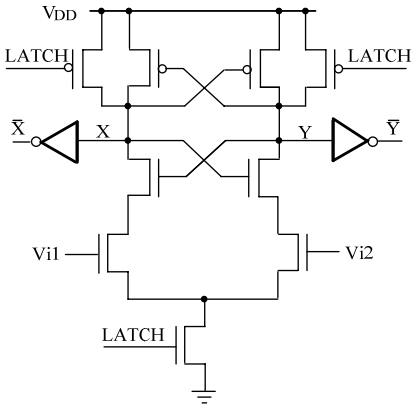


Figure 1-e: Latch

Amplifier stage

The amplifier stage is a simple differential gain stage with "resistive" loads (see fig. 1-d). The output common-mode voltage of this circuit is well defined and given by:

$$V_{CM}(out) = \frac{V_o^+ + V_o^-}{2} = V_{DD} - \frac{i_b R}{2}$$

This circuit gives a moderate gain of ~ 4 with a bias current of 10 µA. A gate length of 0.5 µm is used for the input transistors to reduce the offset voltage at the cost of a reduced speed. The two source follower buffers after amplifying stages are used to reduce kickback effects. A Monte-Carlo simulation gives a sigma of 4 mV for the input offset of the first stage (amplifier + SF). Note that the gain of this stage is non-linear and falls at high input signals levels (see fig 1-f). The transconductance of the input devices is maximum at the origin.

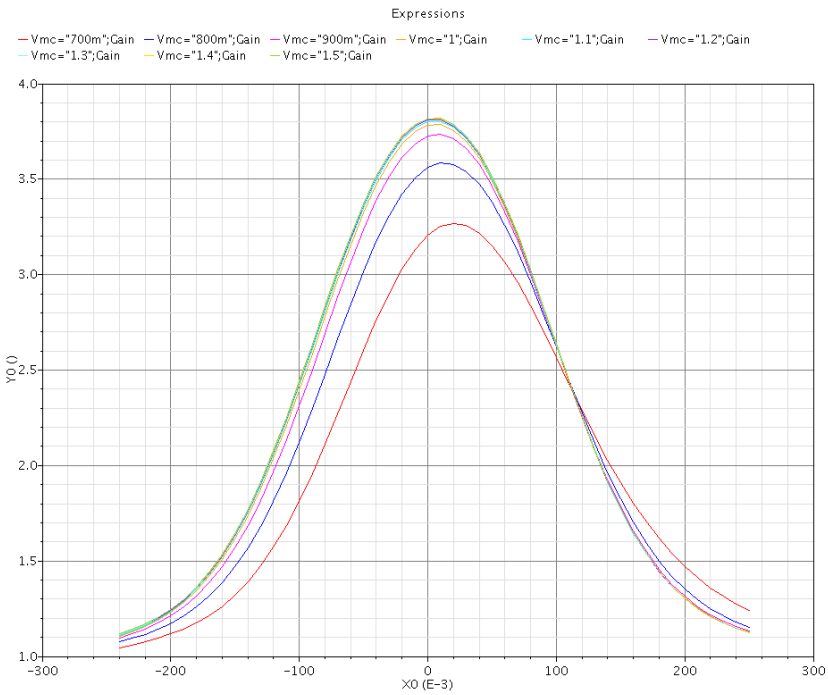


Figure 1-f: Gain of the first stage (amplifier +SF) as a function of the input signal level.

Latch

The architecture of the latch is presented on figure 1-e. This is a dynamic latch which offers good speed and no-static power dissipation. When the latch signal is low (resetting period), the lower NMOS transistors prevents the static current flow and the outputs are held at V_{DD}. Once the LATCH signal goes high, the transistors forming the two cross-coupled inverters immediately go into the active region. Because these transistors turn off, there is no static power dissipation once the latch outputs are fully developed. Two additional small inverters are used to balance the charges seen by the outputs of the latch. The switching time is in the order of 2 ns loaded by a flip-flop (FF).
It is difficult to compensate the offset of the latch because of the non-linear positive feedback but it is reduced by the gain of the amplifying stages.
The supply and ground voltages of the latch use dedicated lines and pads to alleviate the mixed-signal coupling.

Other characteristic

The static current consumption of the discriminator is 70 µA. To take into account the requirement of certain machine time cycle, the discriminator can be also set in an idle mode to reduce the power dissipation during the machine dead time. An optional power pulsing circuitry has been implemented to reduce the static current in the amplifying stages of a factor 100 (see figure 1-g). The bias voltages of the amplifier stages can be buffered if necessary.

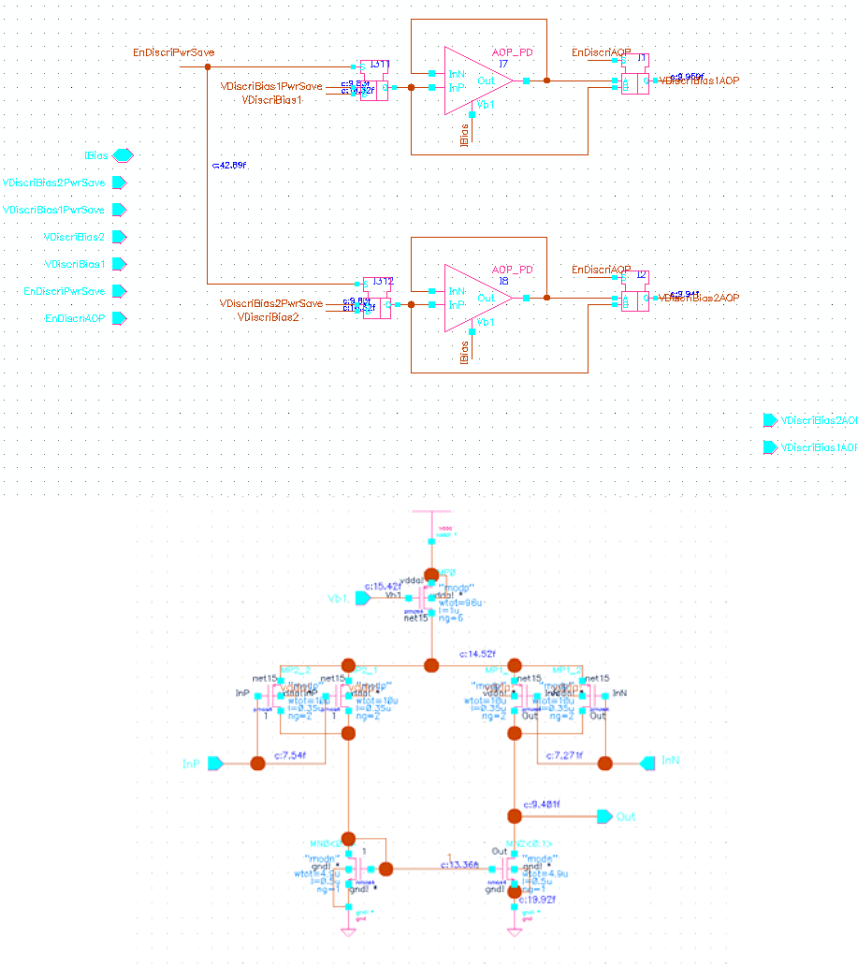
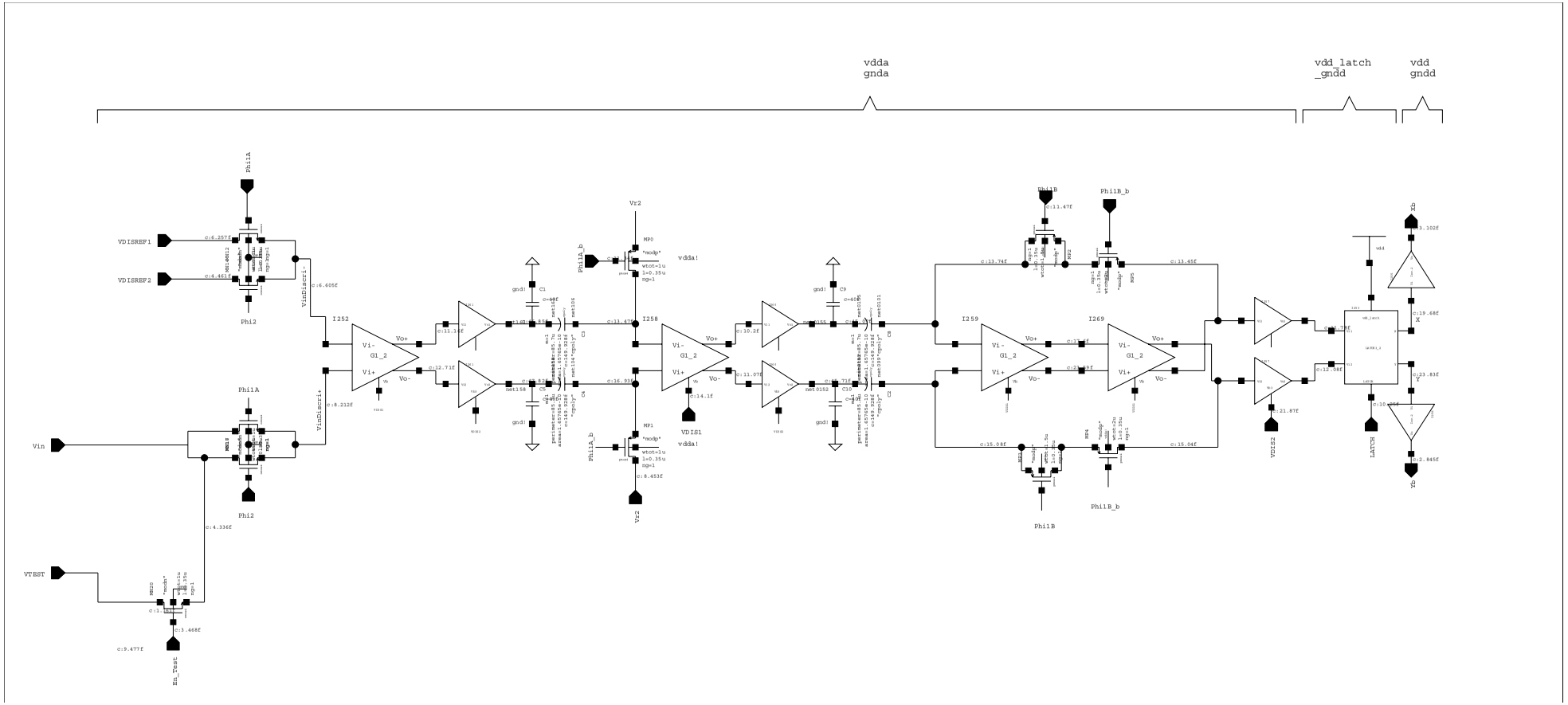
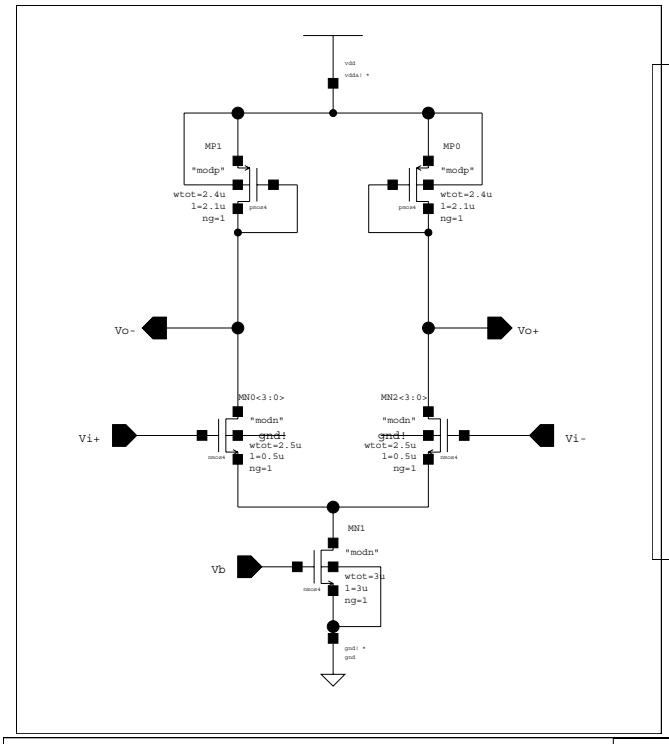


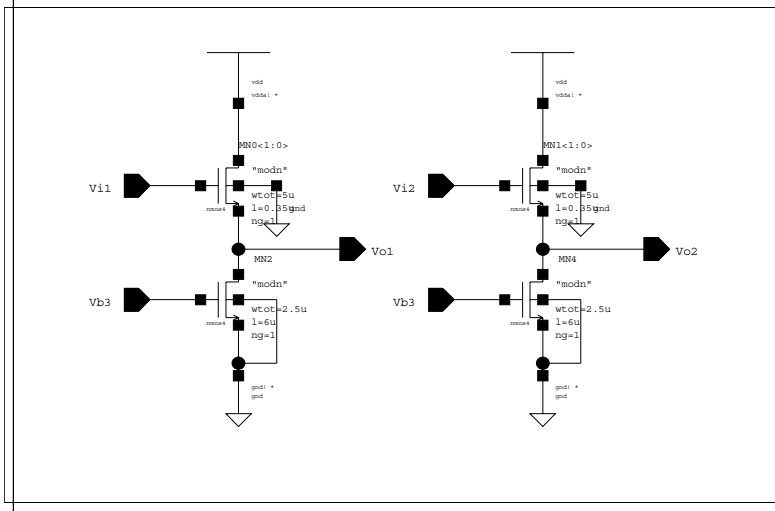
Figure 1-g: Power pulsing circuitry



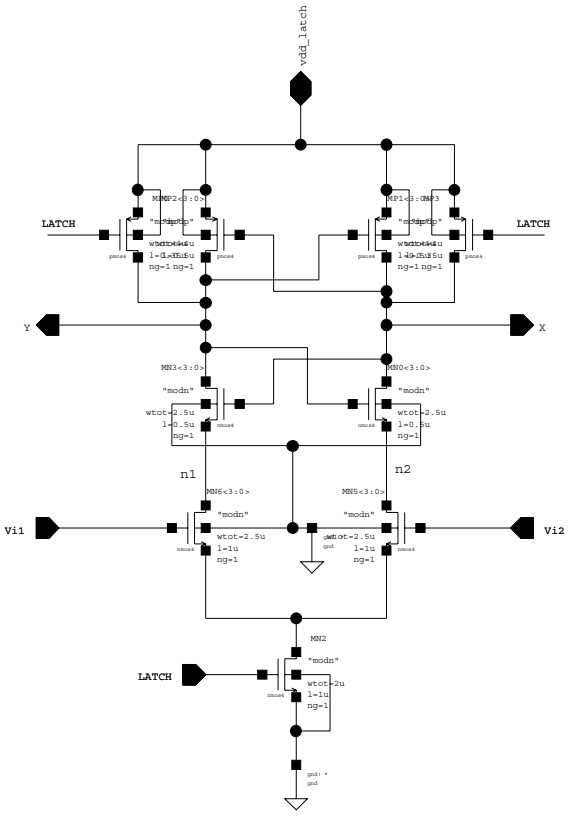
Schematic of the discriminator



Schematic of the amplifier



Schematic of the source followers



Schematic of the latch

2- Study of the scaling to a large size sensor

In the paragraph 2-1, we have studied the stabilization of reference and clamping voltages of the discriminator during the RD and CALIB periods when there are ~ 1000 discriminators (2 cm long) working at readout frequency of 5 MHz (200 ns/row). Like the MIMOSA-26 sensor, the discriminator row has been divided into 4 groups in the Ultimate sensor. 4 bias DACs allow to compensate the process dispersion for each group of discriminators.

2-1- Stabilization of reference and clamping voltages

In Ultimate, there are 960 discriminators at the bottom of the pixel array. During the RD phase, one Nmos transistor by discriminator is connected to the line VRef1 and during the CALIB phase, one Nmos transistor is connected to the line VRef2. The Vref1 and the VRef2 are applied successively at the same input of the discriminator. The clamping voltage at the discriminator level (noted Vr2 in the Figure 1-c) is applied at the intermediate differential inputs. The reference and clamping voltages are provided at the input of lines of near 2 cm long.

When the discriminators are connected to the analogue voltage, all transistors turn on at the same moment generating a voltage overshoot. This value will be greater near the source and it will take a certain time to retrieve the baseline. It is necessary to have stable signals during the active RD and CALIB periods (30 ns).

In order to have stable voltages, the row of discriminators has been segmented in 4 groups (see fig. 2-1-a). This point is less critical for the clamping voltage because of the differential structure of discriminator.

Like in the PHASE-1 and MIMOSA-26 sensors, the RC of the reference lines has also been reduced from the original discriminator layout by multiplying by a factor 2 the track width (2.5 µm). In this way, the resistance is divided by 2 but the capacitor is not multiplied by 2 ($C_{tot} = C_{area} + C_{peri}$).

To be able to drive the load capacitor, a buffer with low output impedance has been implemented at the input of the each reference line.

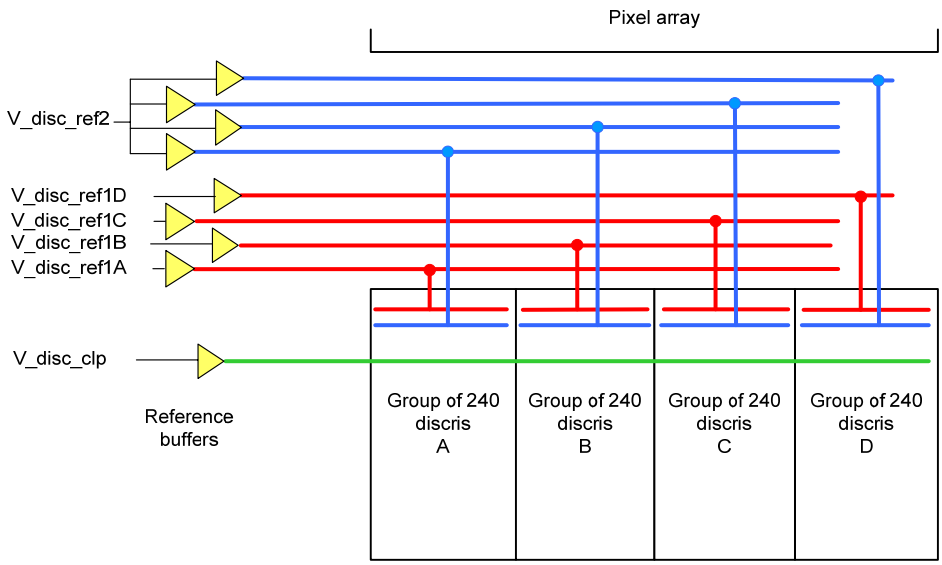


Figure 2-1-a: Floorplan of the reference and clamping voltages of the discriminator

2-2- Test results of the MIMOSA-26 sensor

The Table 2-2 shows the test results of the discriminators only (not connected to pixels) for the MIMOSA-26 sensor.

The temporal noise (TN) and the fixed pattern noise (FPN) have been also extracted from the transfer functions of the discriminators connected to the pixels. The figure 2-2-a and 2-2-b show the measurement results as a function of frequency for the MIMOSA26 sensor.

The measured temporal noise remains less than 900 µV and the FPN is less than 400 µV. Therefore, a resolution of about 1 mV can be reached at a clock frequency of 80 MHz (5 MHz pixel readout frequency).

The figure 2-2-c shows the threshold dispersion as a function of the discriminator position. One can see that there is still an effect of the ramp on the threshold dispersion.
This effect could be removed by optimizing the timing diagram (see following paragraph 2-3).

	TN (µV)		FPN (µV)		Offset (µV)	
Sub-array/ freq	20 MHz	80 MHz	20 MHz	80 MHz	20 MHz	80 MHz
A	396	422	93	140	211	-365
B	381	401	259	323	360	-291
C	372	398	581	723	766	372
D	376	404	442	535	1041	941

Table 2-2: Temporal Noise, Fixed Pattern Noise, Offset for the test of the discriminators only (pixel not connected)

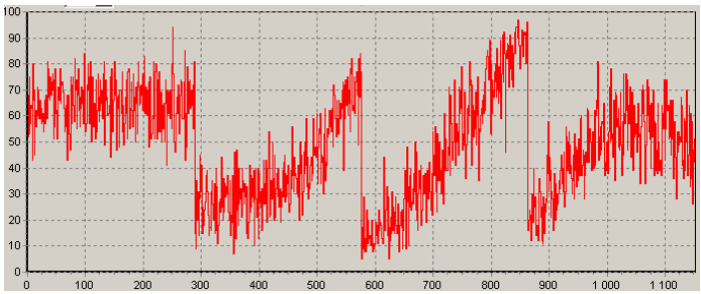


Figure 2-2-c: Threshold dispersion as a function of the discriminator position

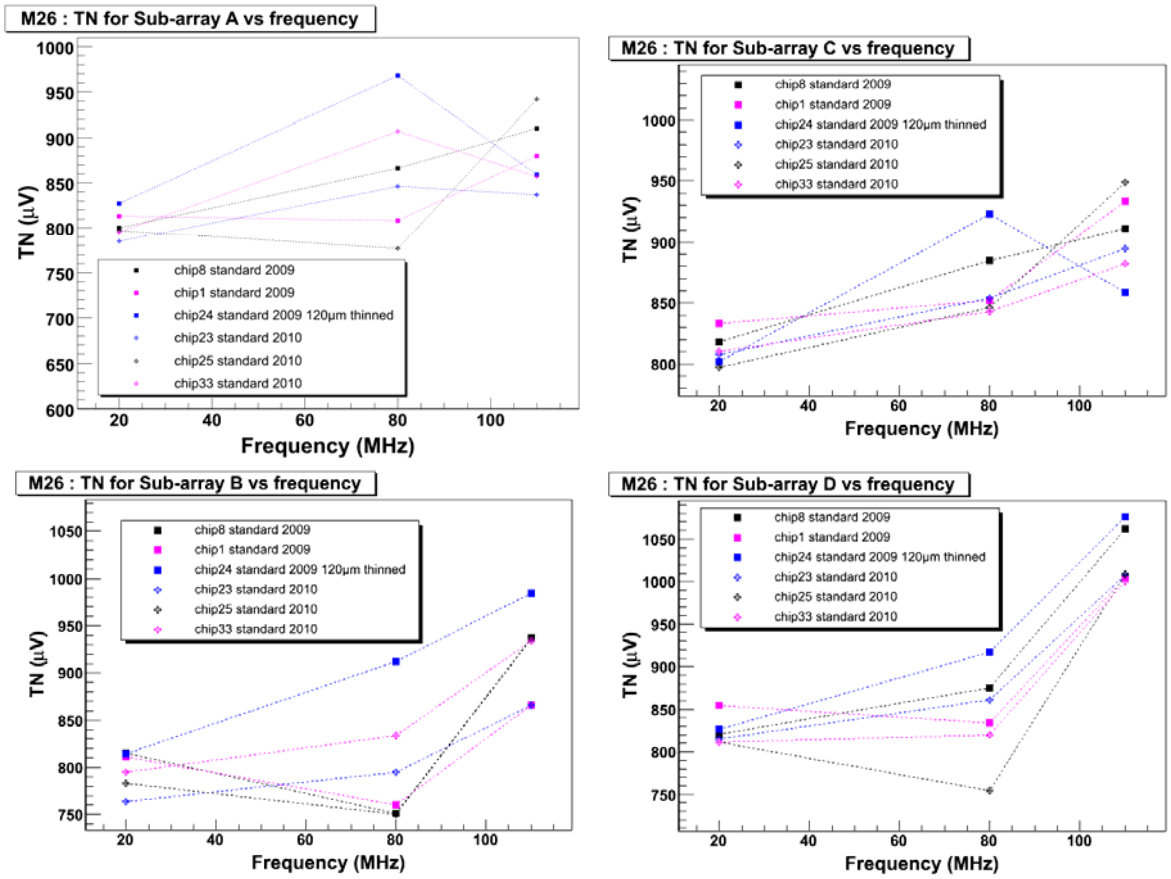


Figure 2-2-a: Temporal noise of the discriminators (connected to pixels) of MIMOSA26

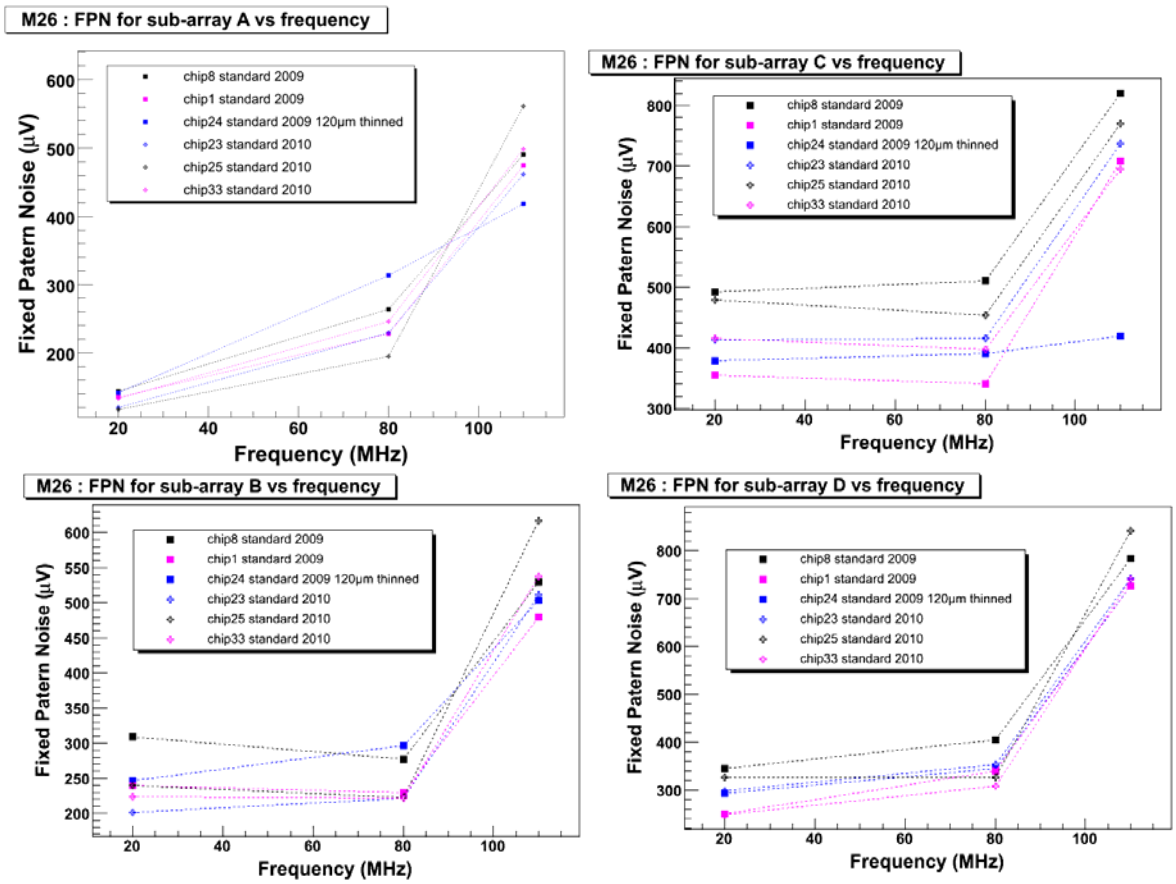


Figure 2-2-b: FPN of discriminators (connected to pixels) of MIMOSA26

2-3- Optimization of the discriminator timing diagram

In order to correct the offset dispersion, an optimization of the discriminator timing diagram is needed. In this paragraph, 6 possible cases are defined for the calculation of the discriminator offset.

Calculation of the input offset of the discriminator

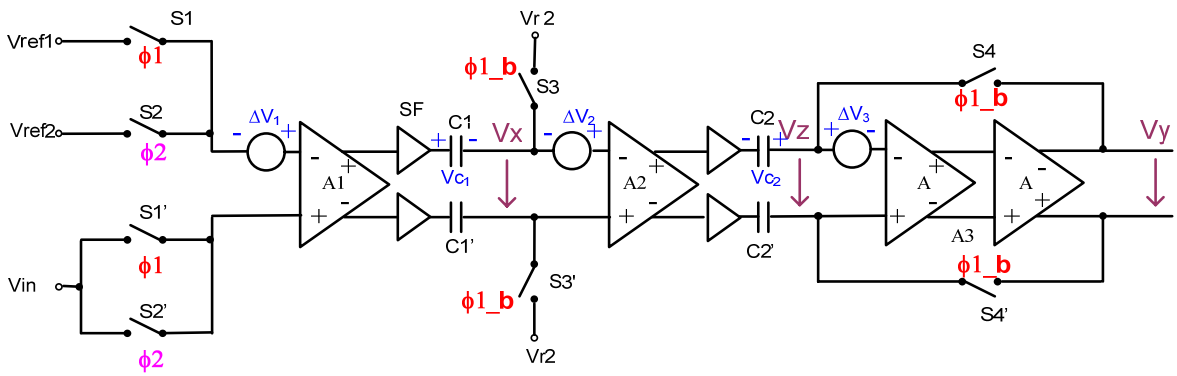


Figure 2-3-a: Diagram block of the amplifying stages

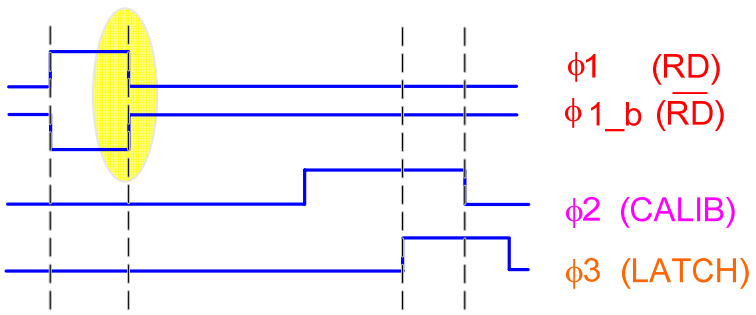


Figure 2-3-b: Timing diagram

At the beginning of the RD phase, the switches S1-S1', S3-S3' et S4-S4' are closed simultaneously. The voltage Vr2 = 0 is assumed for simplification. The signal V_{C1}= $A_1(V_{ref1}+\Delta V1-V_{inRd})$ is then stored on the capacitor C1 and the signal V_{C2}= $[A_3/(1+A_3)]\,\Delta V3 - A_2\Delta V2$ is stored on the capacitor C2 where A1, A2 et A3 are the respective gains of amplifier stages and ΔV1, ΔV2 et ΔV3, their respective offsets.
At the end of RD phase, when the switches S1-S1', S3-S3' et S4-S4' are opened, one will inject a certain quantity of charges generating an offset at the nodes Vx and Vz. Indeed, when the switch transistor opens, the charges which have been accumulated in the channel will flow through the source or the drain in a ratio depending of the impedances seen of each side. For the switches S1-S1', there is a symmetry but the impedances and the input signal level can be different. For the switches S3-S3' et S4-S4', the structure is differential and allows eliminating errors associated with the charges injection. In the real case, the offset will exist because the transistors matching related to the technology tolerance is not perfect.

Using ε_1, ε_3 and ε_4, offset due to the opening of the switches S1-S1', S3-S3' and S4-S4' respectively, we can now calculate the discriminator input offset. 4 cases illustrated the

importance of the order of switches opening are presented below and the results are summarized in table 2-3.

1st case: *At the end of RD phase, the switches S1-S1' are first opened, then S3-S3'and then S4-S4'*, the voltages V_{C1} and V_{C2} will be equal to:

$$V_{C1} = A_1(V_{ref1} + \varepsilon_1 + \Delta V_1 - V_{inRd}) - \varepsilon_3$$

$$V_{C2} = \frac{A_3}{1+A_3}\Delta V_3 + \varepsilon_4 - A_2(\Delta V_2 + \varepsilon_3)$$

At the beginning of the CALIB phase, the switches S2-S2' are closed. The voltage at the node X is given by:

$$V_X = A_1(V_{ref2} - V_{inCal} + \Delta V_1) - V_{C1}$$

$$V_X = A_1[(V_{ref2} - V_{ref1}) - (V_{inCal} - V_{inRd})] - A_1\varepsilon_1 + \varepsilon_3$$

The voltage at the node Y is:

$$V_Y = A_3(V_Z - \Delta V_3)$$

$$V_Z = V_{C2} + A_2(V_X + \Delta V_2)$$

$$V_Y = A_3[V_{C2} + A_2(V_X + \Delta V_2) - \Delta V_3]$$

$$V_Y = A_3\left(A_2V_X + A_2\Delta V_2 + \frac{A_3}{1+A_3}\Delta V_3 - A_2\Delta V_2 - A_2\varepsilon_3 + \varepsilon_4 - \Delta V_3\right)$$

$$V_Y = A_3\left[A_2\left(A_1V_{sig} - A_1\varepsilon_1 + \varepsilon_3\right) - \frac{1}{1+A_3}\Delta V_3 - A_2\varepsilon_3 + \varepsilon_4\right]$$

$$V_Y = A_3A_2A_1V_{sig} - A_3A_2A_1\varepsilon_1 - A_3\frac{\Delta V_3}{1+A_3} + A_3\varepsilon_4$$

$$V_Y(\text{at the input}) = V_{sig} - \varepsilon_1 - \frac{\Delta V_3}{A_1A_2(1+A_3)} + \frac{\varepsilon_4}{A_1A_2}$$

$$\boxed{V_{off1} = -\varepsilon_1 - \frac{\Delta V_3}{A_1A_2(1+A_3)} + \frac{\varepsilon_4}{A_1A_2}}$$

We can see that the error related to the opening of the switches S1-S1', noted ε_1, is not corrected. The error due to the offset of amplifier 3 is reduced by the factor $1/A_1A_2(1+A_3)$. The error due the charge injection related to the opening of the switches S4-S4' is attenuated by the factor $1/A_1A_2$. The charges injection due to the opening of the switches S3-S3' is eliminated.

2nd case: *At the end of RD phase, the switches S1-S1'are first opened, then S4-S4' then S3-S3'*, the offset voltage at the input is given by:

$$\boxed{V_{off2} = -\varepsilon_1 - \frac{\Delta V_3}{A_1 A_2 (1 + A_3)} + \frac{\varepsilon_3}{A_1} + \frac{\varepsilon_4}{A_1 A_2}}$$

We have the same errors as previously and in addition, the error due to the opening of the switches S3-S3' attenuated by the factor $1/A_1$.

3rd and 4th cases: *See summary in Table 2-3*

5th case: *At the end of RD phase, the switches S3-S3' are first opened, then S4-S4', then S1-S1':*

$$V_{C1} = A_1(V_{ref1} + \Delta V_1 - V_{inRd})$$

$$V_{C2} = \frac{A_3}{1 + A_3}\Delta V_3 - A_2 \Delta V_2$$

1) The switches S3-S3' are opened, then S4-S4', the voltages V_{C1} et V_{C2} are:

$$V_{C1} = A_1(V_{ref1} + \Delta V_1 - V_{inRd}) - \varepsilon_3$$

$$V_{C2} = \frac{A_3}{1 + A_3}\Delta V_3 + \varepsilon_4 - A_2(\Delta V_2 + \varepsilon_3)$$

2) The switches S1-S1' are opened, the voltage at the nodes V_X and V_Z are:

$$V_X = A_1 \varepsilon_1 + \varepsilon_3$$

$$V_Z = \frac{A_3}{1 + A_3}\Delta V_3 + \varepsilon_4 + A_1 A_2 \varepsilon_1$$

3) The switches S2-S2' are closed, we obtain:

$$V_X = A_1 V_{sig} + \varepsilon_3$$

$$V_Z = A_1 A_2 V_{sig} + \frac{A_3}{1 + A_3}\Delta V_3 + \varepsilon_4$$

$$V_Y = A_3(V_Z - \Delta V_3)$$

$$V_Y = A_1 A_2 A_3 V_{sig} - A_3 \frac{\Delta V_3}{1 + A_3} + A_3 \varepsilon_4$$

$$\boxed{V_{off3} = -\frac{\Delta V_3}{A_1 A_2 (1 + A_3)} + \frac{\varepsilon_4}{A_1 A_2}}$$

Therefore, if the switches are opened in this order, first S3-S3' then S4-S4' then S1-S1', the error ε_1 due to the opening of the switches S1-S1' is eliminated.

6ième case: *At the end of RD phase, the switches S4-S4' are first opened then S3-S3' then S1-S1'*, the input offset of the discriminator is found as:

$$V_{off4} = -\frac{\Delta V_3}{A_1A_2(1+A_3)} + \frac{\varepsilon_3}{A_1} + \frac{\varepsilon_4}{A_1A_2}$$

In this case, the error due to the opening of the switches S3-S3' is added and attenuated by the gain A_1.

Summary

case	Order of switches opening	Input offset of the discriminator
1	S1, S3, S4	$-\varepsilon_1 - \frac{\Delta V_3}{A_1A_2(1+A_3)} + \frac{\varepsilon_4}{A_1A_2}$
2	S1, S4, S3	$-\varepsilon_1 - \frac{\Delta V_3}{A_1A_2(1+A_3)} + \frac{\varepsilon_3}{A_1} + \frac{\varepsilon_4}{A_1A_2}$
3	S3, S1, S4	$-\varepsilon_1 - \frac{\Delta V_3}{A_1A_2(1+A_3)} + \frac{\varepsilon_4}{A_1A_2}$
4	S4, S1, S3	$-\varepsilon_1 - \frac{\Delta V_3}{A_1A_2(1+A_3)} + \frac{\varepsilon_3}{A_1} + \frac{\varepsilon_4}{A_1A_2}$
5	S3, S4, S1	$-\frac{\Delta V_3}{A_1A_2(1+A_3)} + \frac{\varepsilon_4}{A_1A_2}$
6	S4, S3, S1	$-\frac{\Delta V_3}{A_1A_2(1+A_3)} + \frac{\varepsilon_3}{A_1} + \frac{\varepsilon_4}{A_1A_2}$

Table 2-3

In conclusion, the switches S3-S3' et S4-S4' have to be opened before the switches S1-S1' and consequently, the major error due to the opening of the switches S1-S1' could be eliminated. The switches S3-S3' have to be also opened before the switches S4-S4' in order to eliminate the error due to the opening of S3-S3'. This error is less important because the structure is differential and the error is divided by the gain of the first stage. The figure 2-3-c shows the optimized timing diagram to remove the input offset of discriminator.

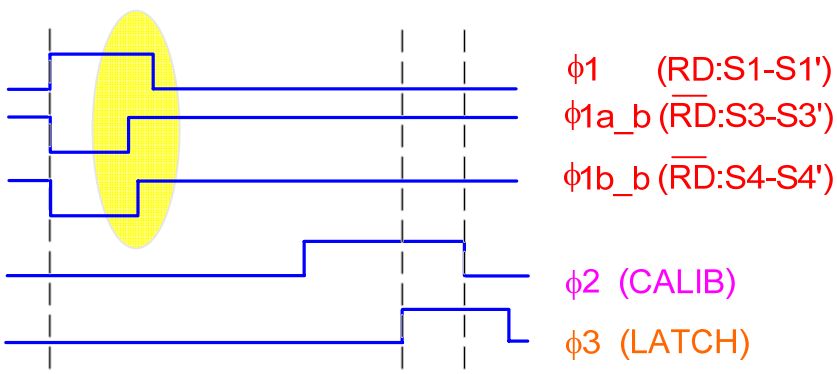


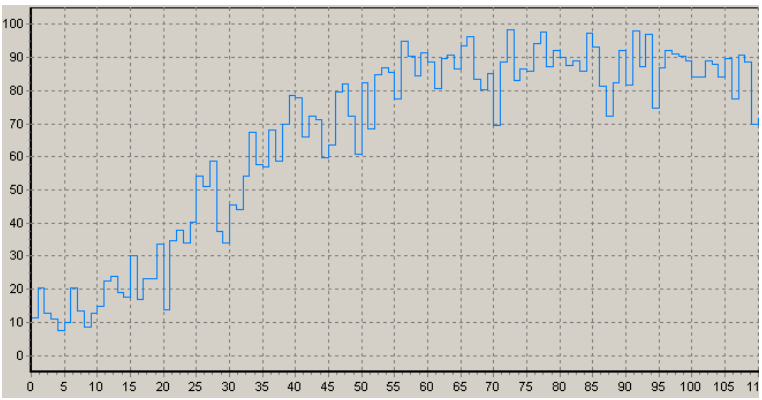
Figure 2-3-c: Optimized timing diagram

2-4- Test results of MIMOSA-22AHR

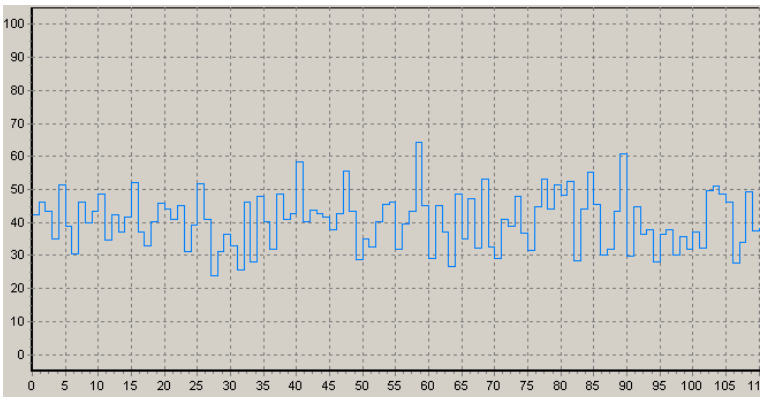
MIMOSA-22AHR is a small prototype with 128 discriminators. In order to verify the timing diagram, an additional functionality has been implemented in the MIMOSA-22AHR allowing three possibilities:

a) RD_b signal is delayed of 3ns compared to the RD
b) RD signal is delayed of 3 ns compared to RD_b (as in optimized timing diagram)
c) Both RD and RD_b signals are delayed on 3ns. They are sent in the same time.

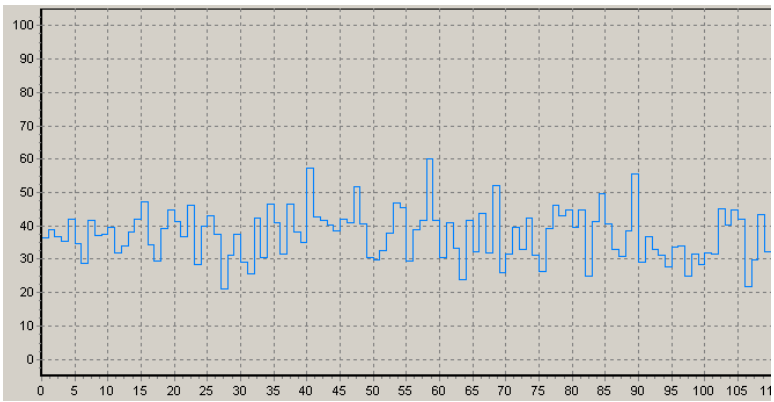
The figure 2-4-a presents the test results of the threshold dispersion as a function of the discriminator position in three cases. The discriminator is connected to the pixels.



Case (a) Delay on RD_b



Case (b) Delay on RD



Case (c): Same delay on RD and RD_b

Figure 2-4-a: Threshold dispersion as a function of the discriminator position for 3 cases

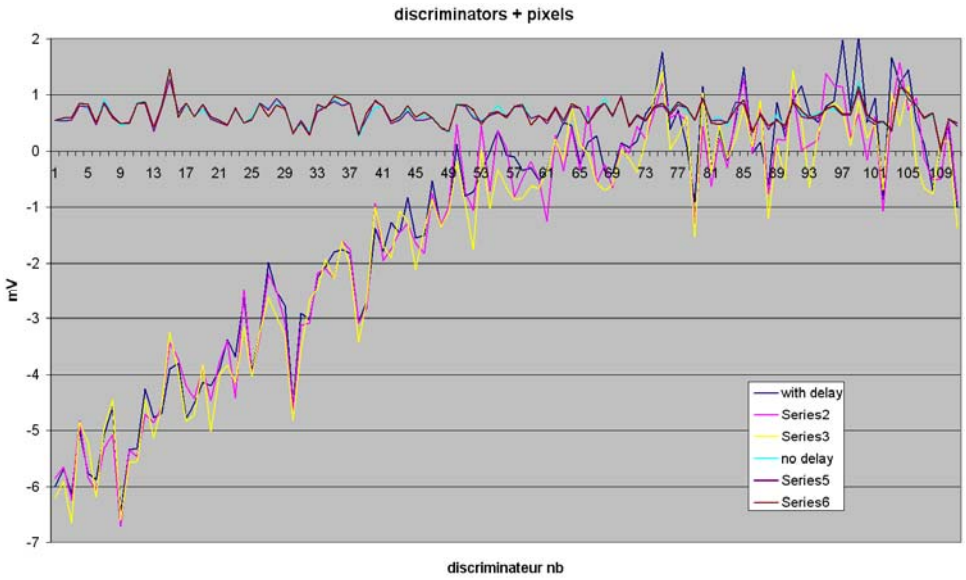


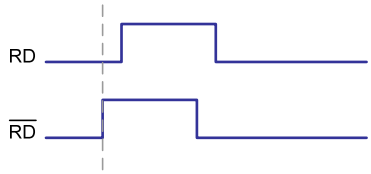
Figure 2-4-a: Threshold dispersion as a function of the discriminator position with delay on RD_b for different pixel row (with delay, series2, series3) and with no delay for different pixel row (no delay,series5, series6).

It can be observed that when the RD_b signal is delayed compared to the RD signal, the threshold dispersion can be also reproduced in the small prototype.

In Ultimate sensor, the signal RD will be delayed compared to RD_b to remove the systematic threshold dispersion

2-5- Simulation of the discriminator row of Ultimate

The discriminator row of Ultimate has been simulated with extracted parasitic RC on reference lines (VRef1, VRef2 and Vr2) and control lines (Φ1, Φ2 and Φ3). The row is divided in 4 groups noted A, B, C and D. The reference buffers have been replaced by ideal generators. The discriminator timing diagram is optimized as following:



The simulation was carried out with the simulator Ultrasim, Analog mode, high precision.

The figure 2-5-a presents the settling of the reference and clamping voltages for each group of discriminator.

The figure 2-5-b presents the intermediate voltages at the output node of the first gain stage noted V_X, at the node of the second output stage noted V_Z and at the third output stage noted V_Y (before the latch).

In the figure 2-5-a, we can see that the reference and clamping voltages have the time to reach their final values in the RD and CALIB periods. In the Figure 2-5-b, we can note that all intermediate voltages V_X, V_Z and V_Y are stable and are at zero volt in the RD and CALIB periods. The residuals values seen at the input of the discriminator (V_X/A1) are shown in the figure 2-5-c.

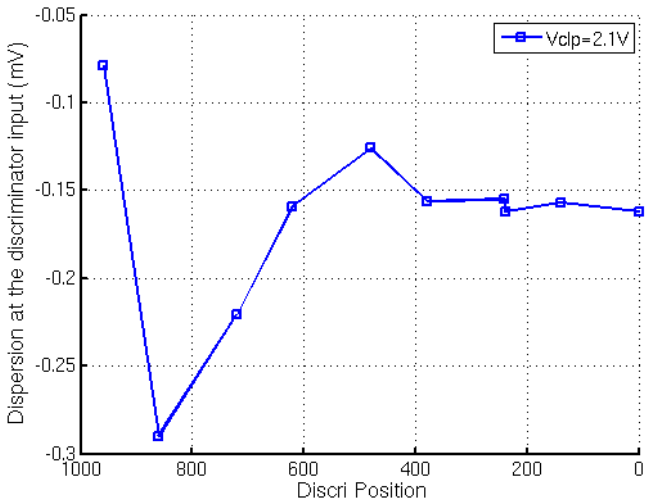
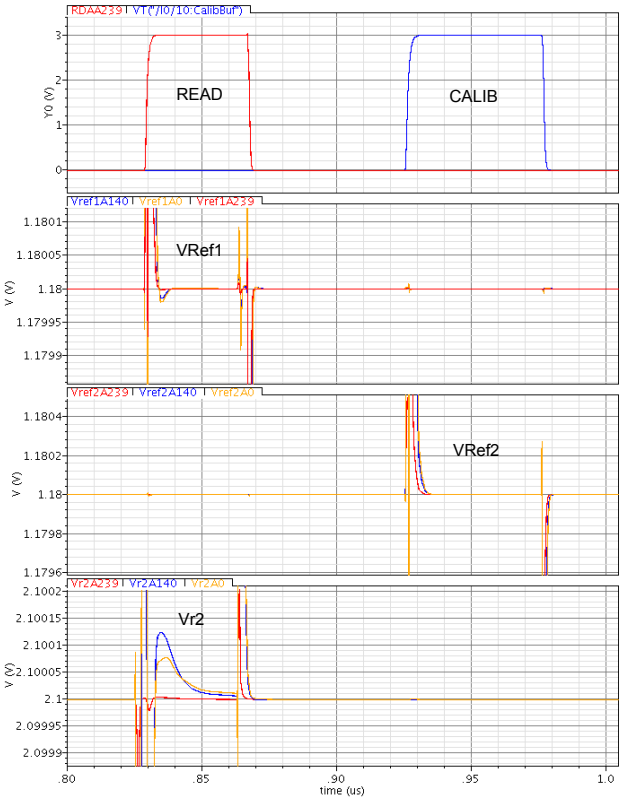


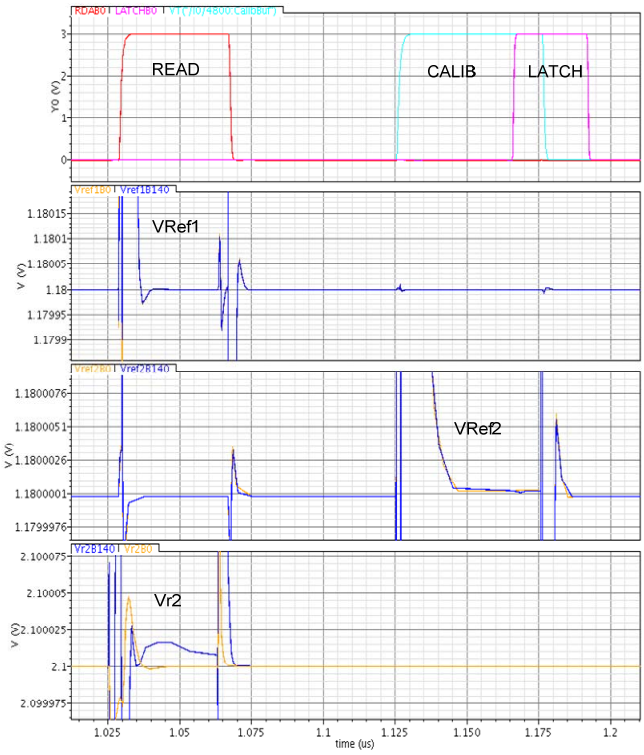
Figure 2-5-c: Dispersion at the discriminator input as a function of the position

We can see in the figure 2-5-c that the dispersion resulting of the effect of the long line on the timing diagram has been corrected and is lower than 300 µV.

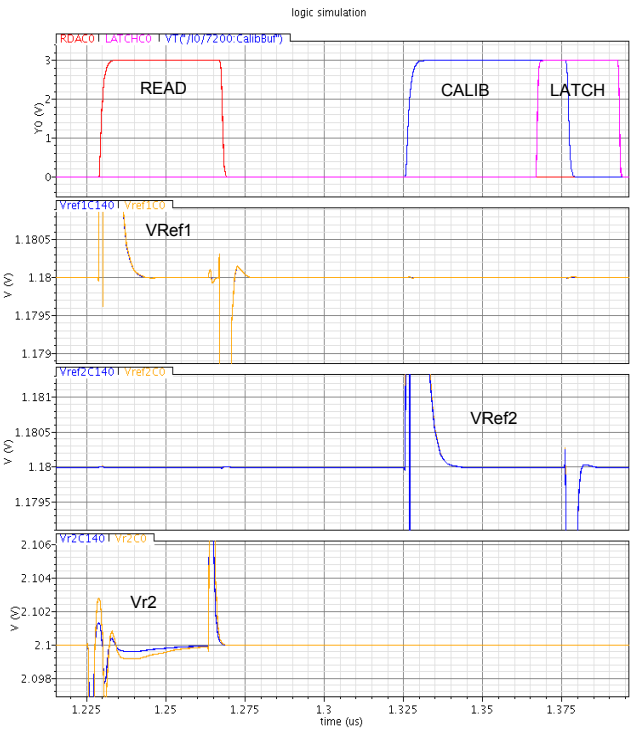
These results have been obtained after the analysis of test results of PHASE-1. The following paragraph describes the simulations which have been carried out on the PHASE-1 sensor to reproduce the dispersion.



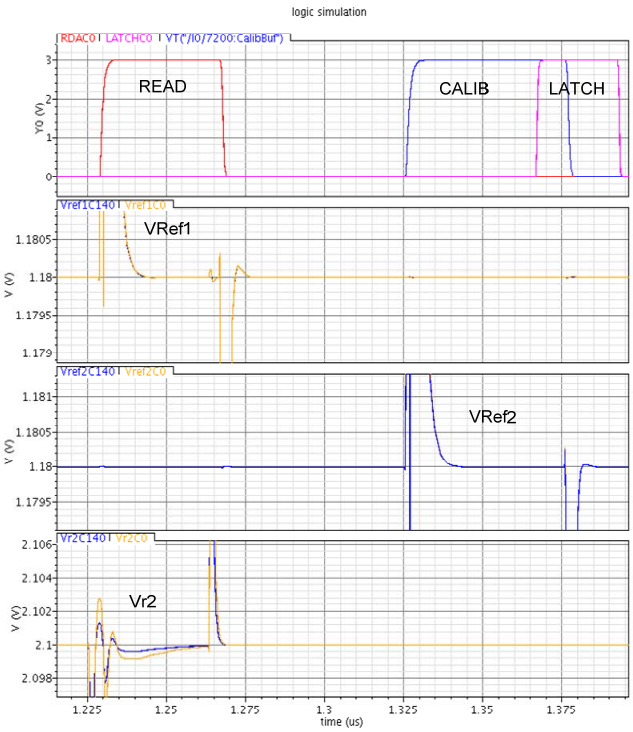
Group A



Group B

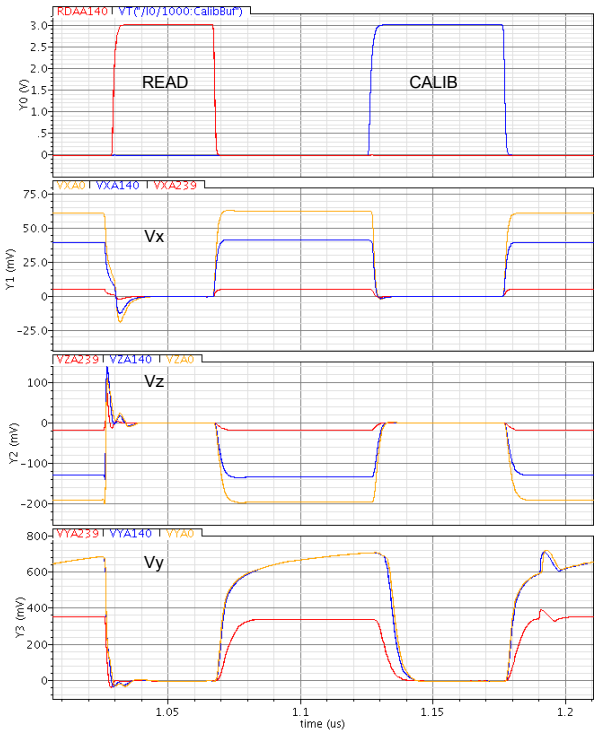


Group C

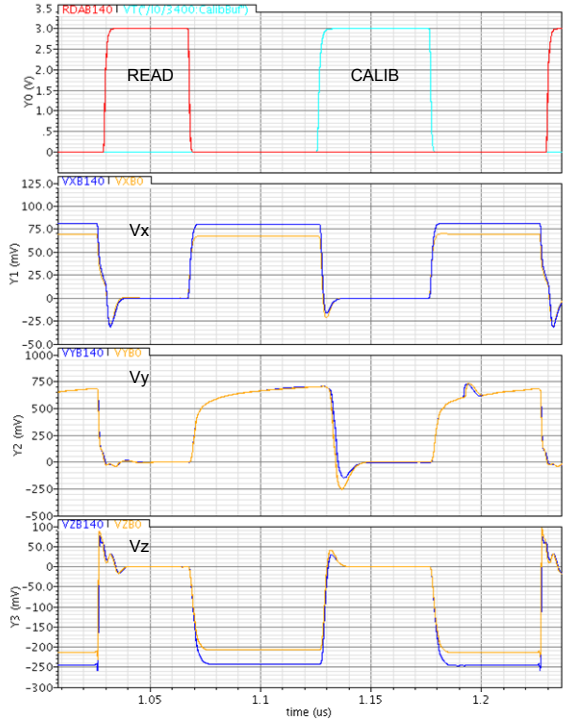


Group D

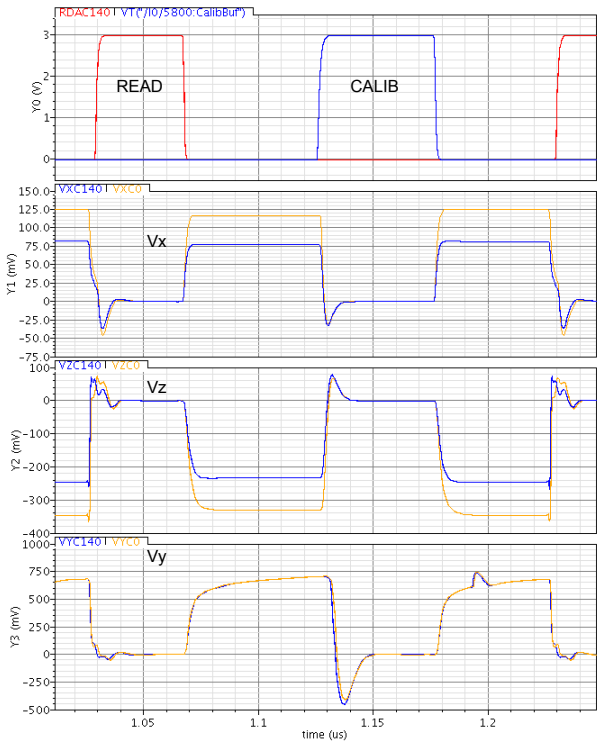
Figure 2-5-a: settling of the reference voltages, VRef1, VRef2 and Vr2 (clamping discri) for each group of discriminators.



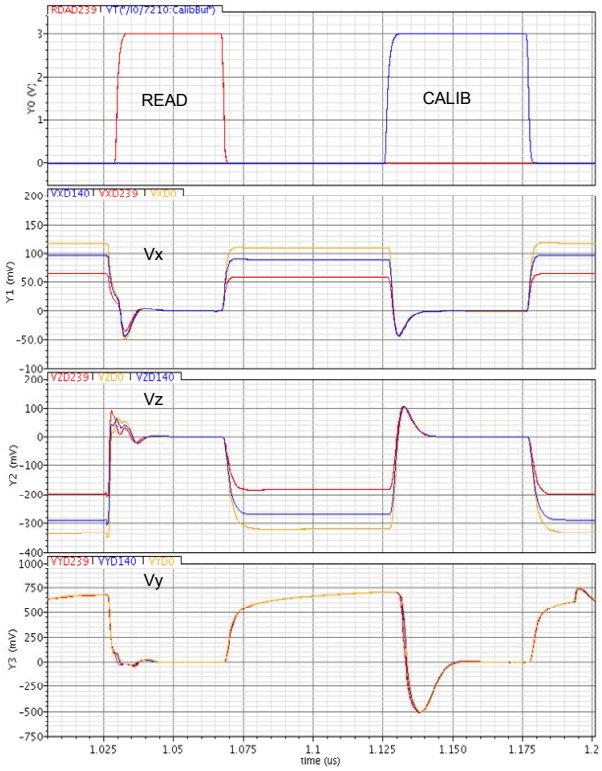
Group A



Group B



Group C

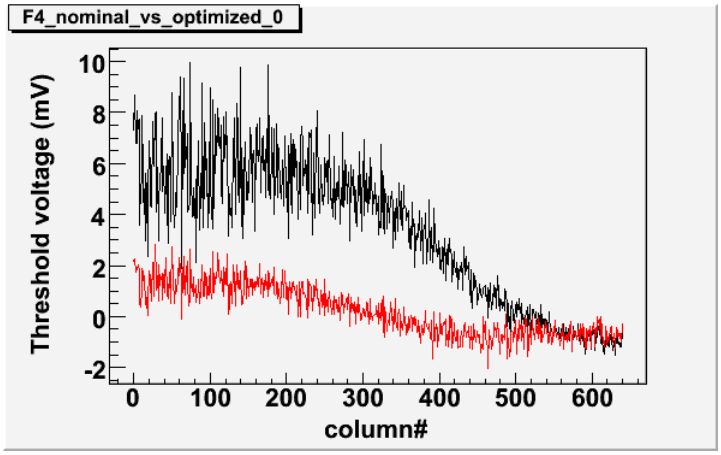


Group D

Figure 2-5-b: settling of the intermediate voltages VX (first gain stage output), VZ (second gain stage output) and VY (third gain stage output) for each group of discriminators.

2-6- Simulation of the PHASE1 discriminator row

In order to reproduce the evolution of the threshold dispersion observed by the test team at BNL (as shown in the figure below), the discriminator row of PHASE1 chip has been simulated taking into account the effect of the long lines.



Simulation conditions :

Phase1 consists of 640 discriminators. The RC of the control lines (RD, RD_b, CALIB, LATCH) and reference voltages lines (VRef1, VRef2, VDISCLP (or Vr2: Clamping Discri)) have been considered. The common-mode VMCPix is 1.18 V. The reference buffers are replaced by ideal generators.

In the figures below, the dispersion represents the value of the voltage V_X defined in Figure 2-3-a. This value has to be divided by the gain A_1 (# 3.7) of the first stage to obtain the threshold dispersion of the discriminator.

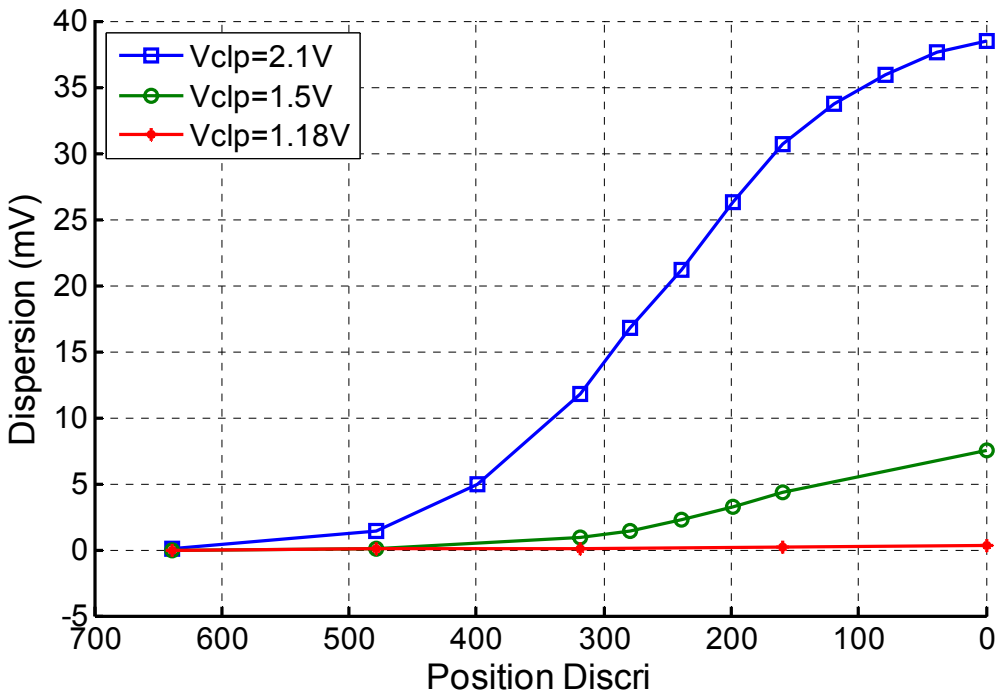
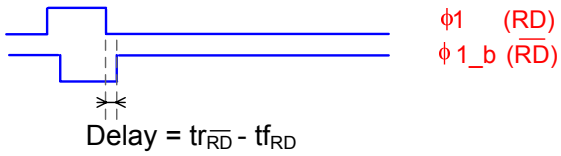


Figure 2-6-a: Dispersion of V_X as a function of the position of discriminator for 3 clamping voltages

The figure 2-6-a shows the dispersion at the node V_X as a function of the discriminator position. This waveform represents well what we have been observed in test.

The figure 2-6-b presents the control signals RD (Φ1) and RD_b (Φ1_b) as a function of the discriminator position.

The figure 2-6-c shows the influence of the delay defined by the difference between the rise edge of RD_b and the fall edge of the RD as a function of the discriminator position.



The following explains classical timing issues on command lines. But they are complexe due to the long interconnects.

One has to remind that in PHASE1, the switches S1-S1' ($W_{S1\text{-}S1'}$ = 1 µm) and S4-S4' dummy ($W_{S4\text{-}S4'}$=1.5 µm) are connected to the RD line and the switches S3- S3' ($W_{S3\text{-}S3'}$ = 6 µm) and S4-S4' ($W_{S4\text{-}S4'}$ = 2 µm) are connected to the RD_b line. We note that the capacitive load of the RD_b line is much largest than that of the RD line. In figure 2-6-b, we see that the slope of the RD_b signal decreases faster than that of RD signal. This is the case as the discriminator is close to the source. Therefore, the RD_b signal is delayed relative to the RD signal. In this configuration, the offset ε_1 due to the opening of the switches S1-S1' is memorized partly in the capacitors C1-C1'. The switches S3-S3' et S4-S4' are controlled by the same signal RD_b. If the S3 and S4 slopes are identical (true in simulation), the switches open at the same time. The slope can change if the signal level at the source of transistor is different. Here, it is not the case: the clamping voltage is 2.1 V (for S3-S3') and the ouput common-mode is 2.1 V (for S4-S4'). In the layout, the RD_b signal is divided in two paths to the transistors S3-S3' and to the transistors S4-S4'. As the capacitor is three times greater on the S3-S3' line, the slope decreases faster than that of the S4-S4'. This configuration is unfavourable and the charge injection ε_3 could be also memorized.

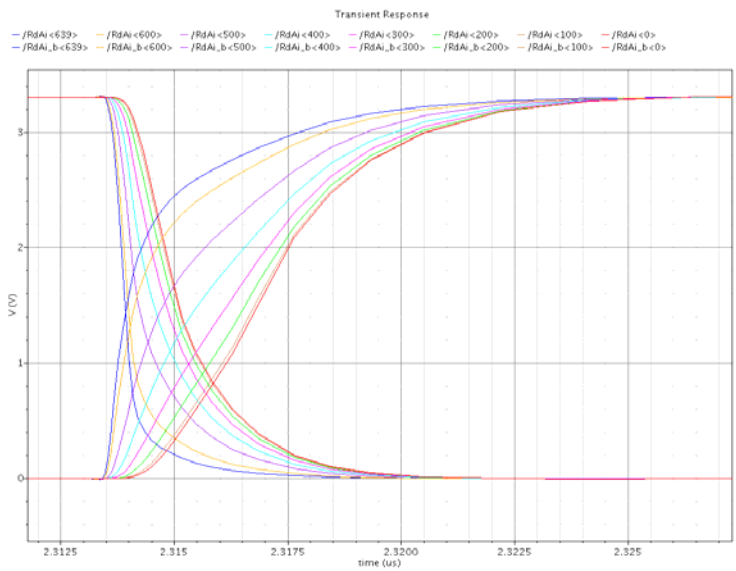


Figure 2-6-b: Evolution of the signal RD and RD_b (at the moment where S1-S1', S3-S3' and S4-S4' turn off) as a function of the discriminator position (for example, in blue: discri 639 the closest of the source, in red: discri 0 the farthest).

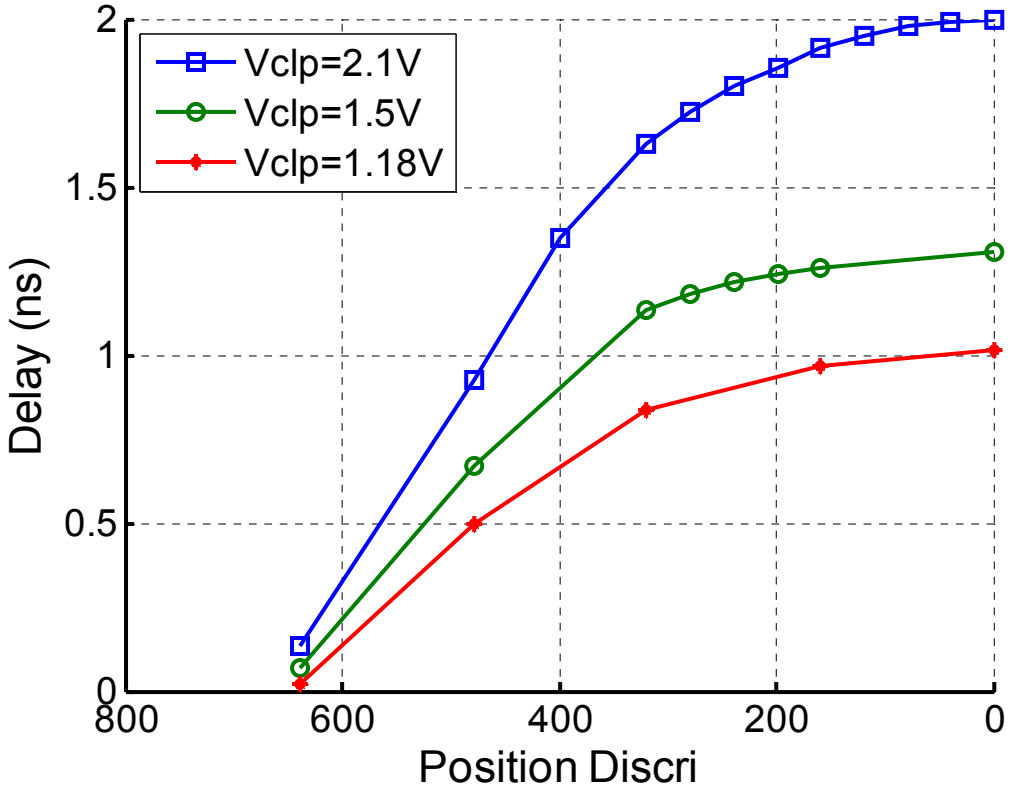


Figure 2-6-c: Delay between the signal RD_b and RD as a function of the discriminator position for 3 clamping voltage.

In the figure 2-6-c, it can be observed that the delay continues to increase but slowly as the discriminator is far from the source. The delay between RD and RD_b depends greatly of the value of the clamping voltage.

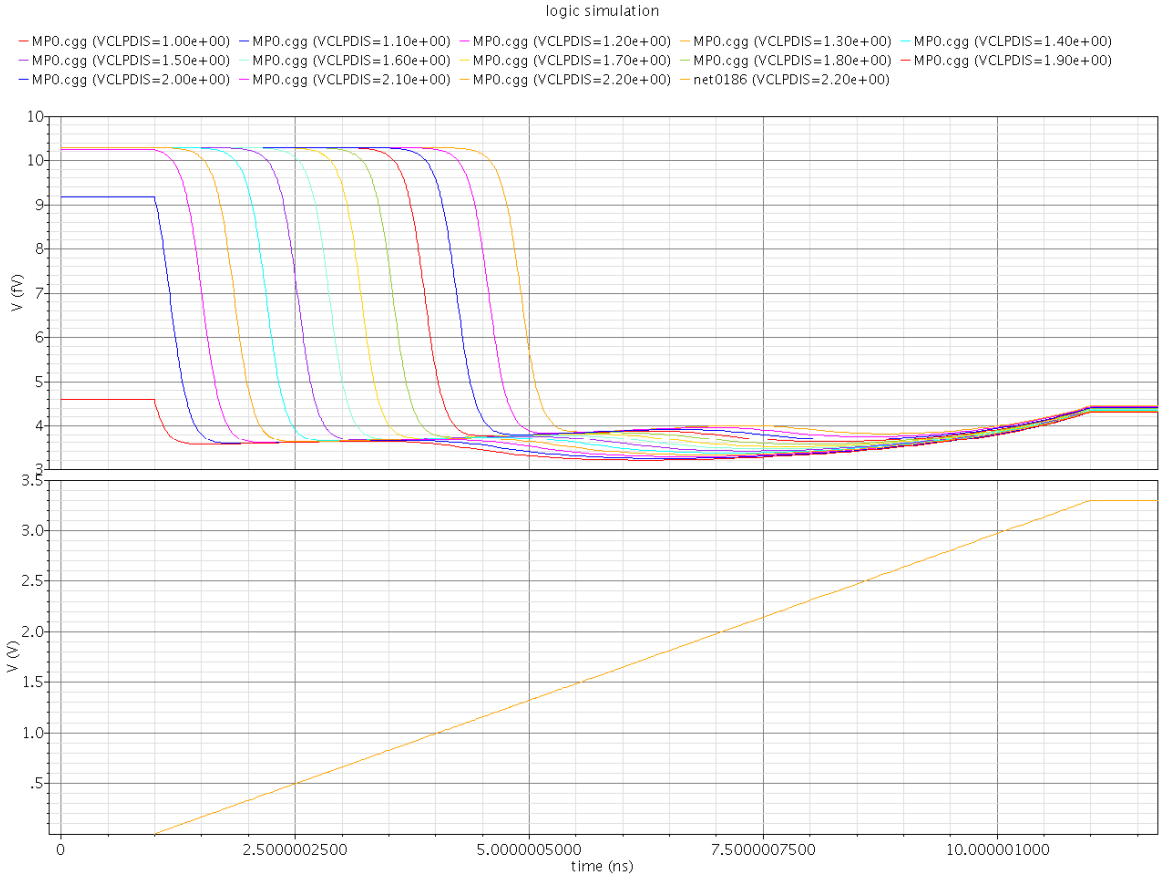


Figure 2-6-d: At the top, variation of the gate capacitance C_g of the clamping transistor PMOS in fC for different clamping voltages for a gate control signal moving the transistor from on to off state. At the bottom, voltage applied at the gate of the clamping transistor

The figure 2-6-d represents the variation of the gate capacitance C_g of the transistor PMOS (S3) as a function of the voltage applied on the transistor source in the range of values 1-2.2 V, during the low-to-high transition (when the switch turns off). We can see that the transition between Cg_{On} (~10fF) and Cg_{Off} (~4 fF) appears at different moments as a function of the voltage applied at the source of transistor for a given slope of the gate control signal. The moment of transition increases linearly with the source voltage. Therefore, the signal RD_b will be more delayed as the clamping voltage will be higher. This can explain that the delay RD-RD_b depends of the clamping voltage.

If the clamping voltage is reduced, the Vgs-Vt is also reduced and the resistor R_{on} of the switch increases (R_{on}(W=6 µm) = 1.7 kΩ => 11.7 kΩ). The time constant increases but remains much lower than the RD time ($t_{on} = R_{on}C_{clamp}$ =0.2 ns => 1.7 ns).

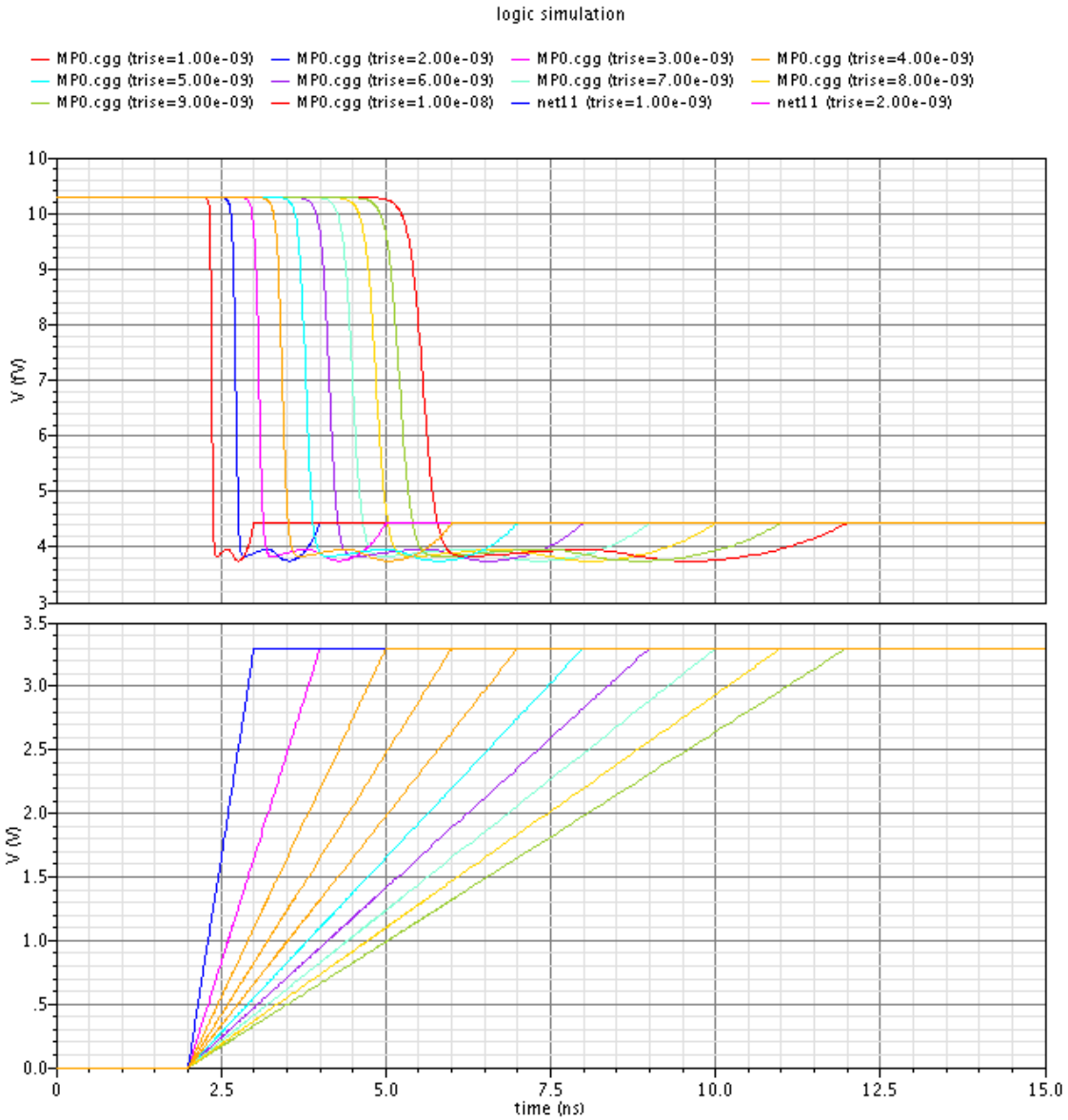


Figure 2-6-e: At the top, variation of the gate capacitance C_g of the clamping transistor PMOS in fC for different slopes of the gate control signal. The voltage at the source of transistor is 2.1 V.
At the bottom, voltage applied at the gate of the clamping transistor

The figure 2-6-e shows the variation of the gate capacitance C_g of the transistor PMOS (S3) as a function of the slope of the gate control signal. We note that the moment of the on-off transition increases linearly as the slope of gate control signal decreases.

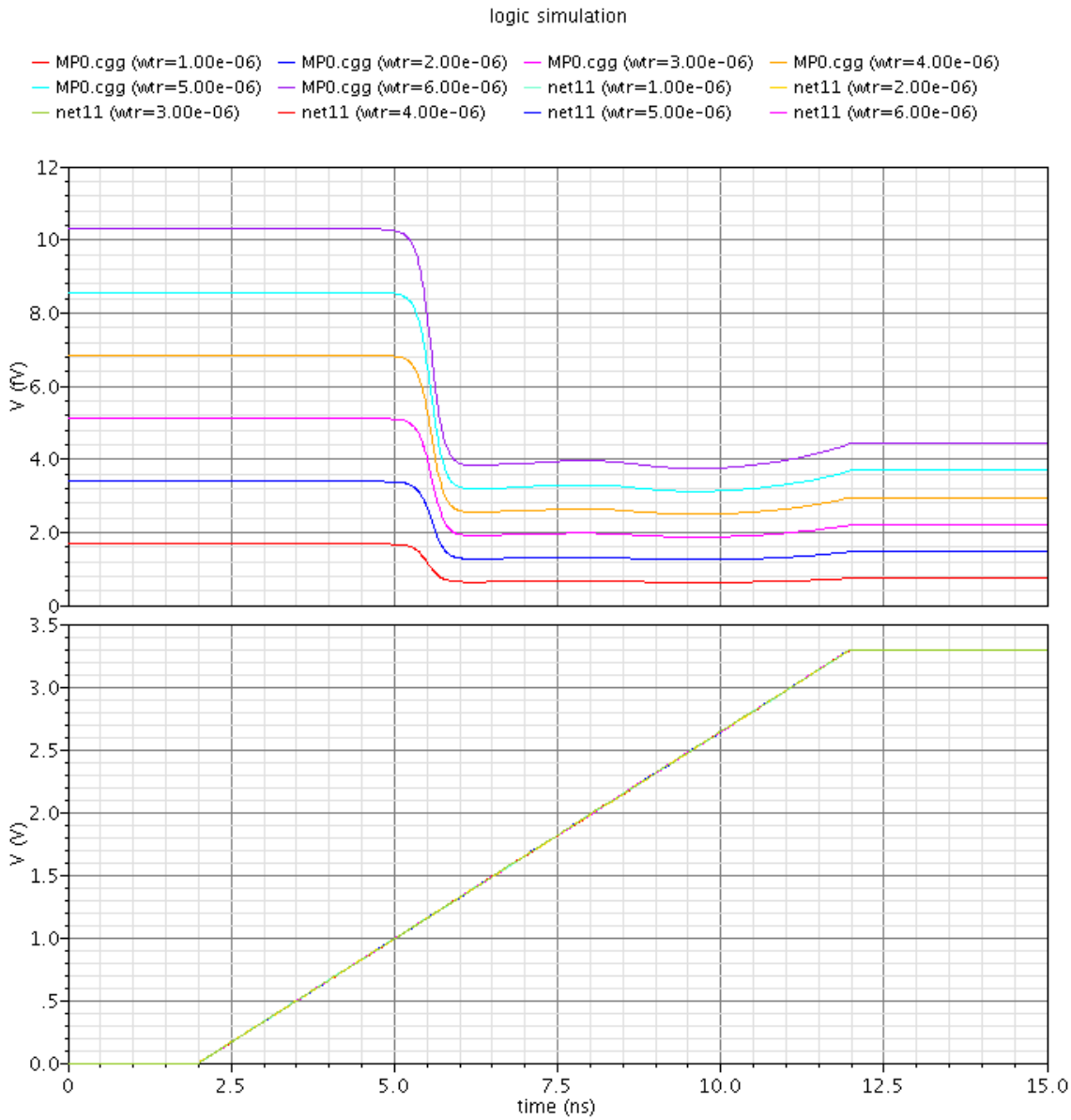


Figure 2-6-f: At the top, variation of the gate capacitance of the clamping transistor PMOS in fC for different gate widths (w). The voltage at the source of transistor is 2.1 V
At the bottom, voltage applied at the gate of the clamping transistor.

The figure 2-6-f presents the variation of the gate capacitance C_g of the transistor PMOS (S3) as a function of the gate width (w). We see that the gate capacitance Cg_{On} and Cg_{Off} is linear with the gate width. This parameter has no influence on the moment of the on-off transition. Reducing the transistor width allows decreasing the capacitance and will have an effect of the timing.

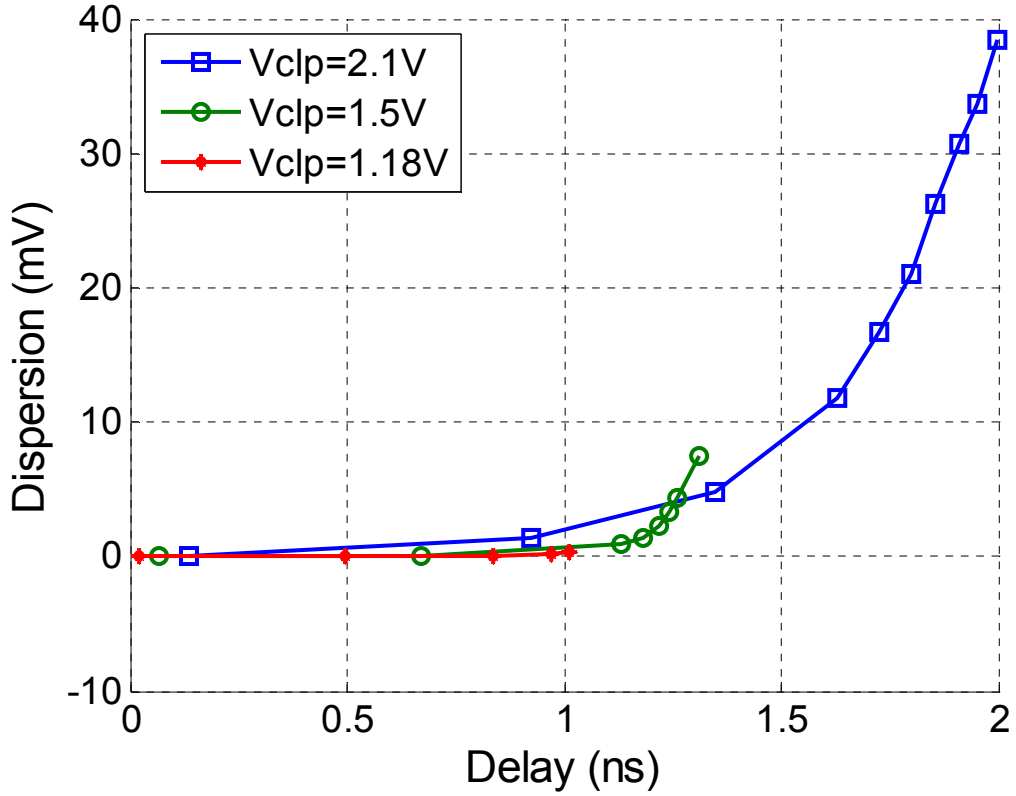


Figure 2-6-g: Dispersion at the node Vx as a function of the delay between RD_b and RD for 3 clamping voltages.

The figure 2-6-g shows the dispersion at the node Vx as a function of the delay between the signals RD and RD_b for 3 clamping voltage. Now, we note a slightly influence of the value of the clamping voltage on the dispersion.

2-7- Influence of some factors on the discriminator dispersion

The charge injection involves a complex process whose resulting effects depend on several factors. Two sources of errors appear at the opening of the switch: the clock feed-through and the charge redistribution.

The source and drain of the switch are connected to the gate by parasitic capacitances ("overlap capacitances"). The overlap capacitance gate-drain and the capacitance at the drain side form a capacitive divider and then a fraction of the clock voltage is partially injected in the signal path. The charge Q and the error voltage ΔV can be written by:

$$Q = C_{ovl}\ (V_h - V_l)$$

$$\Delta V \cong \frac{Q}{C}$$ where C is the capacitor at each side

As the overlap capacitor is proportional to the transistor width, this error can be considered as a constant offset and is reduced by using differential structure.

The other source of error is the charge redistribution. When the switch turns off, the charge which has been accumulated in the channel disappears and is redistributed towards both sides. This charge Q and the error ΔV can be expressed by:

$$Q \cong C_{ox}\ WL\ (V_h - V_{sig} - V_t)$$

$$\Delta V = \frac{Q}{2C}$$ (Assuming half charge goes to each side)

This error depends on the signal and can cause distortion.

In order to study the influence of some parameters such as the impedance levels at the source and drain nodes, the signal input levels..., we have simulated one discriminator by varying the slope of the signal RD_b (see figure 2-7-1-a).

2-7-1- Threshold dispersion as a function of the delay RD-RD_b

<u>Simulation conditions:</u>

One discriminator of PHASE1
The resistance in the pixel line is R_{Pixel} =1 Ω,
The resistance in the reference line is R_{VRefl} = 1 kΩ
We have taken these values to highlight the charge injection.
Φ_1=RDA
Φ1a_b=RDA_b
Φ1b_b=RDA_b

The figure 2-7-1-b shows the evolution of the voltage at the node V_x as a function of the slope of RD_b and therefore of the delay between RD and RD_b. We see that the offset dispersion, when the switches S1-S1' turns off before S3-S3', increases linearly with the delay.

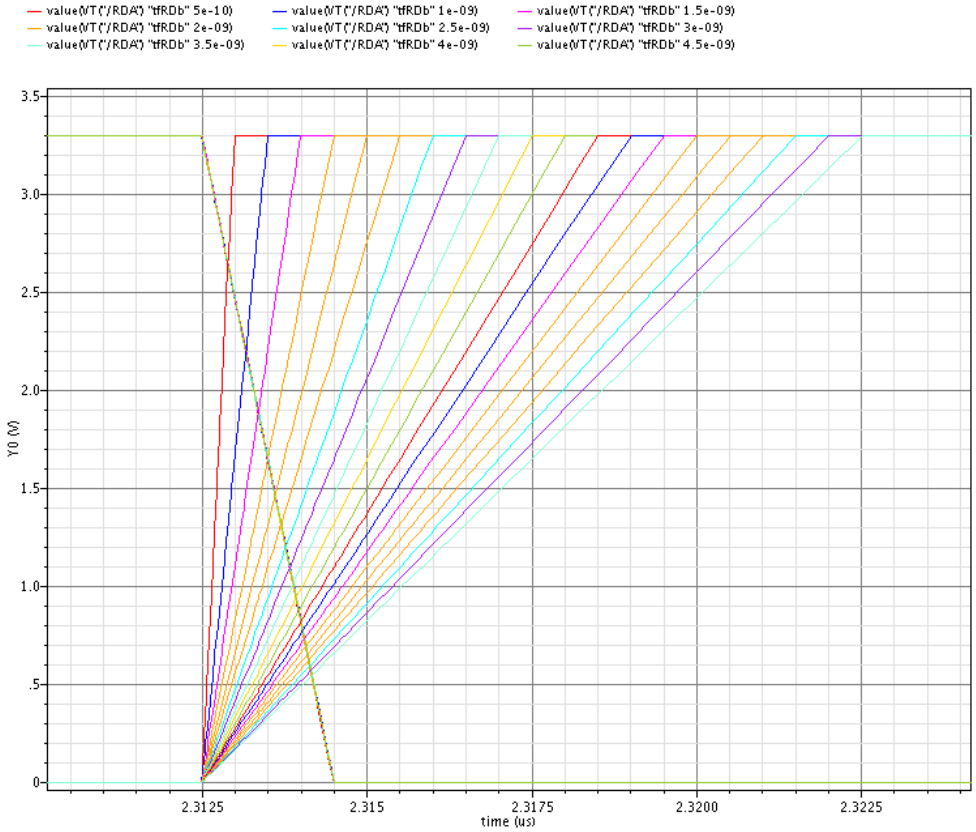


Figure 2-7-1-a: Evolution of the slope of the signal RD_b. The slope of the signal RD remains constant.

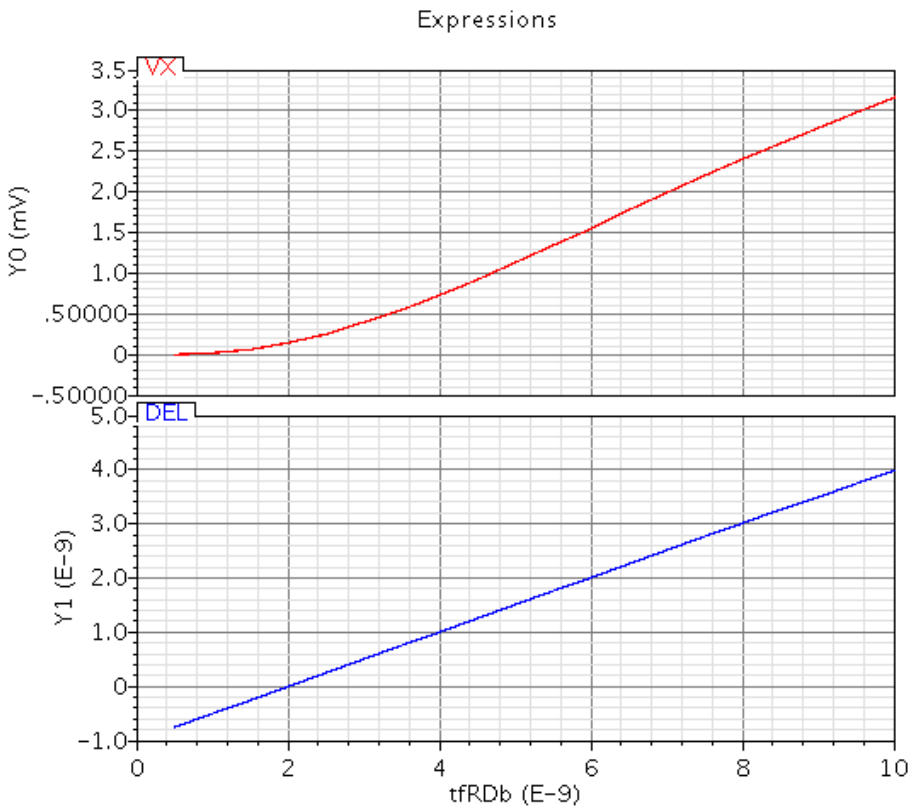


Figure 2-7-1-b: Evolution of the voltage at the node V_X as a function of the slope of RD_b.

2-7-2- Threshold dispersion as a function of the delay RD-RD_b and the value of clamping voltage

The figure 2-7-2 presents the dispersion at the node V_X as a function of the delay RD-RD_b for 3 clamping voltage 2 V, 1.5 V and 1 V. We see that the charge injection decreases as the clamping voltage becomes lower. In fact, the delay between RD-RD_b depends of the signal applied to the source of the switch transistor (cf fig.2-6-d).

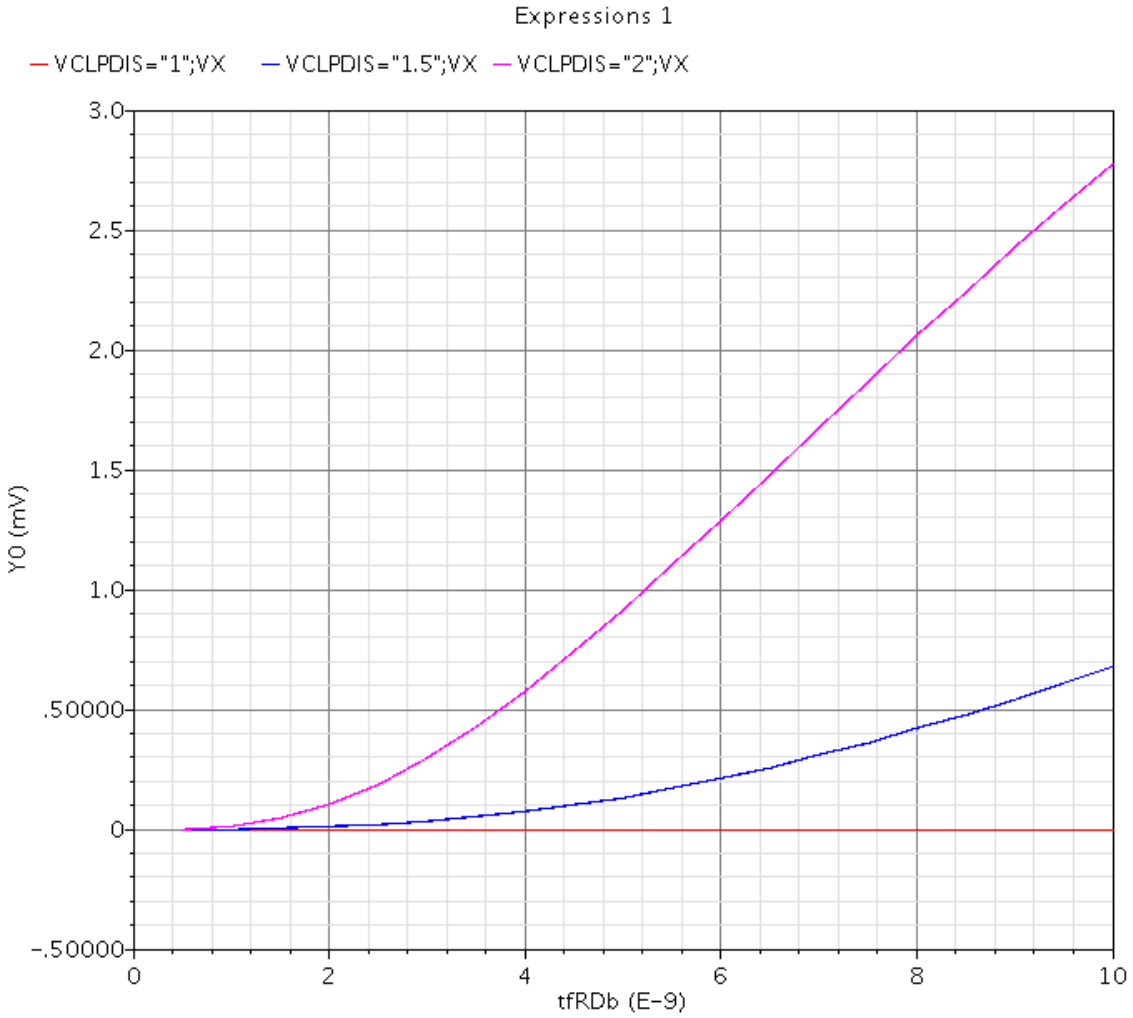


Figure 2-7-2: Evolution of the voltage at the node V_X as function of the slope of RD_b for 3 clamping voltage 2 V, 1.5 V and 1 V.

2-7-3- Threshold dispersion as a function of the delay RD-RD_b and the impedance seen at the input V_{Ref1}

The figure 2-7-3 shows the evolution of the dispersion as a function of the delay RD-RD_b for various resistances at the input of V_{Ref1}.

We see that the dispersion depends linearly of the resistances seen at the input of the reference voltage V_{Ref1} and at the pixel output V_{in}. The sign and the value of charge injection ε_1 will depend of impedances at the inputs V_{REf1} and V_{in}.

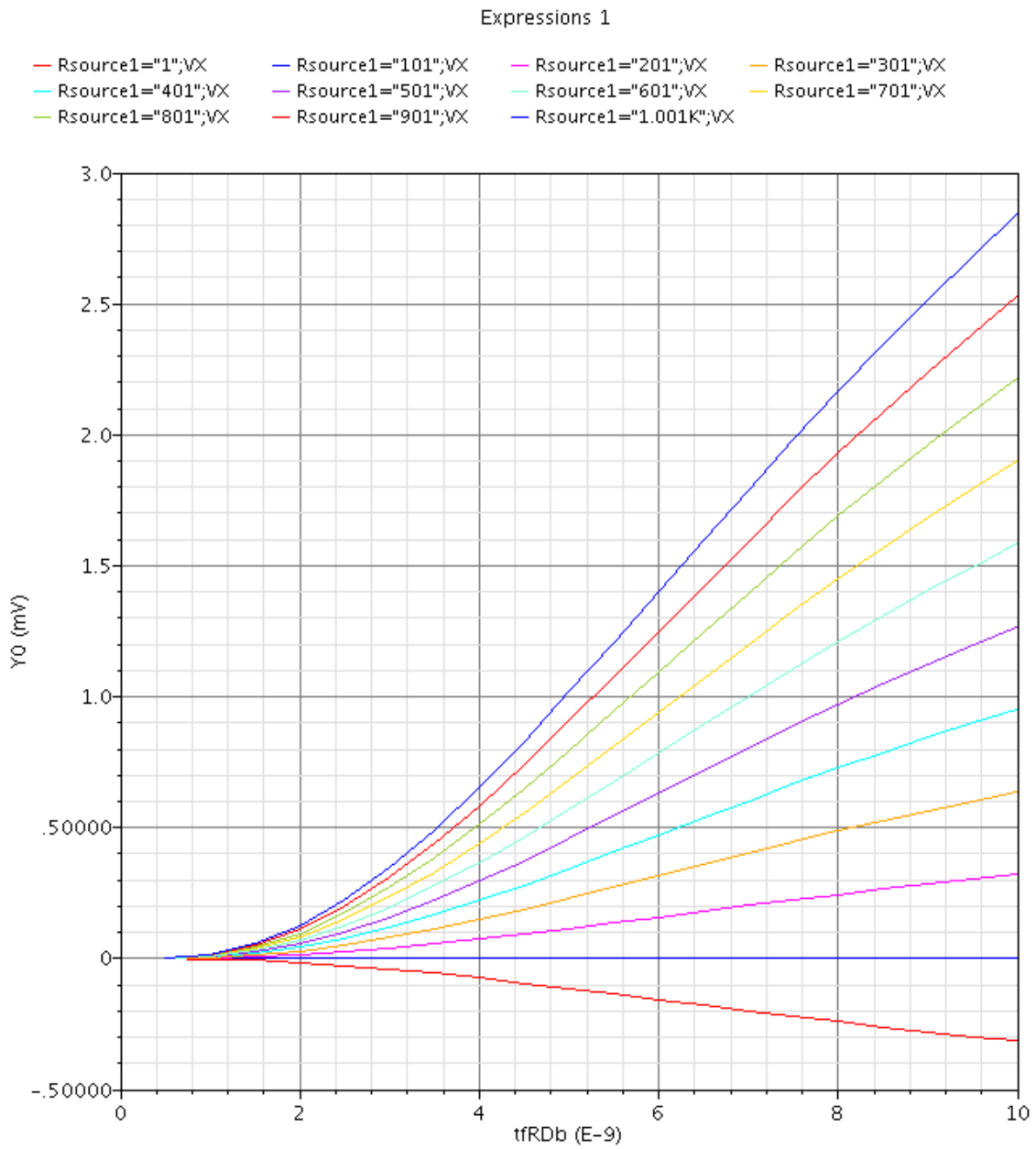


Figure 2-7-3: Evolution of the voltage at the node V_X as function of the slope of the signal RD_b for various resistances on the reference V_{Ref1} (range of 1-1 kΩ). The resistance at the ouput pixel is 100 Ω.

2-7-4- Threshold dispersion as a function of the value of VRef2

The figure 2-7-4-a presents the evolution of the dispersion at the node V_X when the reference voltage V_{Ref2} varies from - 150 mV to +150 mV relative to the common-mode voltage of pixel ($V_{MCpixel}$ = 1.2 V). We see that the charge injection ε_1, when the switches S1-S1' turns off, increases as the reference voltage V_{Ref2} is further from the common-mode.

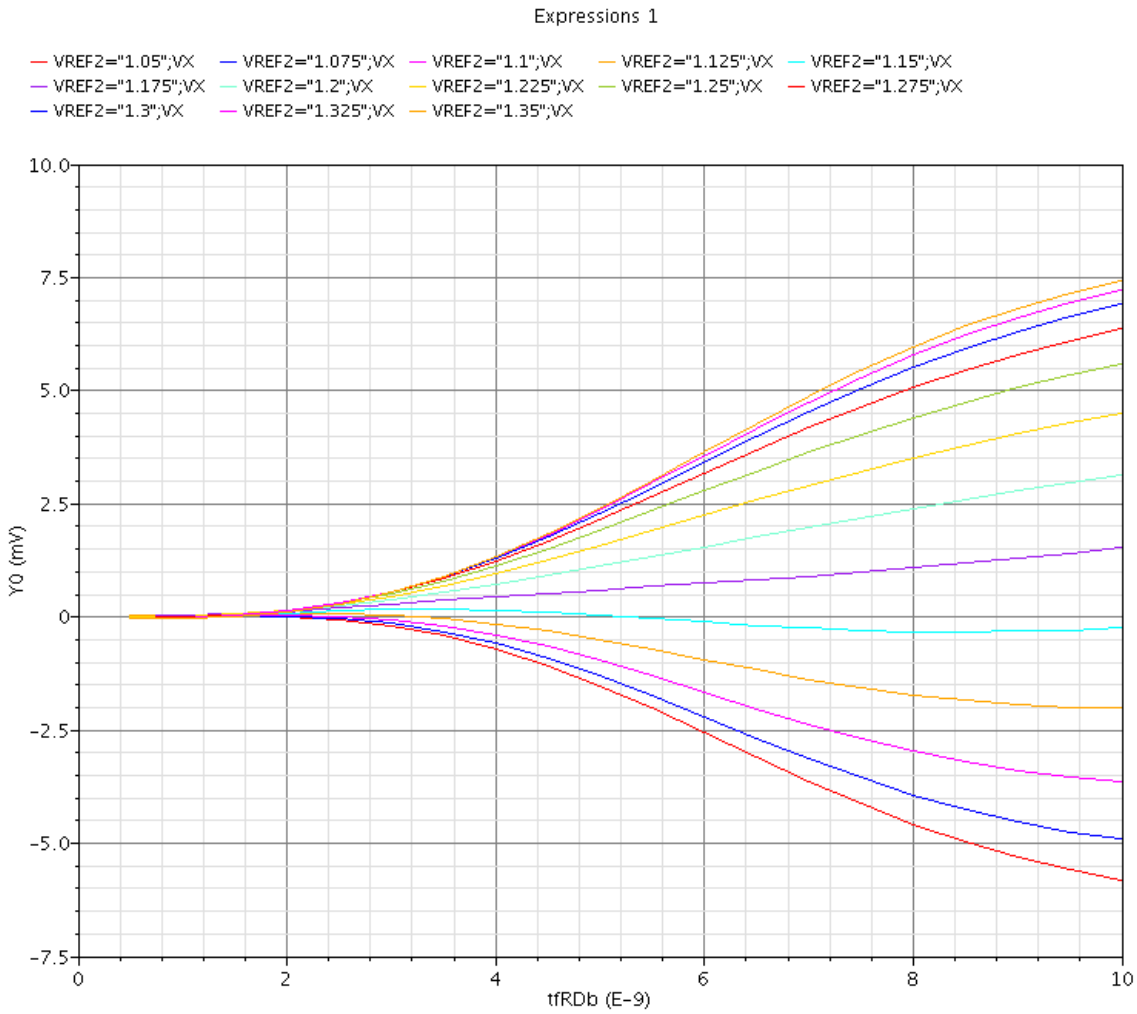


Figure 2-7-4-a: Evolution of the dispersion at the node V_X as function of the slope of the signal RD_b for various values of the reference voltage V_{Ref2}. V_{Ref2} varies from -150 mV to + 150 mV relative to the voltage at the output pixel V_{in}.

The figure 2-7-4-b shows the dispersion at V_x as a function of the discriminator position in the row for various voltagesV_{Ref2}.

The figure 2-7-4-c presents the dispersion at V_x for a signal RD delayed of 3n compared to the signal RD_b to eliminate the charge injection ε_1 (see figure 2-7-4-d).

The figure 2-7-4-f (and 2-7-4-g) is an other way to represent the figure 2-7-4-b (respectively 2-7-4-c).

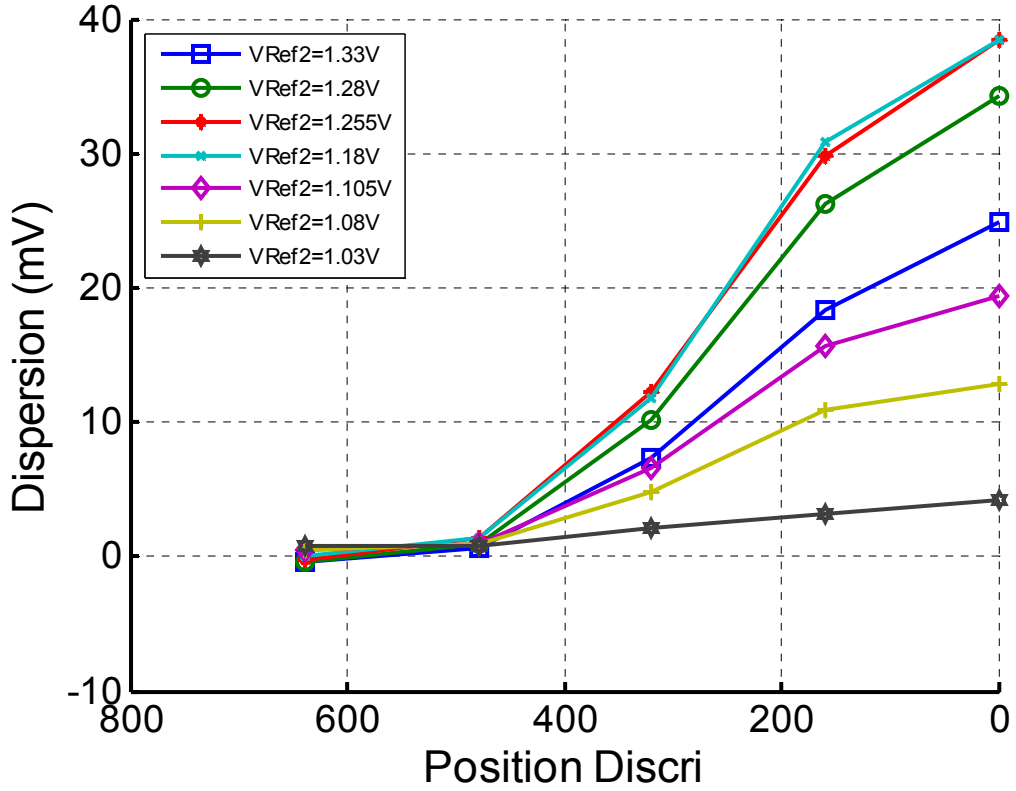


Figure 2-7-4-b: Evolution of the dispersion at V_X as a function of discriminator position for different values of the reference voltage VRef2. The clamping voltage is 2.1 V.

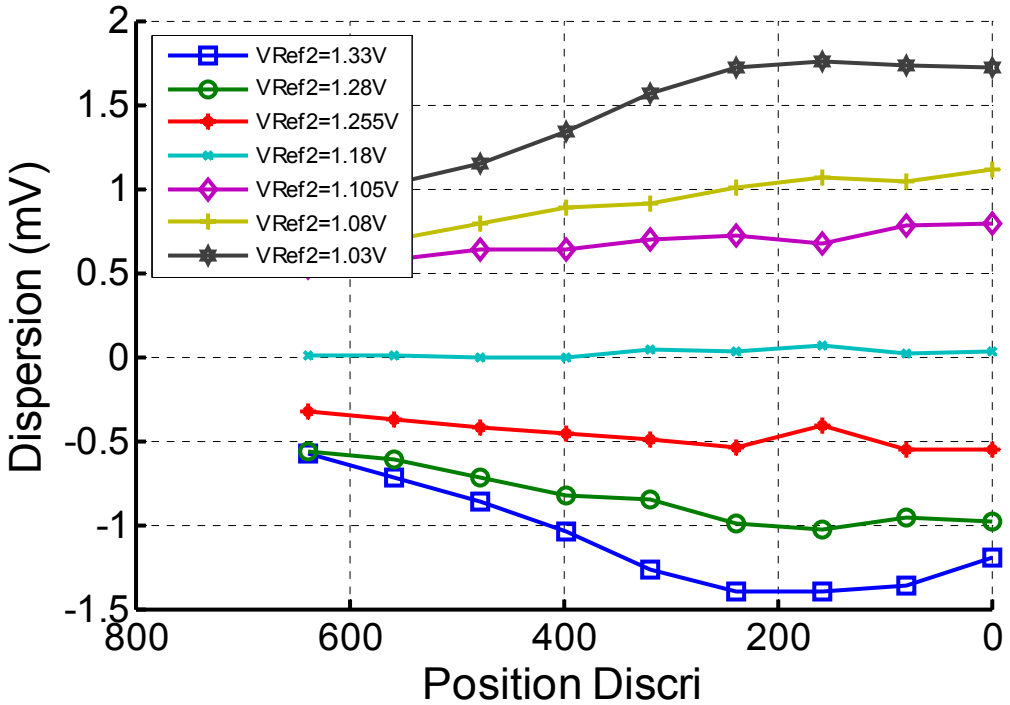


Figure 2-7-4-c: Evolution of the dispersion at V_X as a function of discriminator position for different values of the reference voltage VRef2. The clamping voltage is 2.1 V and the signal RD is delayed of 3 ns relative to the signal RD_b to eliminate the charge injection ε_1.

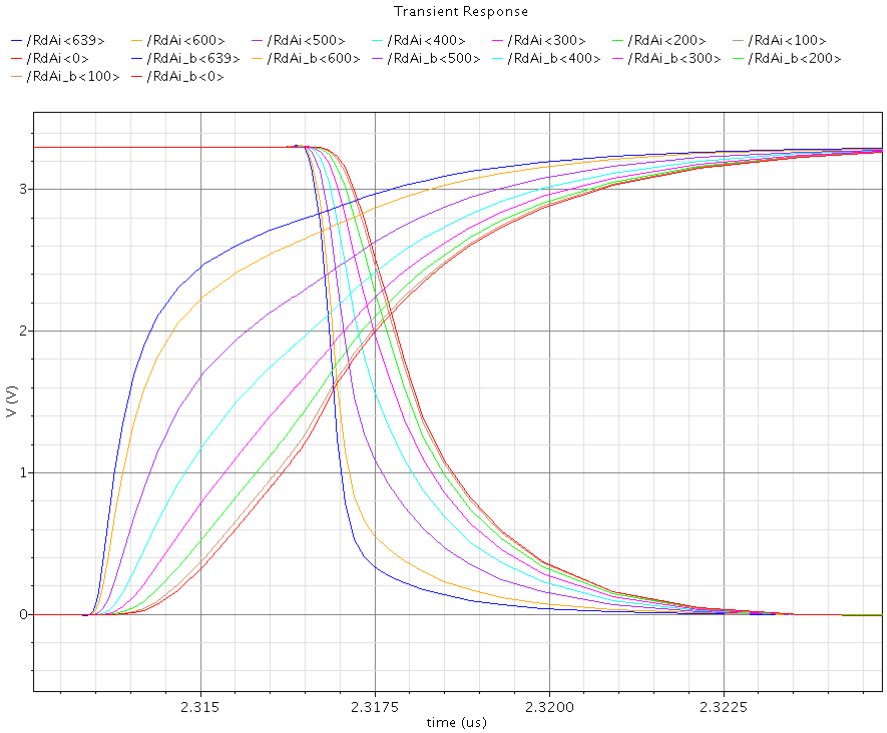
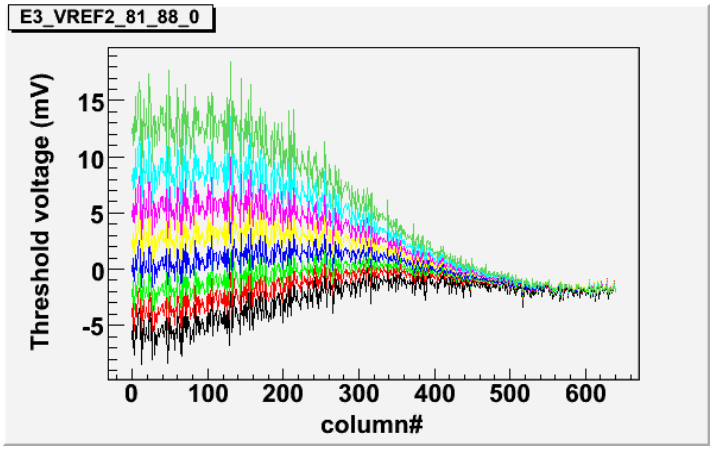


Figure 2-7-4-d: Evolution of the signals RD and RD_b after applying a delay of 3n on the signal RD at the source.



Chip E3 (parameter scan)

VREF2 = 81	0.852 V
VREF2 = 82	0.863 V
VREF2 = 83	0.873 V
VREF2 = 84	0.885 V
VREF2 = 85	0.895 V
VREF2 = 85	0.906 V
VREF2 = 86	0.916 V
VREF2 = 87	0.927 V

Figure 2-7-4-e: VREF2 scan by the BNL test team

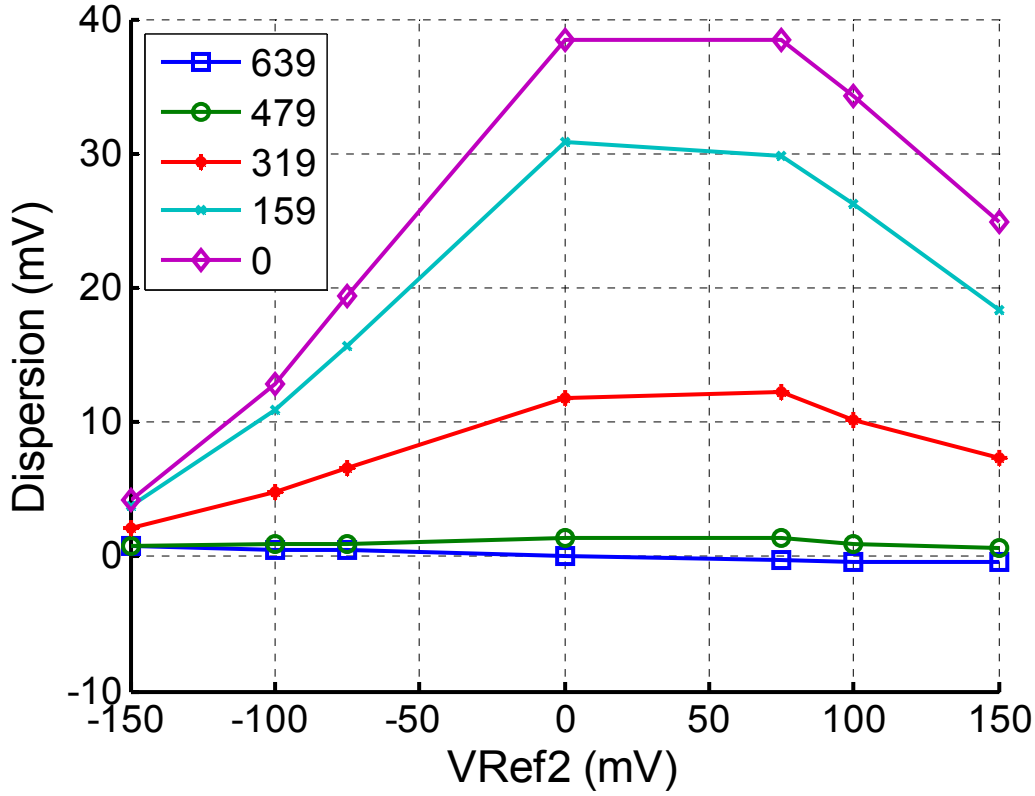


Figure 2-7-4-f: Evolution of the dispersion at V_X as a function of the variation of VRef2 (relative to the pixel common-mode) for selected discriminators in the raw. The clamping voltage is 2.1 V and the RD is not delayed.

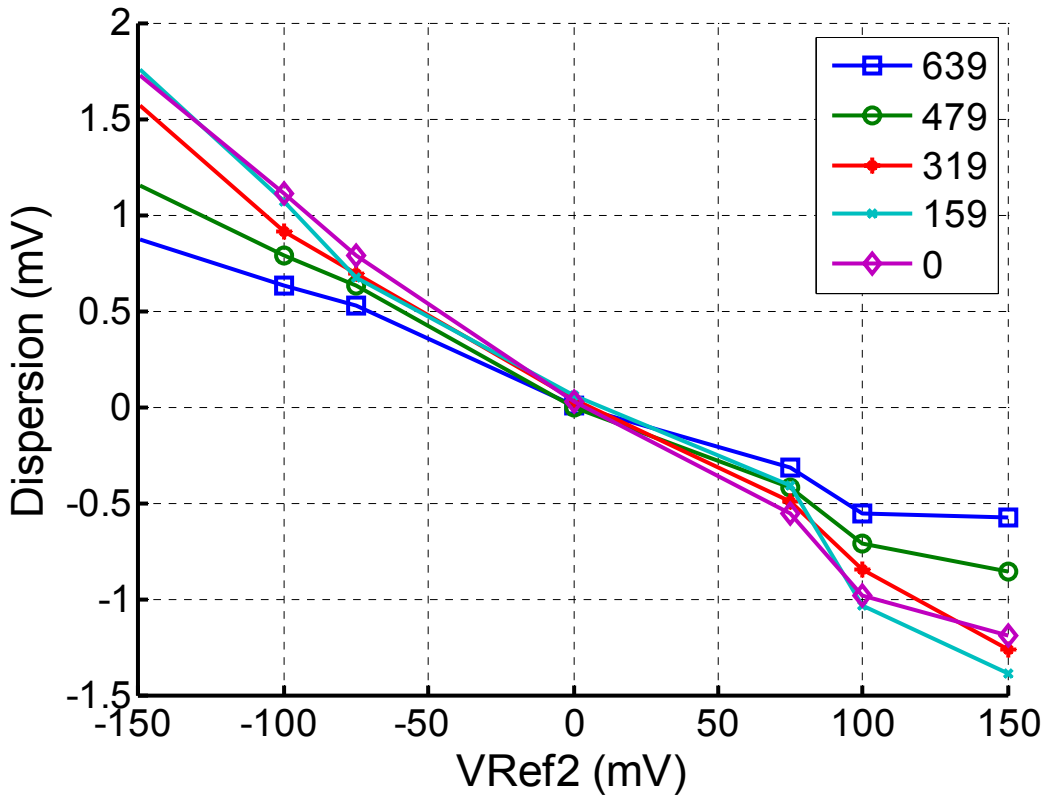


Figure 2-7-4-g: Evolution of the dispersion at V_X as a function of the variation of the voltage VRef2 for selected discriminators in the raw. The clamping voltage is 2.1 V and the signal RD is delayed of 3 ns relative to the signal RD_b to eliminate the charge injection ε_1.

We see that the shape of the figure 2-7-4-b is similar as the test measurement (see figure 2-7-4-e).

We see that the waveforms giving the dispersion at Vx as a function of the variation of the voltage VRef2 can have different shape. When the RD signal is delayed of 3 ns, the dispersion is quite linear with the voltage VRef2 (cf figure 2-7-4-g). When the signal RD is not delayed, the shape is different which looks like the shape of the gain (cf fig. 1-f).

The table 2-7-a and 2-7-b and the figures 2-7-4-h, i and j show the simulation of the discriminator in the 6 possible cases. The dispersion at the nodes V_X, V_Z and V_Y depend linearly with the voltage VRef2 for case 5 and 6 (same situation as figure 2-7-4-g). In cases 1, 2 and 4, we observe a shape closer of that of the figure 2-7-4-f.

case	Order of opening switches	VX	VZ	VY
1	S1, S3, S4	$-A_1\varepsilon_1+\varepsilon_3$	$-A_1A_2\varepsilon_1+\frac{A_3\Delta V_3}{(1+A_3)}+\varepsilon_4$	$-A_1A_2A_3\varepsilon_1-\frac{A_3\Delta V_3}{(1+A_3)}+A_3\varepsilon_4$
2	S1, S4, S3	$-A_1\varepsilon_1+\varepsilon_3$	$-A_1A_2\varepsilon_1+A_2\varepsilon_3+\frac{A_3\Delta V_3}{(1+A_3)}+\varepsilon_4$	$-A_1A_2A_3\varepsilon_1+A_2A_3\varepsilon_3-\frac{A_3\Delta V_3}{(1+A_3)}+A_3\varepsilon_4$
3	S3, S1, S4	ε_3	$-A_1A_2\varepsilon_1+\frac{A_3\Delta V_3}{(1+A_3)}+\varepsilon_4$	$-A_1A_2A_3\varepsilon_1-\frac{A_3\Delta V_3}{(1+A_3)}+A_3\varepsilon_4$
4	S4, S1, S3	$-A_1\varepsilon_1+\varepsilon_3$	$-A_1A_2\varepsilon_1+A_2\varepsilon_3+\frac{A_3\Delta V_3}{(1+A_3)}+\varepsilon_4$	$-A_1A_2A_3\varepsilon_1+A_2A_3\varepsilon_3-\frac{A_3\Delta V_3}{(1+A_3)}+A_3\varepsilon_4$
5	S3, S4, S1	ε_3	$\frac{A_3\Delta V_3}{(1+A_3)}+\varepsilon_4$	$-\frac{A_3\Delta V_3}{(1+A_3)}+A_3\varepsilon_4$
6	S4, S3, S1	ε_3	$A_2\varepsilon_3+\frac{A_3\Delta V_3}{(1+A_3)}+\varepsilon_4$	$A_2A_3\varepsilon_3-\frac{A_3\Delta V_3}{(1+A_3)}+A_3\varepsilon_4$

Table 2-7-a: Voltages at nodes VX, VZ and VY defined on the figure 2-2-a

case	Order of opening switches	VX	VZ	VY
1	S1, S3, S4	9.5mV	-31mV	494.5mV
2	S1, S4, S3	9.5mV	-31.2mV	497mV
3	S3, S1, S4	29.16nV	-12.3mV	240mV
4	S4, S1, S3	9.5mV	-29.9mV	484 mV
5	S3, S4, S1	-320nV	2.4uV	-48uV
6	S4, S3, S1	-345nV	169nV	-3.4uV

Table 2-7-b: Simulation results for VRef2 equal to 1.2 V

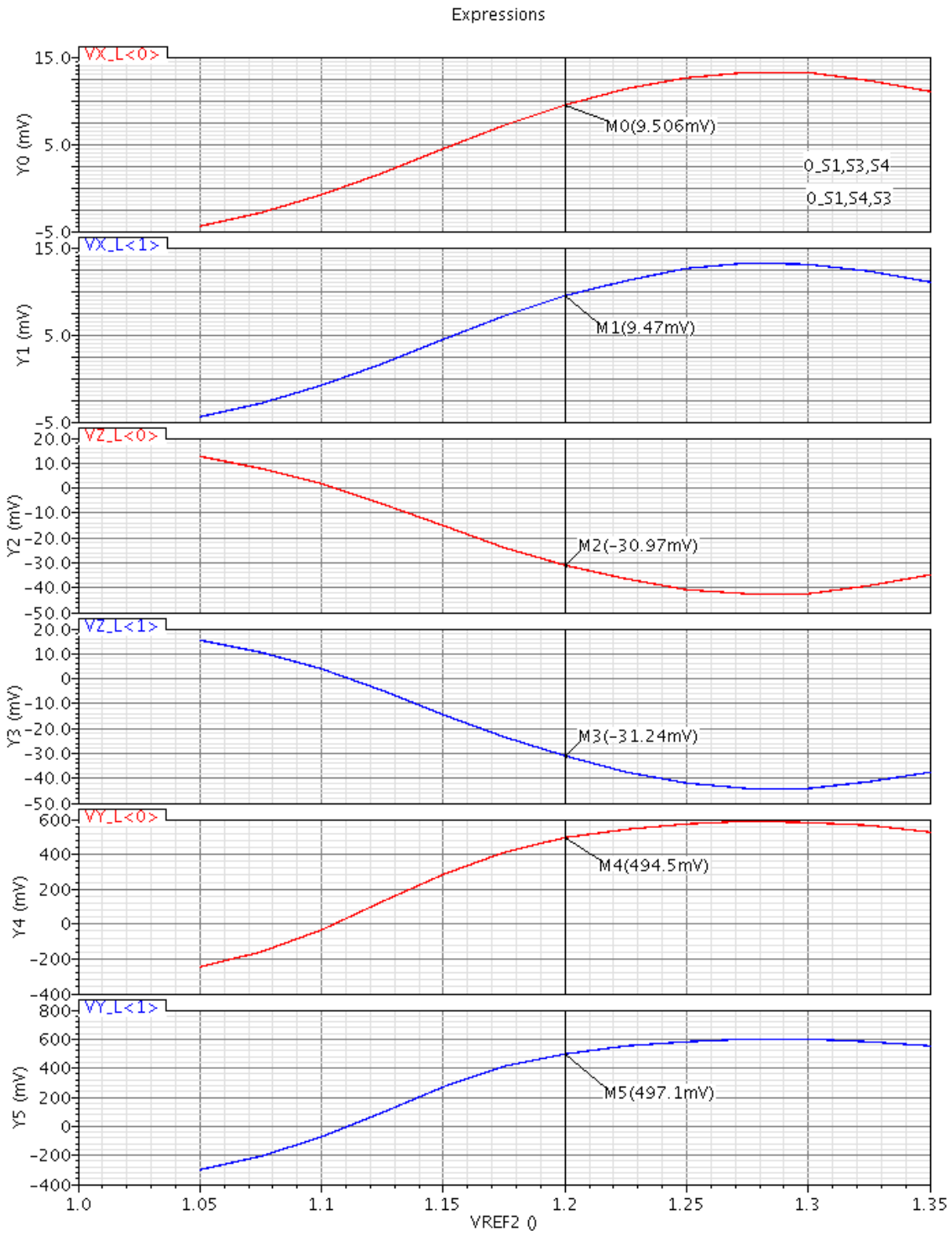


Figure 2-7-4-h: Case n°1 and 2

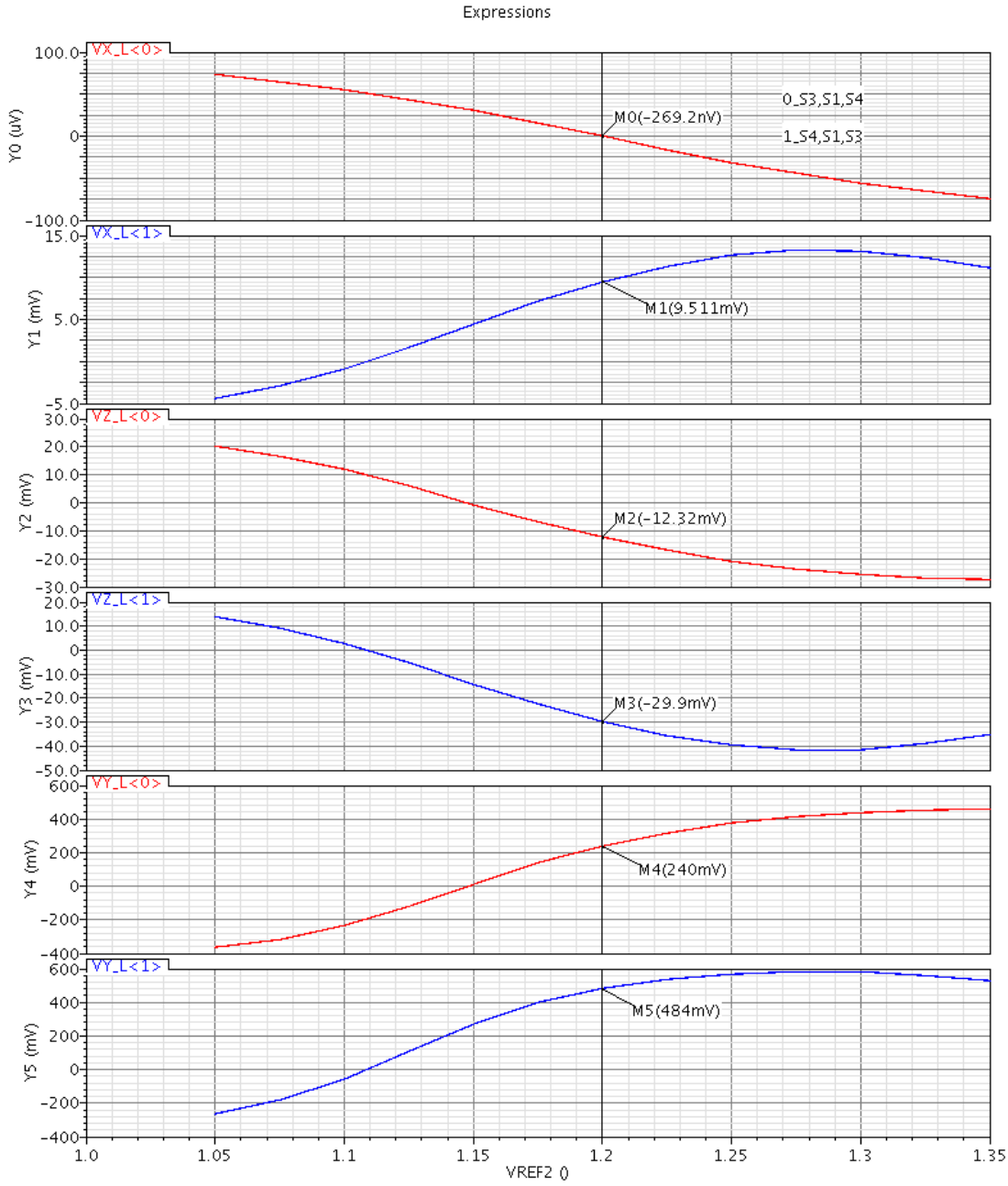


Figure 2-7-4-i: Case n°3 and 4

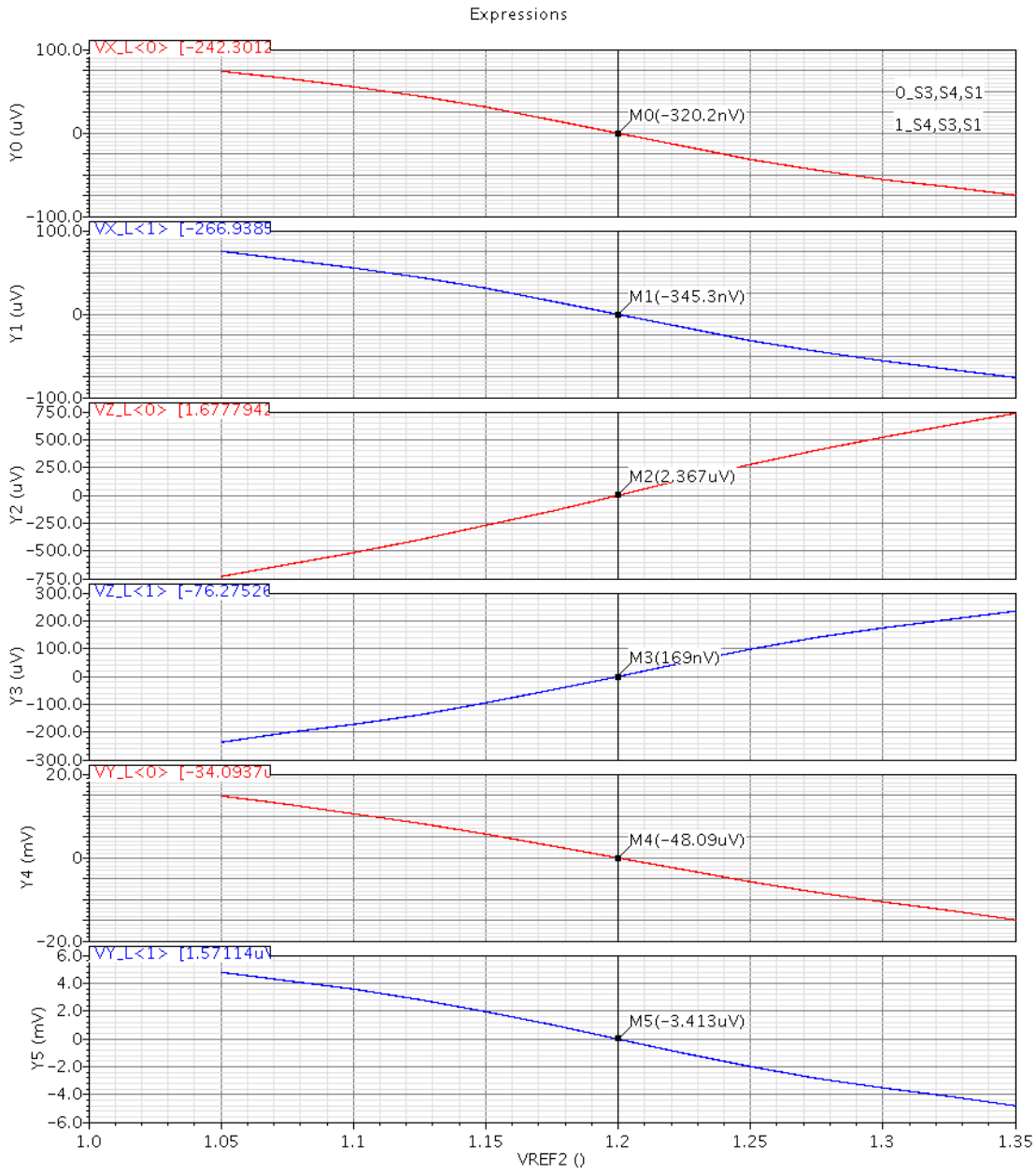


Figure 2-7-4-j: Case n°5 and 6

3- Conclusion

The column-level, low power, fully offset compensated multistage discriminator is well adapted to the readout of the active pixel.

This design has been implemented and tested in many successive medium size sensor prototypes (with a row of 128 discriminators).

For the large size sensor working at high pixel readout frequency (5 MHz), about 1000 discriminators work at the same time. It needed stable reference and clamping voltages. Consequently, the discriminator row has been segmented in four groups.

The timing diagram has been optimized to resolve the problem of threshold dispersion due to the effect of the long interconnects.

A resolution ~ < 1 mV can be expected at 5MHz pixel readout frequency in the Ultimate sensor.

The static power dissipation of the discriminator is 210 µW at 3 V power supply.

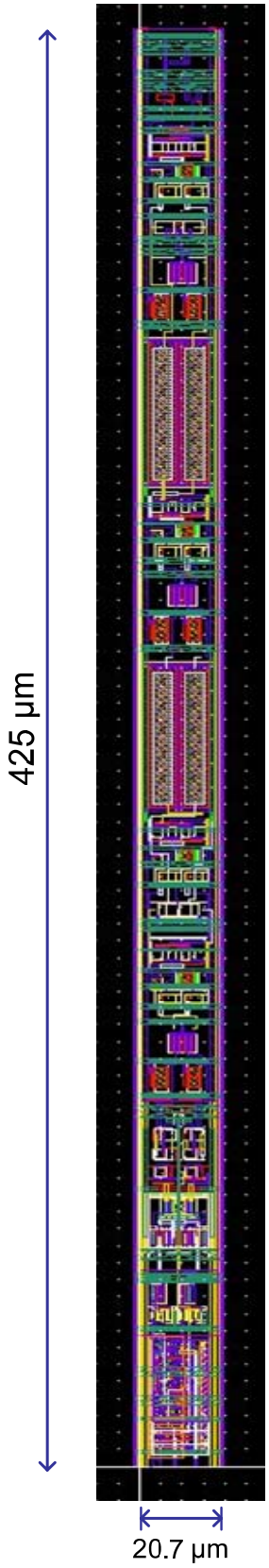


Figure 3: Layout of the discriminator