LG, MS 2006/10/08

HFT 2006 Beam test Readout and Hardware Status.

We report the hardware and readout status for the preparation of the 3 MIMOSTAR2 detector telescope to be tested in the STAR Beam run beginning in 2006.

Hardware on hand:
3 tested Motherboards v2.
2 tested daughtercards with 50 MHZ ADCs and JTAG connections.
3 MIMOSTAR2 detectors mounted to flex cables. 2 tested and working.
3 Stratix development boards.
3 DDL modules
4 RORC modules with fiber optic cables for testing.
Control PC with JTAG control for Altera, Xilinx and MIMOSTAR2.
DAQ PC with RORC installed.
Insertion hardware and electronics mounting hardware.
Cables for readout.

JTAG status:
The JTAG communication to the MIMOSTAR2 sensors in functional over two paths. We can configure the sensors via the control PC serial port and via firmware in the NIOS environment in the Stratix board. Some initial problems were traced to the need for drivers to strengthen the TCK JTAG signal. This appears to be due to input sensitivity in the MIMOSTAR2 JTAG receivers.

RDO status:
We have successfully driven the MIMOSTAR2 output signals though the signal path into the ADCs on the daughter cards at 50 MHz, digitized the signals and read out the data via chipscope. The data appears to be what we expect and has allowed us to perform tests on various cable types and configurations looking at induced noise. A report on this can be found at xxxx
In addition, we have successfully chained two MIMOSTARs on flex cables, configured both over JTAG and verified chip function from one multidrop LVDS clock line.

Firmware status:
The front end has been tested and we are able to store the ADC signals into the SRAM at 50 MHz. The firmware for reading full frame events has been written but not yet tested with the MIMOSTAR2s output. The firmware for CDS and cluster finding will be completed when Thorsten returns from Germany. The cluster gathering and event building firmware has been written and tested on the bench but not yet tested with MIMOSTAR2 output data. The firmware for sending data over the DDL / RORC link is under development.

Software status:

The event data format and basic control structure has been finalized and can be found here: http://www.lbnl.leog.org/rdo/Data_format_HFT.pdf Chinh Vu will produce a set of fake data files and Andrew Rose will write both the overall control shell and the online event displays.