LG, MS
2006/01/19

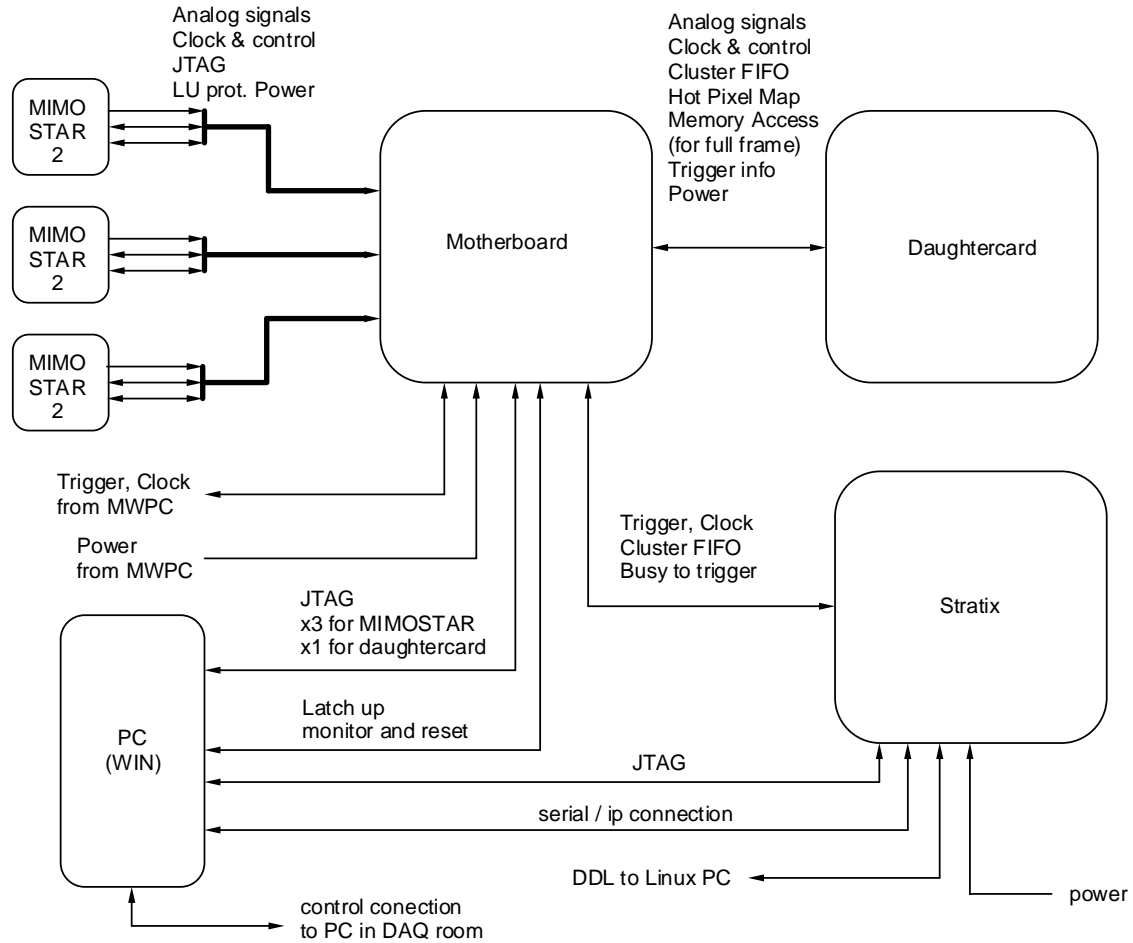HFT Development and Prototyping effort for the 2006-2007 STAR Run.

Our goal is to test functionality of a prototype MIMOSTAR2 detector in the environment at STAR in the 2006-2007 run at STAR. We anticipate gathering information on:

- Charged particle environment near the interaction region in STAR.
- Performance of our cluster finding algorithm.
- Performance of the MIMOSTAR2 sensors.
- Functionality of our tested interfaces to the other STAR subsystems.
- Performance of our hardware / firmware as a system.
- The noise environment in the area in which we expect to put the final HFT.

To realize this goal we are assembling a prototype telescope and the mechanical infrastructure and positioning system to allow us to place a 3 MMIMOSTAR2 detector telescope into the STAR magnet near the interaction region. This plan presents challenges in the mechanical, electronics, firmware and infrastructure aspects of assembling and integrating a prototype system into the STAR environment. The basic design of our system is shown below.

Electronics Hardware

Configuration: 3 separate MIMOSTAR2 chips on individual mounts in a telescope configuration. This system is controlled and read out into a motherboard mounted to a Stratix development board. Trigger and clock come from the MWPC cables as does power. This system is meant to be a functional test of our intended HFT readout system. This system is well described in the readout section of our proposal which can be found here http://www.lbnl.leog.org/RDO_section_HFT_proposal.pdf. A block diagram of the test system is shown below.

Analog signals
Clock & control
JTAG
LU prot. Power

Analog signals
Clock & control
Cluster FIFO
Hot Pixel Map
Memory Access
(for full frame)
Trigger info
Power

MIMO STAR 2

MIMO STAR 2

MIMO STAR 2

Motherboard

Daughtercard

Trigger, Clock
from MWPC

Power
from MWPC

JTAG
x3 for MIMOSTAR
x1 for daughtercard

Latch up
monitor and reset

Trigger, Clock
Cluster FIFO
Busy to trigger

Stratix

PC
(WIN)

JTAG

serial / ip connection

DDL to Linux PC

power

control conection
to PC in DAQ room

In this test, the basic data flow is as follows. Triggers are received from the STAR triggering system into the motherboard and implemented in the FPGA on the daughtercard. MIMOSTAR2 Configuration (JTAG), latch up protected power, clock, sync and reset are provided via shielded CAT-5 cables from the motherboard (the schematic can be found here http://www.lbnl.leog.org/rdo/mimostar2_mb_prelim_v4.pdf). In our configuration, the MIMOSTAR2s will be running in parallel with multidrop LVDS clock and only 1 mx first is brought out for synchronization. The analog signals and mxfirst are transferred from the MIMOSTAR2 detectors mounted on the flex PCBs (http://www.lbnl.leog.org/rdo/mimostar2_cable_sept_test_final.pdf) via the same CAT-5 cables back to the motherboard and routed to the daughtercard for ADC conversion, data resorting, CDS and cluster finding. The daughtercard schematic can be found here http://www.lbnl.leog.org/rdo/mimostar2_mb_prelim_v4.pdf. Cluster addresses or full frame data (raw or CDS) is then routed from the daughtercard through the motherboard into the Stratix development board and to our data acquisition linux PC via the CERN ALICE DDL / RORC modules. From the DAQ linux PC, the evets are built into the STAR event structure and/or into our own event files.

Hardware
The hardware used in this test consists of 3 MIMOSTAR2 detectors mounted on 25 micron kapton flex PCBs, a motherboard, daughtercard, stratix development board, DDL,

DAQ linux PC and configuration PC. A photograph of the assembled motherboard, daughtercard, Stratix development board and DDL, and of the assembled cable is shown below.
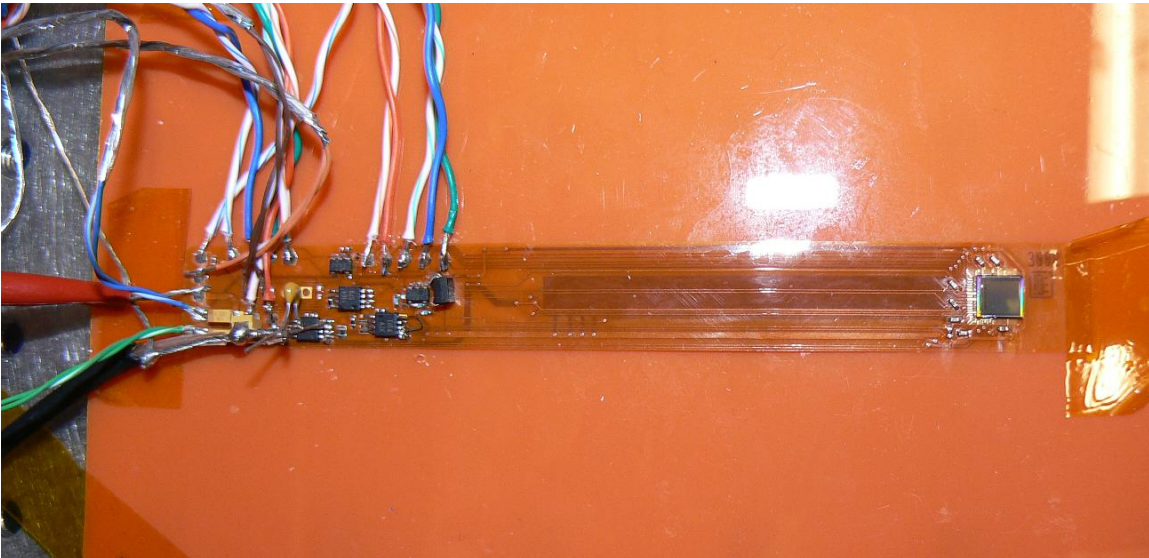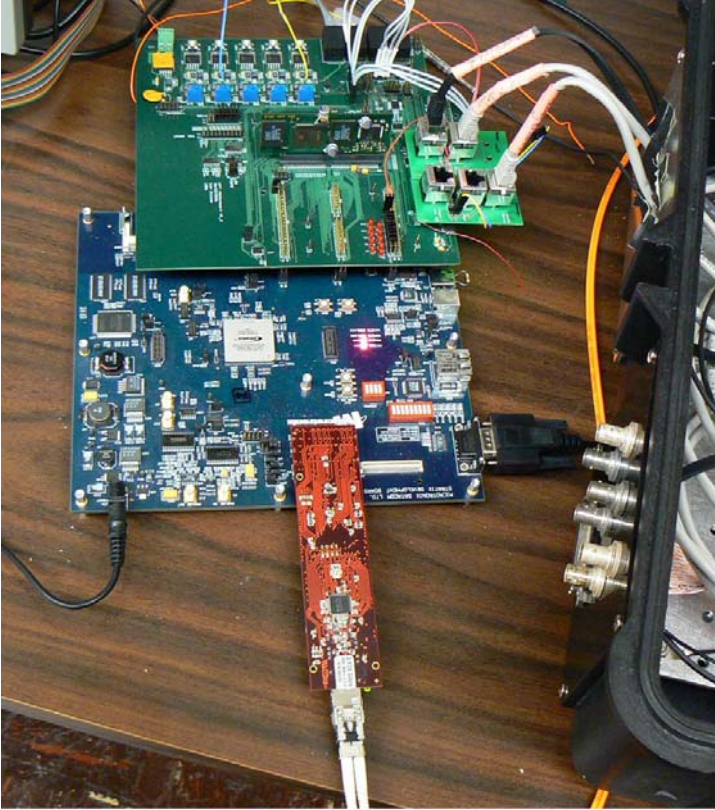
Firmware
The firmware required for this test includes most all of the functionality of the final firmware needed for the full detector. The following basic functionality is required:

Implemented on daughtercard
- Accept and respond appropriately to triggers in the STAR trigger system.
- SRAM memory controller
- 50MHz 12bit ADC serial interface
- Data re-sorter
- CDS
- Full frame readout
- Cluster finding
- Cluster FIFO building

Implemented on Stratix board
- Event building
- JTAG configuration of the chained MIMOSTAR2 chips from the Stratix board.
- Interface to control shell
- DDL control and interface
- Latch-up detection and remote reset

Integration

Some significant effort is required to insert this telescope into the STAR experiment close to the interaction point. An insertion system, electronics control box and cooling system have been designed and fabricated. The basic system is shown below:
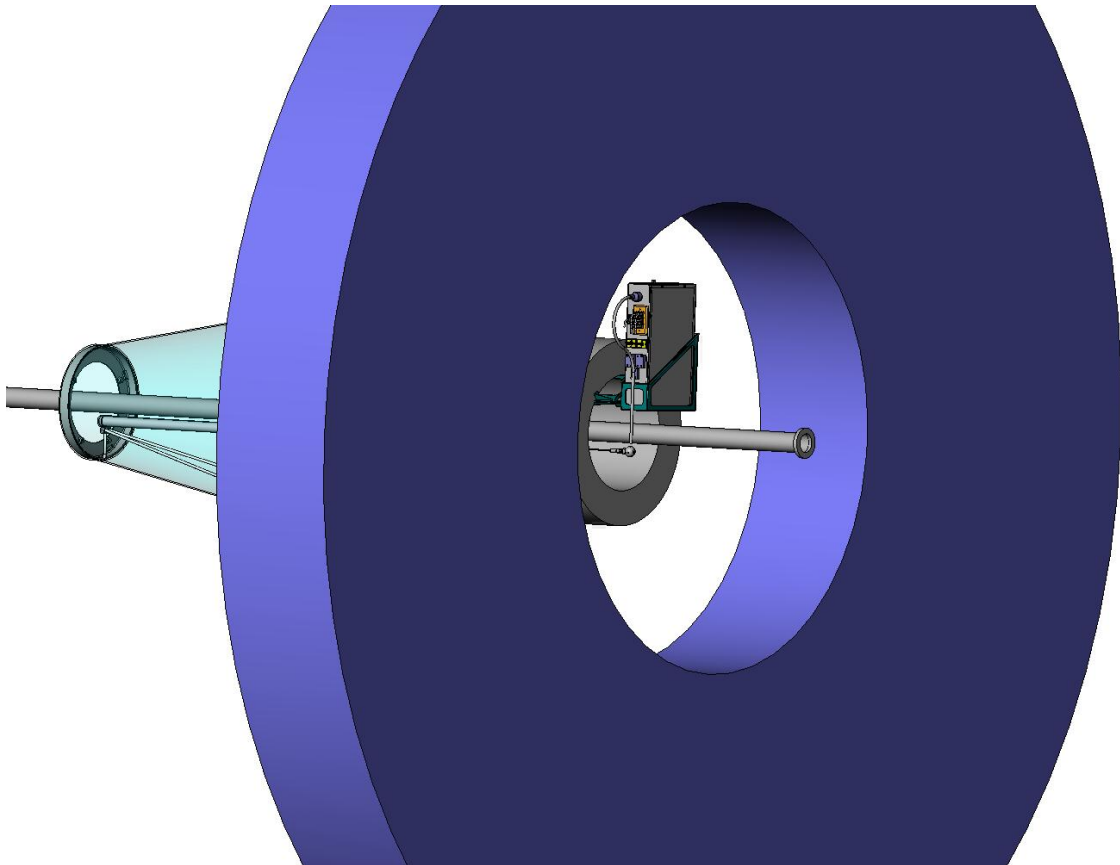
In this diagram, the insertion tube that carries our telescope to a point near the interaction region is shown with respect to the STAR magnet pole tip. The electronics box is mounted in the hole in the pole tip above the beam pipe. Cooling is provided by a vacuum system that draws air past the MIMOSTAR2 detectors through a tube that also carries our signal cables. The MIMOSTAR2 detectors on their flex cables will be mounted into a positioning assembly (shown below) that will hold position and protect the telescope as it is slid into the insertion tube.

Current Status

Electronics Hardware / Hardware – All required PCBs, cables, computers, etc are in hand. We have are currently working on some problems involving noise in our electronics setup. We hope to resolve this shortly and assemble and test the telescope setup in a beam run at the ALS at LBL before moving the system to BNL for the beam test.

Firmware – The required functionality listed above has been implemented and tested in the ways possible before a working set of detectors is used.

Integration – The insertion tube and electronics box are in place at BNL as is the cooling system, DAQ and control PCs. Final assembly and testing of the telescope is required before we can do further testing.