

MimoStar1

User Manual

MimoStar1 User Manual v1.0

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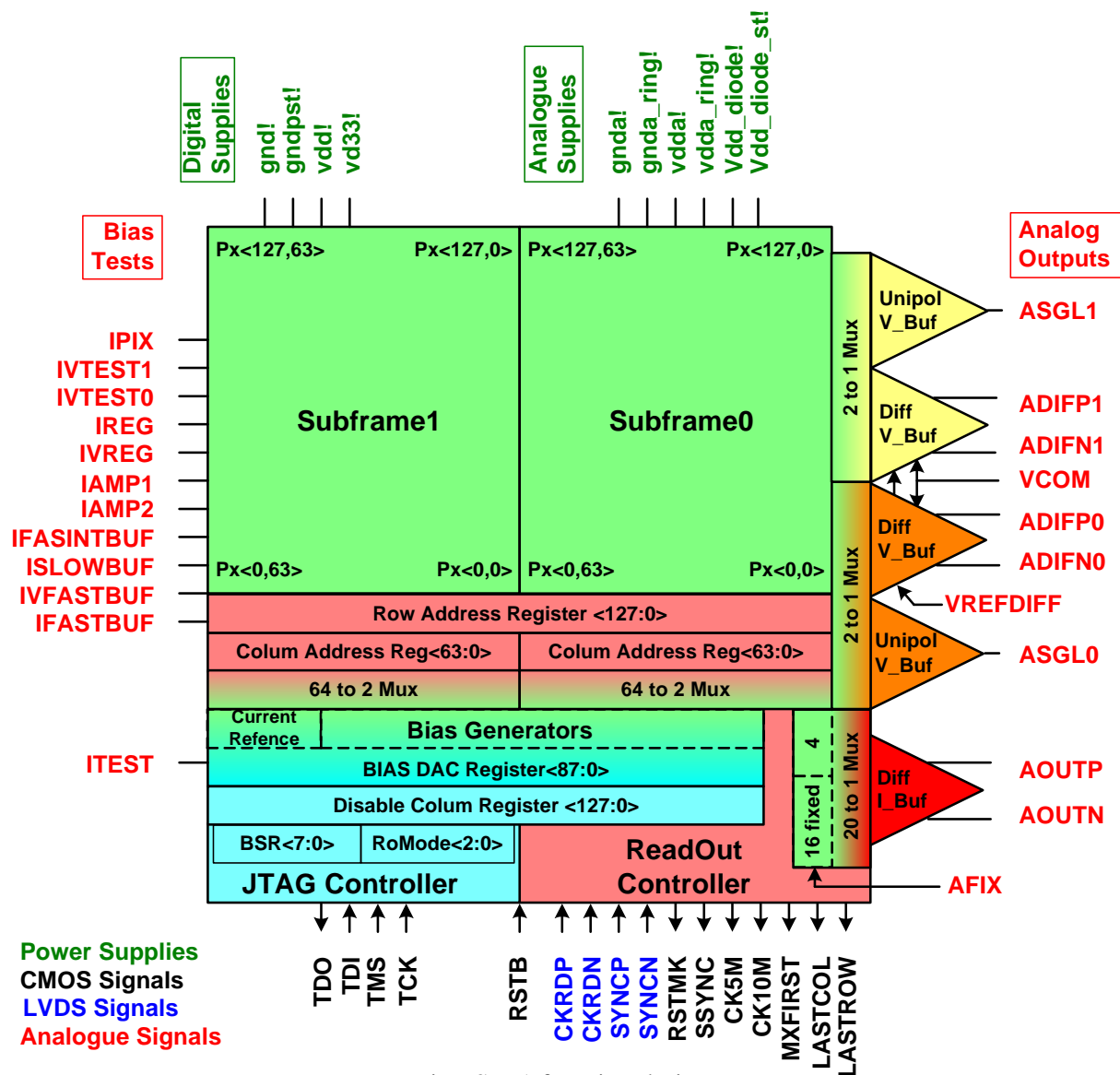
MimoStar		
Version	Date	Description
1	Submitted 5/07/04	First Version int TSMC 0.25 via MOSIS. In fab 23 rd /08/04

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1 Introduction

MimoStar1 is a Monolithic Active Pixel Sensor prototype dedicated to vertex particle tracking in a future update of the STAR vertex detector. The matrix is composed by 128 x 128 pixels of 30 μm pitch and based on self biased diode architecture. It is organised in 2 matrices, or subframes, of 128 lines x 64 columns, accessed in parallel during the readout. Actually Mimostar1 is a downsized prototype which emulates the future final circuit. This one is foreseen with 640 x 640 pixels organised in 10 subframes of 640 lines x 64 columns. The addressing of each subframe is sequential and starts from the upper left pixel up to the lower right pixel. Analogue data are extracted via a selectable set of analogue buffers. One can choose between the parallel outputs or the serial output.

- Parallel output
Two types of output voltage buffers are provided; unipolar and differential Each subframe have its dedicated buffer running at a readout speed from 5 up to 10 MHz
- Serial output
The serialised, multiplexed, data of the 2 pixel subframes are driven out via a differential current output buffer. Its readout speed should be from 50 up to 100 MHz.



MimoStar1 functional view

Does not correspond to the floorplan; neither for the core, neither for the pad ring



MimoStar1 is very simple to operate.

- Power On Reset or Reset
- Setup of the chip

It is performed with programmable registers accessed via an embedded slow control interface. It consists to:

- Load the DACs which bias the analogue blocks
- Select the serial or the parallel analogue outputs
- Readout of the chip
 - The readout starts when the input "SYNC" LVDS token signal is sampled by the readout clock
 - After a latency of few clock cycles, analogue signals appear on the selected output(s)
 - Digital maker outputs are available for the control of the readout process
 - Pixels are sequentially read in a specific order explained later in the document
 - Successive pixel frames are read until the readout clock is stopped
 - A frame resynchronisation can be performed at any time by setting up the "SYNC" token again

2 Control Interface

The control interface of MimoStar1 complies with the Boundary Scan, JTAG, IEEE 1149.1 Rev 1999 standard. It allows the access to the internal registers of the chip like the bias register and the analogue output selection register.

On Power-On-Reset, an internal reset for the control interface is generated. The finite state machine of the Test Access Port (TAP) of the controller enters in the Test-Logic-Reset state and the ID register is selected.

Remarks on the Differential Voltage Output Buffers:

MimoStar1 has been designed in order to be fully adjustable via the control interface. Nevertheless 2 functionalities still need to be fixed with a voltage level via 3 pads.

- AFIX is necessary to the Differential Current Output Buffer
- VCOM and VREFDIFF are for the selection and for the bias of the Differential Voltage Output Buffers

2.1 JTAG Instruction Set

The Instruction Register of the JTAG controller is loaded with the code of the desired operation to perform or with the code of the desired data register to access.

Instruction	5 Bit Code	Selected Register	Notes
EXTEST	01	BSR	JTAG mandatory instruction
HIGHZ	02	BYPASS	JTAG optional instruction
INTTEST	03	BSR	JTAG optional instruction
CLAMP	04	BYPASS	JTAG optional instruction
SAMPLE_PRELOAD	05	BSR	JTAG mandatory instruction
BIAS_GEN	10	BIAS register	User instruction
DIS_COL	11	Disable Columns	User instruction
ID_CODE	12	(1)	Reserved - JTAG optional instruction
NU1	13	(1)	Reserved, Not Used
NU2	14	(1)	Reserved, Not Used
NU3	15	(1)	Reserved, Not Used
NU4	16	(1)	Reserved, Not Used
RO_MODE	17	Read Out Mode	User instruction
BYPASS	1F	BYPASS	JTAG mandatory instruction

(1) Instruction codes implemented but not the corresponding registers. To be fixed in the next version.

2.2 JTAG Register Set

JTAG registers are implemented with a Capture/Shift register and an Update register. JTAG standard imposes that the last significant bit of a register is downloaded/shifted first.

Register Name	Size	Access	Notes
INSTRUCTION REG	5	R/W	Instruction Register
BYPASS	1	R Only	

BSR	9	R/W	
BIAS_GEN	88	R/W	Previous value shifted out during write
RO_MODE	3	R/W	Previous value shifted out during write
DIS_COL	128	R/W	
ID_REG, NU1, NU2, NU3, NU4	0	-	Not implemented. For future use

2.2.1 Instruction Register

The Instruction register is a part of the Test Access Port Controller defined by the IEEE 1149.1 standard. The Instruction register of MimoStar1 is 5 bits long. On reset it is set with the ID_CODE instruction. When it is read the 2 last significant bits are set with the markers specified by the standard, the remaining bits contain the current instruction.

X	X	X	1	0
---	---	---	---	---

2.2.2 Bypass Register

The Bypass register consists of a single bit scan register. It is selected when its code is loaded in the Instruction register, during some actions on the BSR and when the Instruction register contains an undefined instruction.

2.2.3 Boundary Scan Register

The Boundary Scan Register, according with the JTAG instructions, tests and set the IO pads. The MimoStar1 BSR is 9 bits long and allows the test of the following input and output pads

Bit #	Corresponding Pad	Type	Signal	Notes
8	LVDS CkRdP/CkRdN	Inputs	CkRd	Resulting CMOS signal after LVDS Receiver
7	LVDS SyncP/SyncN	Inputs	Sync	Resulting CMOS signal after LVDS Receiver
6	SSync	Output	SSync	
5	Ck5M	Output	Ck5M	
4	Ck10M	Output	Ck10M	
3	RstMk	Output	RstMk	
2	LastRow	Output	LastRow	
1	LastCol	Output	LastCol	
0	MxFirst	Output	MxFirst	

2.2.4 BIAS_DAC Register

The BIAS_DAC register is 88 bits large; it sets simultaneously the 11 DACs registers.

As show bellow these 8-bit DACs set voltage and current bias.

After reset the register is set to 0, this fixed the minimum power consumption of the circuit.

The current values of the DACs are read while the new values are downloaded during the access to the register.

An image of the value of each DAC can be measured on its corresponding test pad.

Bit #	DAC #	DAC Name	DAC purpose	Test Pin
88-81	DAC10	I4PIX	Pixel source follower bias	IPIX
80-72	DAC9	V4TEST1	Test Level, emulates a pixel output	IVTEST1
71-64	DAC8	V4TEST0	IDEM	IVTEST0
63-56	DAC7	V4REG	Voltage regulator bias of the Columns Amplifiers	IVREG
55-48	DAC6	I4REG	IDEM	IREG
47-40	DAC5	I4AMP1P/1N	Bias of the group of Columns Amplifier	IAMP1
39-32	DAC4	I4AMP2	IDEM	IAMP2
31-24	DAC3	I4FASTINTBUF	Bias of the Fast Intermediate Buffer	IFASTINTBU F
23-16	DAC2	I4SLOWBUF	Bias of the Unipolar Voltage Output Buffer	ISLOWBUF
15- 8	DAC1	V4FASTBUF	Bias of the Differential Current Output Buffer	IVFASTBUF
7- 0	DAC0	I4FASTBUF	IDEM	IFASTBUF

2.2.5 RO_Mode Register

The RO_Mode register is 3 bits large; it allows the user to select the type of readout for the chip.

- Test mode versus normal mode
- Parallel analogue outputs versus serial output
- Amplification gain of 3 versus 5 for the serial analogue output buffer

Bit #	Bit Name	Purpose	Default value
2	EnaGain3	Select gain 3 for the serial differential output buffer	0 → Gain 5
1	Ena10MHz	Select the 10 MHz voltage output buffers. Selection of the differential buffers is done via the VCOM pad	0 → Diff. Current Output Buffer VCOM = 0V → Unipolar Buffer only VCOM = Vdd → Uni. + Diff. Buffer
0	EnaTstCol	Test Mode: Select the 2 Test Levels, IVTEST1 and IVTEST0, which emulate a pixel output	0 → Normal mode

2.2.6 DIS_COL Register

The DIS_COL register is 128 bit wide. The purpose of this register is to disable the column current sources if a short circuit is suspected on a specific column. During the readout, even if a current source is disabled the corresponding column is selected, i.e. no columns are skipped. Obviously, the signal of the corresponding pixel has no signification.

The default value of the DIS_COL register is 0; it means that all current sources can be activated by the readout logic. Setting a bit to 1 disables the corresponding current source. In MimoStar1, the column<127> is on the left hand side while column<0> is on the right hand side. The organisation of the chip in 2 subframes of 64 columns has no matter to do with the DIS_COL register.

127 (Msb)	0 (Lsb)
DisCol<127>	DisCol<0>

2.2.7 DEV_ID Register

The Device Identification register is not implemented yet. When selected by the ID_CODE instruction or after a reset no real data are shifted, a 0 value takes place on TDO, the JTAG serial output of the chip.

3 Running MimoStar1

The following steps describe how to operate Mimostar1

3.1 After reset

On RSTB active low signal:

- All BIAS registers are set to the default value, i.e. 0
- DIS_COL is set to 0
- RO_Mode is set to 0
- JTAG state machine in Test-Logic-Reset state
- JTAG ID_CODE instruction is selected

Then the bias, register have to be loaded.

The same for the RO_MODE and DIS_COL registers if the running conditions differ from defaults.

Finally the readout can be performed either in normal mode or in test mode.

3.2 Biasing MimoStar1

The BIAS_DAC register has to be loaded before operating MimoStar1.

The 11 DACs which constitute this register are built with the same 8 bits DAC current generator which has a 1 μ A resolution. Specific interfaces like current mirror for current sourcing or sinking and resistors for voltages, customise each bias output. The following table gives the hexadecimal codes to download in order to obtain the nominal settings.

DAC Name	Value ₁₆	Value ₁₀	Internal	Output	Unit	Digital Output	Resolution
----------	---------------------	---------------------	----------	--------	------	----------------	------------

			current- μ A	t value		Range	
I4PIX	40	64	64	51.6	μ A	0 – 255	0.8 μ A
V4TEST1	82	130	130	1.42	V	0 – 165	10.5 mV
V4TEST0	72	114	114	1.25	V	0 – 165	10.5 mV
V4REG	2D	45	45	2	V	0 – 185	10.5 mV
I4REG	40	64	64	102	μ A	0 – 255	1.6 μ A
I4AMP1P/1N	40	64	64	41	μ A	0 – 255	0.63 μ A
I4AMP2	3A	58	58	31	μ A	0 – 255	0.515 μ A
I4FASTINTBUF	40	64	64	103.6	μ A	0 – 255	1.6 μ A
I4SLOWBUF	40	64	64	51.5	μ A	0 – 255	0.8 μ A
V4FASTBUF	4A	74	74	816	mV	0 – 165	10.5 mV
I4FASTBUF	44	68	68	68	μ A	0 – 255	1 μ A

3.2.1 BIAS_DAC Register Format

Bit range	87 – 80	79 - 72	71 - 64	63 - 56	55 - 48
DAC Name	I4PIX	V4TEST1	V4TEST0	V4REG	I4REG
47 - 40	39 - 32	31 - 24	23 - 16	15 - 8	7 - 0
I4AMP1P/1N	I4AMP2	I4FASTINTBUF	I4SLOWBUF	V4FASTBUF	I4FASTBUF

3.3 Setting the Readout_Mode Register

After reset, the default value of the Readout_Mode register, as shown in the JTAG Register Set paragraph, allows the following readout conditions:

Register value (binary)	Read Out Mode
000	Normal serial data with output gain=5
100	Normal serial data with output gain=3
001	Test serial data with output gain=5
101	Test serial data with output gain=3
X10	Normal parallel data
X11	Test parallel data

Remember that the selection of the differential voltage buffers is done via the VCOM pad.

- VCOM =0 V \rightarrow Unipolar Buffer only
- VCOM =2.5 V \rightarrow Unipolar and Differential Buffers

3.4 Readout

Once JTAG registers have been loaded, the readout of MimoStar1 can initiate.

The readout starts at the first rising clock edge after the "SYNC" signal disappears. It is confirmed by the digital makers RstMk, SSync.

After a latency of 39 clock cycles, analogue signals appear on the selected output(s).

Two types of signal can be generated in serial or in parallel mode; normal pixel signal or test signal.

This gives 4 different formats of data

- Normal Serial Format
- Normal Parallel Format
- Test Parallel Format
- Test Serial Format

Some output makers, not related to a specific format, inform about the synchronisation of the chip.

- Ck10MHz Clock output: CKRD/10 \rightarrow 10 MHz for 100MHz
- Ck5MHz Clock output: CKRD/5 \rightarrow 5 MHz for 100MHz
- MxFirst On the basis of the serial format; Active during odd pixel selection of the subframes
- LastCol Last column of the current row is selected
- LastRow Last row of the frame is selected

3.4.1 Normal data format

In order to improve the readout speed Mimostar1 is organized in subframes, i.e. 2 subframes for this current prototype and 10 for the foreseen full-size version.

During the readout, the 2 subframes of Mimostar1 are accessed in parallel. For each subframe the addressing is sequential from the upper left pixel up to the lower right pixel. The pixel coordinate format is Px<Line, Column>. Thus for each subframe the upper left pixel is Px<127, 63> while the lower right is Px<0, 0>.

3.4.1.1 Serial Mode

The serial mode consists to read successively one pixel of each subframe and then turning back to the first subframe in order to read its next pixel. Even if Mimostar1 is a downsized prototype of 2 subframes the serial strategy has been maintained for 10. This implies for the serial format 8 dummy values on 10 analogue data. This dummy value is fixed via the AFIX pad.

For Mimostar1, the left hand side subframe is named Sf1 and the right hand side is Sf0 while the dummy values generated in place of the 8 non-existing subframes are named from Dv7 to Dv0.

Thus the normal data stream in serial mode has the following format:

```
Sf1Px<127,63>, Sf0Px<127,63>, Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Px<127,62>, Sf0Px<127,62>, Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
.....
Sf1Px<127,0>, Sf0Px<127,0>, Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Px<126,63>, Sf0Px<126,63>....., Sf1Px<126,0>, Sf0Px<126,0>
Sf1Px< 0,63>, Sf0Px< 0,63>....., Sf1Px< 0,0>, Sf0Px< 0,0>
```

3.4.1.2 Parallel Mode

There is one output buffer per subframe: thus the Normal Parallel Mode data stream format for each output is:

```
Px<127,63>, Px<127,62>.....,Px<127,0>
Px<126,63>.....,Px<126,0>
Px< 0,63>.....,Px< 0,0>
```

3.4.2 Test data format

During the test mode the pixel matrix is not connected to the multiplexing electronic. In place, two test levels V4TEST1 (V1), V4TEST0 (V0) are available. They emulate two pixel level outputs. They are adjustable via 2 DACs. Even and odd columns are alternatively connected to one of them. This pattern allows seeing the output signal changing when the readout shifts from one column (pixel) to the other column (pixel).

3.4.2.1 Serial Mode

Testl data stream in serial mode has the following format:

Sf1V1, Sf0V0, Sf1V0, Sf0V1, Sf1V0, Sf0V1, Sf0V1, Sf0V0, Sf1V1, Sf0V0, Sf1V0, Sf0V1, Sf1V0, Sf0V1, Sf0V1, Sf0V0...

3.4.2.2 Parallel Mode

There is one output buffer per subframe: thus the Test Parallel Mode data stream format per output is:

Subframe 1: **V1, V0, V0, V1, V1, V0, V0, V1...**

Subframe 0: **V0, V1, V1, V0, V0, V1, V1, V0...**

3.5 Successive frames and resynchronisation

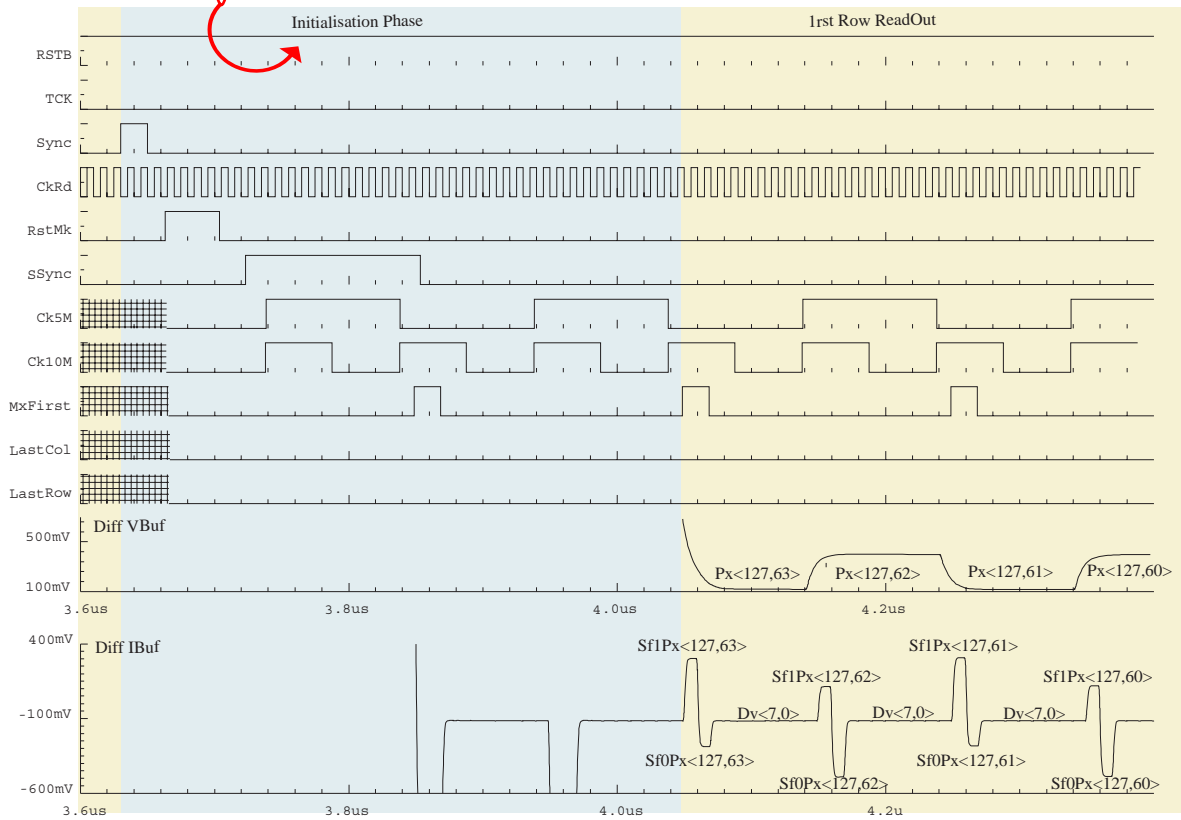
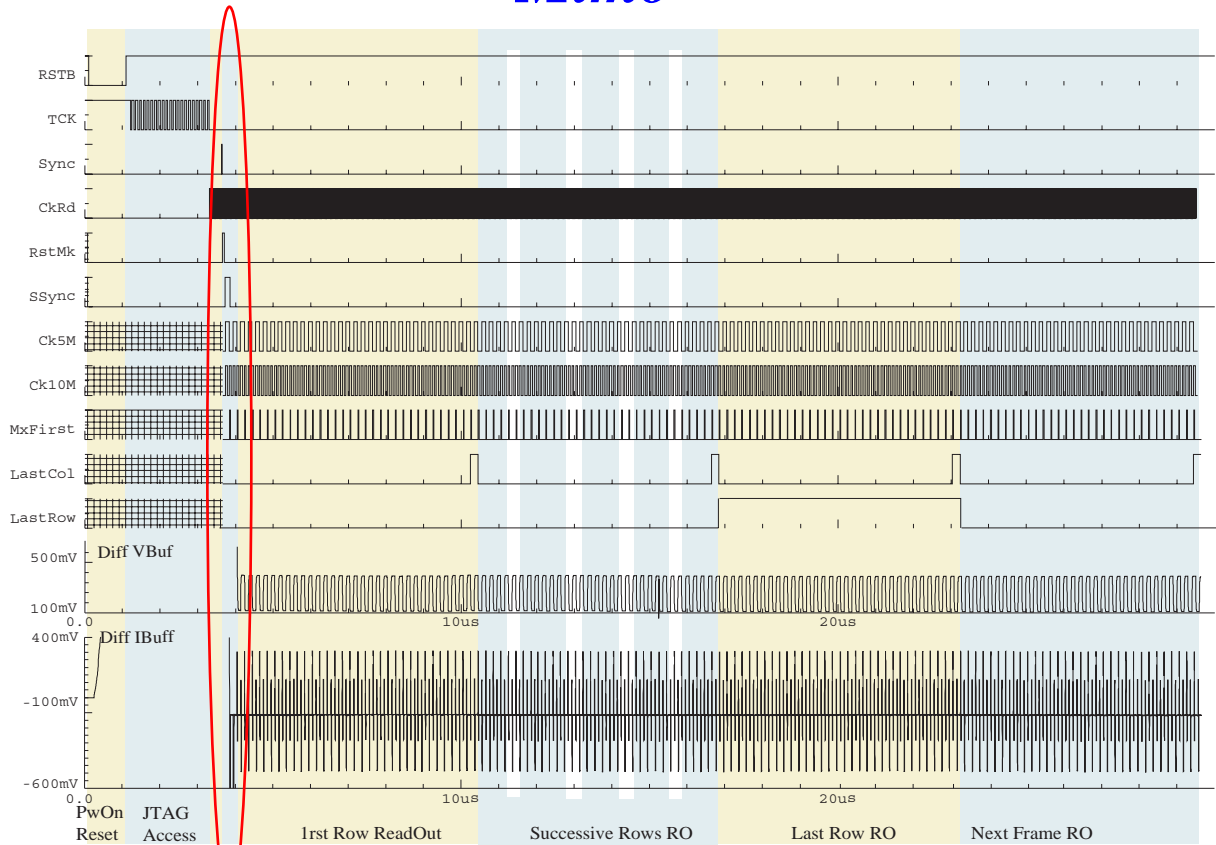
Successive pixel frames are read until the readout clock is stopped

A frame resynchronisation can be performed at any time by setting up the "SYNC" token again.

3.6 MimoStar1 Chronogram

The following chronogram describes a typical access to Mimostar1; Reset, JTAG download sequence and then the readout of the chip. This one starts with the initialisation phase followed by the successive row readouts as showed in the zoom.

The two main analogue outputs, parallel differential voltage output and serial differential current output are displayed like running together which is not the case (conf. Readout_Mode reg.). The differential current buffer is loaded with 2 x 100 Ω.



3.7 Main Signal Specifications

	Parameter	Typical Value	Notes
INIT	RSTB Pulse Width	>1 μ S	Active Low, Asynchronous Power on Reset
JTAG	TCK Frequency	10 MHz	Boundary Scan Clock
	TMS Setup/Hold Time	~10 nS	Boundary Scan Control Signal
	TDI Setup/Hold Time	~10 nS	Boundary Scan Serial Data In
READOUT	CKRD Frequency	Up to 100 MHz	Readout Clock LVDS signal
	CKRD Duty Cycle	50%	
	SYNC Setup/Hold Time	5 nS	Chip Initialisation, LVDS signal. Starts after falling edge on 1rst CKRD sampling
Differential Current Buffer (1)	Input Dynamic range	300 up to 1.3 V	
	Rise time	2 nS	@ 10-90%, for fully input dynamic range
	Fall time	2 nS	Simulated with $Z_{load} = 2*100 \text{ Ohm}$ and $2*5\text{pF}$
	Bandwidth	230 MHz	@ -3 dB
	Transconductance gain	6 mS	
	Output Current Range	-3, 3 mA	
AFIX	Bias value	1.5 V	Serial Output Buffer Dummy Data
Differential Voltage Buffer (2)	Rise time	20 nS	@ 10-90%
	Fall Time	20 nS	
	Bandwidth	20 MHz	@ -3 dB
	Capacitance load	1 pF	
VDIFFREF	Bias value	1.35 V	Bias of the Diff.Voltage Buffers
Unipolar Buffer (3)	Rise/ fall time	10 nS	@ 10-90%, Full analog chain simulated with load capacitance of 10pF
	Fall Time	10 nS	
	Capacitance load	10 pF	

Note 1: The differential current output buffer can be modelled as an ideal current source. Its performances in terms of raising and falling times are limited by its load's time constant ($R_{load} \times C_{load}$)

Note 2: This buffer has not been optimised with the whole analogue chain. Instability may occur for $C_{load} > 5 \text{ pF}$

Note 3: Simple source follower

4 Pad Ring

The pad ring of Mimostar1 is build with

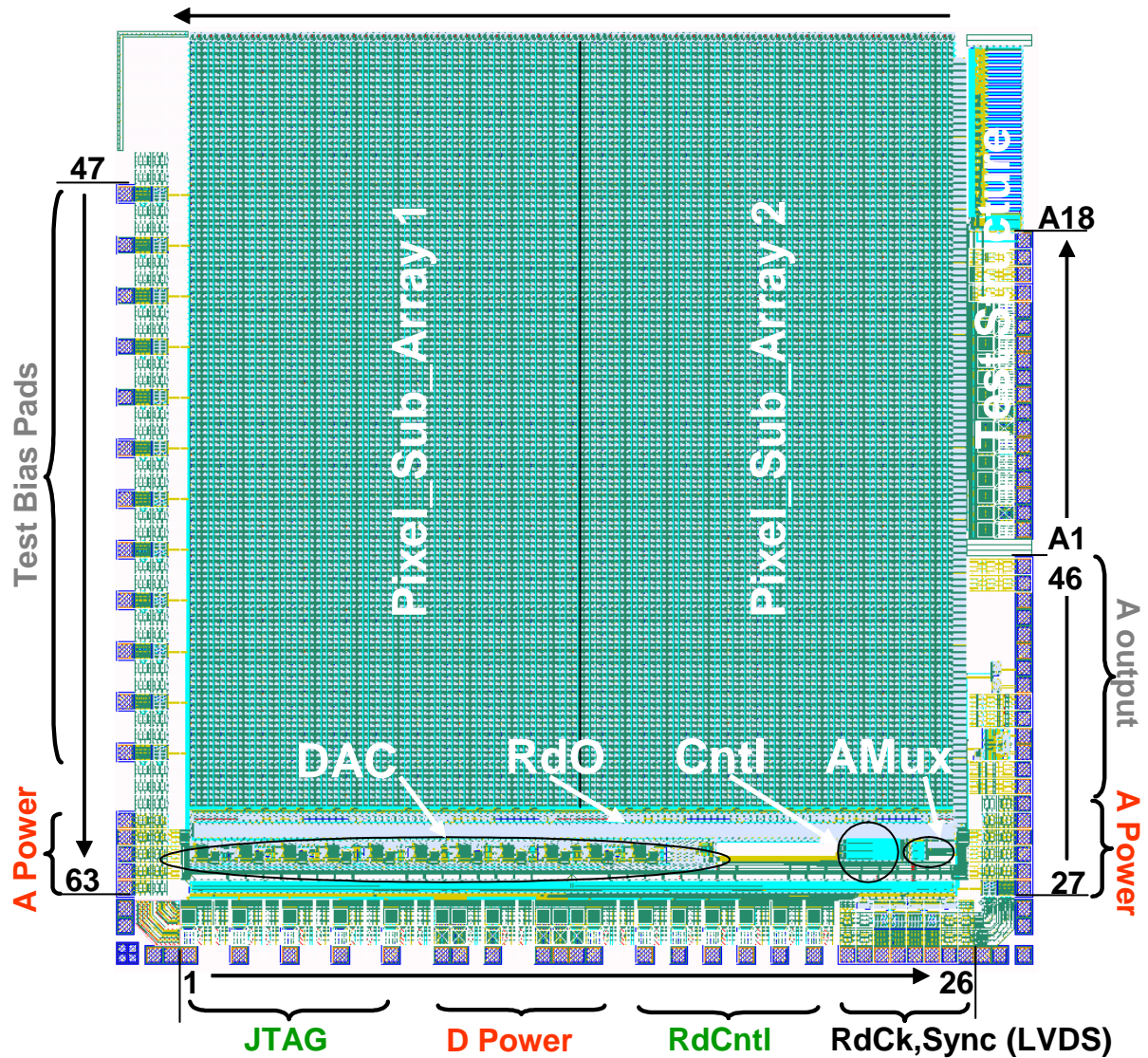
- Pads full custom designed for the analogue signals and power supplies
- Pads from the TPZ873NEZ ARTISAN library for the digital signals and power supplies

The pad ring is split in 6 functional independent parts

- CMOS JTAG and Read Out Control
- LVDS Read Out Drivers
- Analogue Core Supplies
- Read Out Analogue Outputs
- Test Structure pads, Mimostar1 independent
- Bias Test

Each part has its own necessary supply pads.

4.1 MimoStar1 Pad Ring and Floor Plan View



MimosStar1: 63 pads
Test structure: 18 pads
Total: 81 pads
Chip dimension: 4600 x 4680 microns

4.2 Pad List

Pad	Name	Type		Function
Horizontal Bottom Side				
1	RSTB	CMOS In, Schmitt Trigger, Pull-up	PDUSDGZ	Asynchronous Active Low Reset
2	TMS	CMOS In, Schmitt Trigger, Pull-up	PDUSDGZ	JTAG Control Signal
3	TDI	CMOS In, Schmitt Trigger, Pull-up	PDUSDGZ	JTAG Serial Data In
4	TCK	CMOS In, Schmitt Trigger, Pull-up	PDUSDGZ	JTAG Clock
5	TDO	CMOS Out, 3-State	PDT08DGZ	JTAG Serial Data Out
6	VDD	2.5 V Power Supply	PVDD1DG	Digital Core Supply

7	VDD	2.5V Power Supply	PVDD1DG	Digital Core Supply
8	VD33	+3.3 V Power Supply	PVDD2DG	Digital IO Supply
9	GND	GND	PVSS1DG	Digital Core Gnd
10	GND	GND	PVSS1DG	Digital Core Gnd
11	GND_PST	GND	PVSS2DG	Digital IO Gnd
12	RSTMK	CMOS Out, 3-State	PDT08DG Z	Readout Reset Marker
13	SSYNC	CMOS Out, 3-State	PDT08DG Z	Readout Synchro. Start Marker
14	LASTROW	CMOS Out, 3-State	PDT08DG Z	Last Row Marker
15	LASTCOL	CMOS Out, 3-State	PDT08DG Z	Last Column Marker
16	CK5M	CMOS Out, 3-State	PDT08DG Z	CKRD/20→5 MHz for 100MHz
17	CK10M	CMOS Out, 3-State	PDT08DG Z	CKRD/10→10 MHz for 100MHz
18	MXFIRST	CMOS Out, 3-State	PDT08DG Z	Subframes odd pixel selection
19	VDD	2.5 V Power Supply	Full Custom	LVDS Power Supply
20	VDD_RING	2.5 V Power Supply	Full Custom	LVDS Pad Power Supply
21	SYNCP	LVDS In+	Full Custom	Start Readout Signal
22	SYNCN	LVDS In-	Full Custom	
23	CKRDN	LVDS In-	Full Custom	Readout Clock Signal
24	CKRDP	LVDS In+	Full Custom	
25	GND	GND	Full Custom	LVDS Pad Gnd
26	GND	GND	Full Custom	LVDS Gnd
Vertical Right Hand Side				
27	AFIX	ANALOG. In	Full Custom	Serial Output Buffer Dummy Data
28	VDDA	2.5 V	Full Custom	Analogue Core Power Supply
29	VDD_DIODE	2.5 V	Full Custom	Pixel Diode Bias
30	GND	GND	Full Custom	Analogue Core Gnd
31	GND	GND	Full Custom	Analogue Ring Gnd
32	VDD_RING	2.5 V	Full Custom	Analogue Ring Power Supply
33	VDDA	2.5 V	Full Custom	Analogue Output Buffers Supply
34	VDDA	2.5 V	Full Custom	Analogue Output Buffers Supply
35	AOUTN	ANALOG Current Out-	Full	Serial Differential Current Output

			Custom	Buffer
36	AOUTP	ANALOG Current Out+	Full Custom	
37	GND	GND	Full Custom	Analogue Output Buffers Gnd
38	GND	GND	Full Custom	Analogue Output Buffers Gnd
39	ASGL1	ANALOG Voltage Out	Full Custom	Subframe1 Unipolar Output Buffer
40	ASGL0	ANALOG Voltage Out	Full Custom	Subframe0 Unipolar Output Buffer
41	ADIFN0	ANALOG Voltage Out-	Full Custom	Subframe0 Differential Voltage Output Buffer
42	ADIFP0	ANALOG Voltage Out+	Full Custom	
43	ADIFN1	ANALOG Voltage Out-	Full Custom	Subframe1 Differential Voltage Output Buffer
44	ADIFP1	ANALOG Voltage Out+	Full Custom	
45	VREF	ANALOG In	Full Custom	Bias for Differential Voltage Output Buffers
46	VCOM	VDD / GND	Full Custom	Enable of Differential Voltage Output Buffers
A1.. .A18				Not MimoStar1 Purpose
Horizontal Top Side				
Vertical Left Hand Side				
47	ITEST	ANALOG Out	Full Custom	Internal Current Ref Source Test
48	IPIX	ANALOG Out	Full Custom	DAC Test Purpose Only
49	IVTEST1	ANALOG Out	Full Custom	DAC Test Purpose Only
50	IVTEST0	ANALOG Out	Full Custom	DAC Test Purpose Only
51	IVREG	ANALOG Out	Full Custom	DAC Test Purpose Only
52	IREG	ANALOG Out	Full Custom	DAC Test Purpose Only
53	IAMP1	ANALOG Out	Full Custom	DAC Test Purpose Only
54	IAMP2	ANALOG Out	Full Custom	DAC Test Purpose Only
55	IFASTINTBUF	ANALOG Out	Full Custom	DAC Test Purpose Only
56	ISLOWBUF	ANALOG Out	Full Custom	DAC Test Purpose Only
57	IVFASTBUF	ANALOG Out	Full Custom	DAC Test Purpose Only
58	IFASTBUF	ANALOG Out	Full Custom	DAC Test Purpose Only
59	GND	GND	Full	Analogue Ring Gnd

			Custom	
60	GND	GND	Full Custom	Analogue Core Gnd
61	VDD_DIODE	2.5 V	Full Custom	Pixel Diode Bias
62	VDDA	2.5 V	Full Custom	Analogue Core Power Supply
63	VDD_RING	2.5 V	Full Custom	Analogue Ring Power Supply

Foundry submission information

Mimostar1 has been designed in TSMC CMOS Logic 0.25 μm epitaxial process with 1 poly and 5 metal layers. The Process Design Kit has been provided by MOSIS, the same for the ARTISAN libraries which have been used:

- TPZ873NEZ version 230b for the pads
- SAGE sc_2000q2v0 for standard cells

CAD tools are CADENCE DFII 443 with DIVA rules

The chip has been submitted in a Multi Chip Run via MOSIS the 23 august 2004 in the run # T48Z.