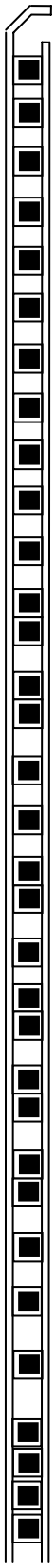
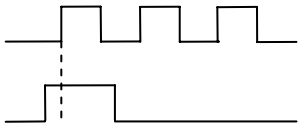
Interfacing to the MIMOSA-5

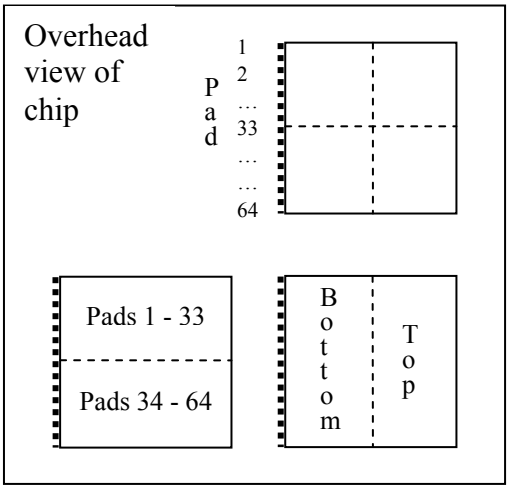


Pad #			
1	34	Shut	Input 5V on, 0V off. Automatic reset after readout if on
2	35	Fast	Input 5V on, 0V off. Read only 1 pixel every 9 if on
3	36	Sum	Input 5V on, 0V off. Sum 3 pixels on 1 row if on
4	37	MKOff	Input 5V on, 0V off. Turn off digital output
5	38	SelMK	Digital output pixel select
6	39	ColMK	Digital output column select (First column marker)
7	40	RowMK	Digital output row select (First row marker)
8	41	RstMK	Digital output reset
9	42	Clock	Digital input clock (up to 40 MHz)
10	43	ClockB	Digital input clock bar
11	44	Reset	Digital input reset
12	45	VDD	Analog input (5V) VDD for digital circuit
13	46	VDD	Analog input (5V) VDD for digital circuit
14	47	Ground	Digital ground
15	48	Ground	Digital ground
16	49	VDMY	Analog DC input: Set output level of the 3 dummy pixels (appear after reset)
17	50	OutTop	Analog DC output: Top section
18	51	VDDB	VDD Buffer (5V)
19	52	VDDB	VDD Buffer (5V)
20	53	OutBot	Analog output: Bottom section
21	54	VRefT	Buffer level: Top (2V) pot
22	55	VRefB	Buffer level: Bottom (2V) pot
23	56	Ground	
24	57	Ground	
25	58	VDDA	VDD Analog (5V)
26	59	VDDA	VDD Analog (5V)
27	60	VDDR	VDD Reset (5V)
28	61	IpolN	36 KΩ resistor to Vdd
29	62	IpolP	100 KΩ resistor to ground
30	63	Att	Input 5V on 0V off. Buffer gain = 2 if on, 4 if off
31	64	Ground	
32		Ground	
33		Ground	

Ground



Reset width a function of clock



Vdd $\xrightarrow{70\mu A}$ Chip pot

GND $\xrightarrow{40\mu A}$ Chip pot