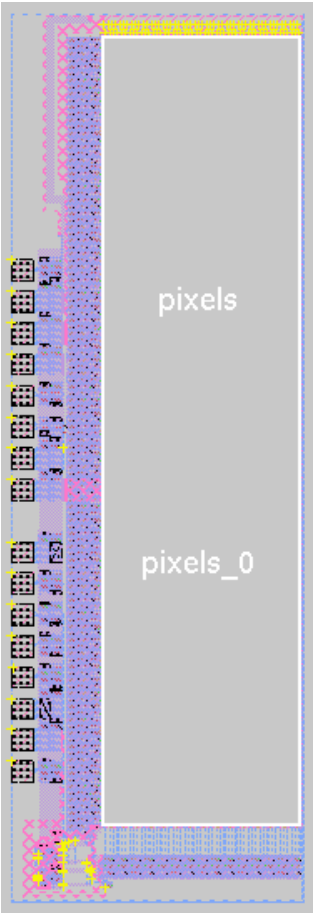
Documentation of the AMI half um chip

Chip Nickname: Neko3_PD_Area

Submitted design file name: Neko_PD_Are_Fina
Submission date: Sep 20, 04



Snapshot of the TOPCELL_Sep16

Neko3_PD_Area AMI 050um process Chip size = 1395 um X 4251.6um

Pad #	**Pad Description**	Cell Name	Notes
1	Reset (global reset M1, in pixel)	Inputpad	
2	Analog_Vdd_M1	powerpad2	
3	Analog_Vdd_M2	powerpad2	
4	Analog_Vdd (for output SF pad 6)	powerpad2	
5	Iout for the output stage source follower SF	Inputpad	
6	Output (output pad of the output stage source follower)	Outputpad	
7	Analog_GND (output SF)	groundpad2	
8	Analog_GND for pwell in all the pixels	groundpad2	
	idle		
9	Digital_Vdd	Powerpad	
10	rck (clock for row shift registers, vshift, vertical, generating Φ_1, Φ_2)	Inputpad	
11	cck (clock for column shift registers, hshift, horizontal, generating Φ_1, Φ_2)	Inputpad	
12	crst (reset for column shift registers, hshift, horizontal)	Inputpad	
13	rrst (reset for row shift registers, vshift, vertical)	Inputpad	
14	Digital_GND	Groundpad	
15	Analog_GND (for the column_current_source)	groundpad2	
16	Iin for column_current_source	inputpad	

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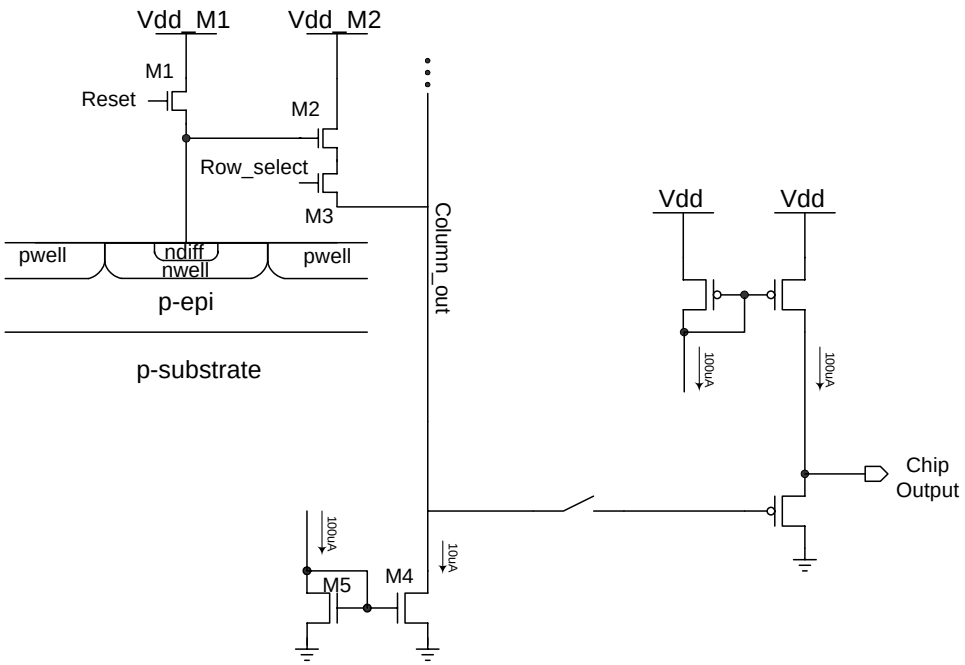
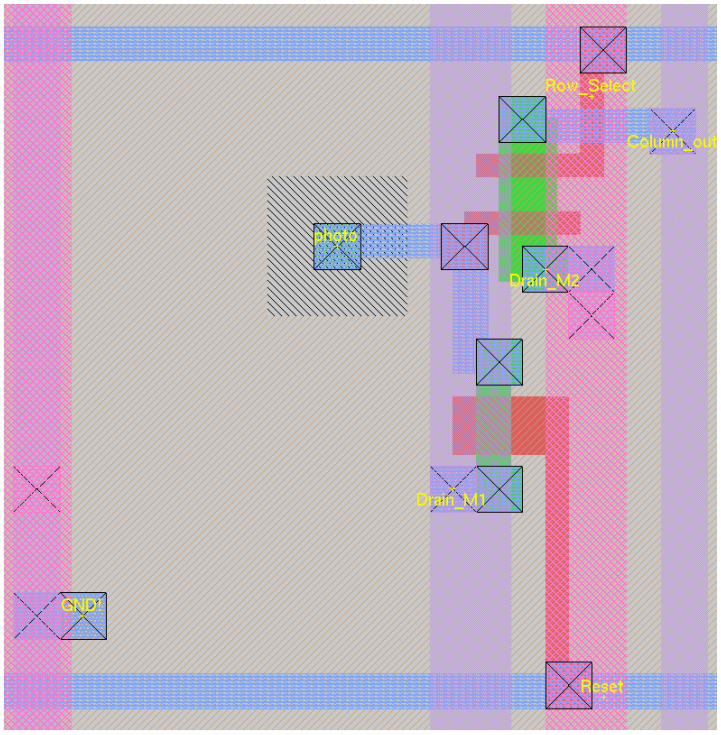


signal path



Specs of photo diodes in different sectors

	Sector1	Sector 2	Sector 3	Sector 4	Sector 5
Area (um^2)	13	20	32	41	54
Dimension (um^2)	6.9×7.8	6.3×6.6	6×5.4	4.5×4.5	3.6×3.6
Number of diodes	40×50	40×50	40×50	40×50	40×50

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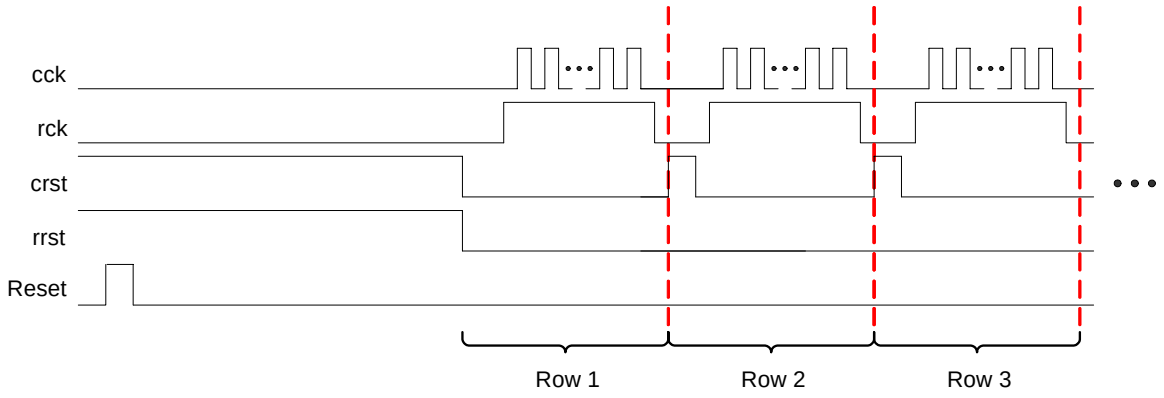
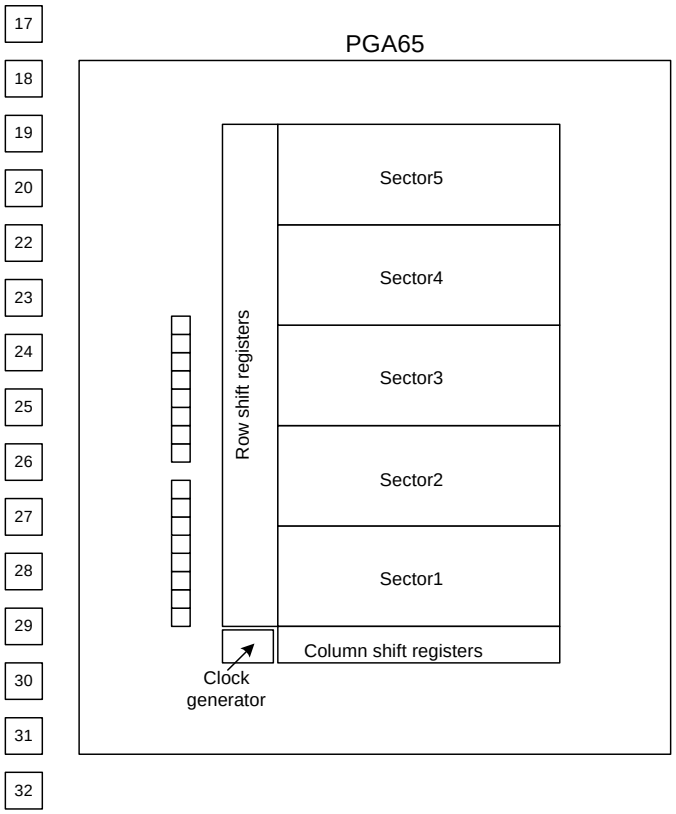
Chip Testing:

1. Vdd = 5.0 V
2. Pad 16 should be connected to Vdd thru a tunable resistor (15 kohm ~ 20 kohm)
3. Pad 5 should be connected to GND thru a tunable resistor (15 kohm ~ 20 kohm)

Timing Diagram:





PGA 65 Package

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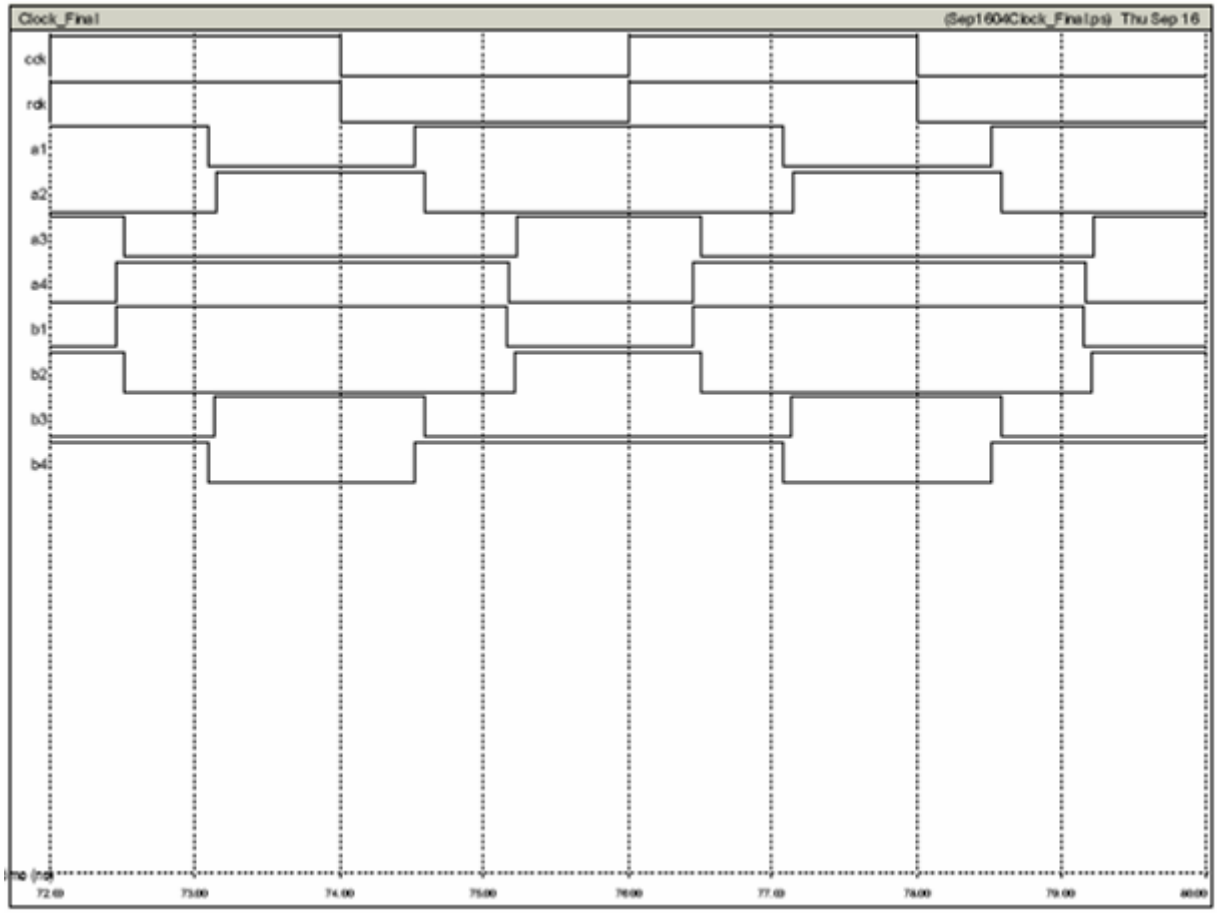
Irsim simulation of the 2-phase non overlapping clock generator



(Sep1604Clock_Final)

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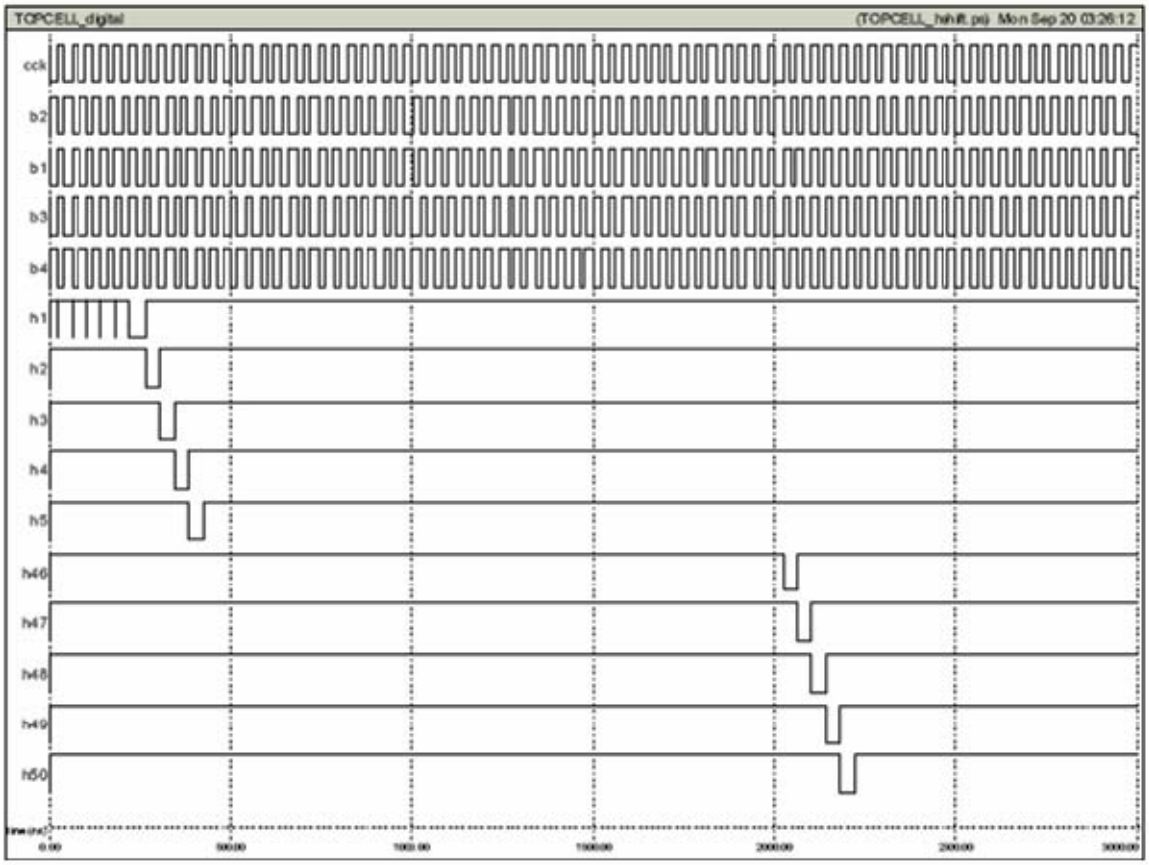

Irsim simulation of the 50 hshift

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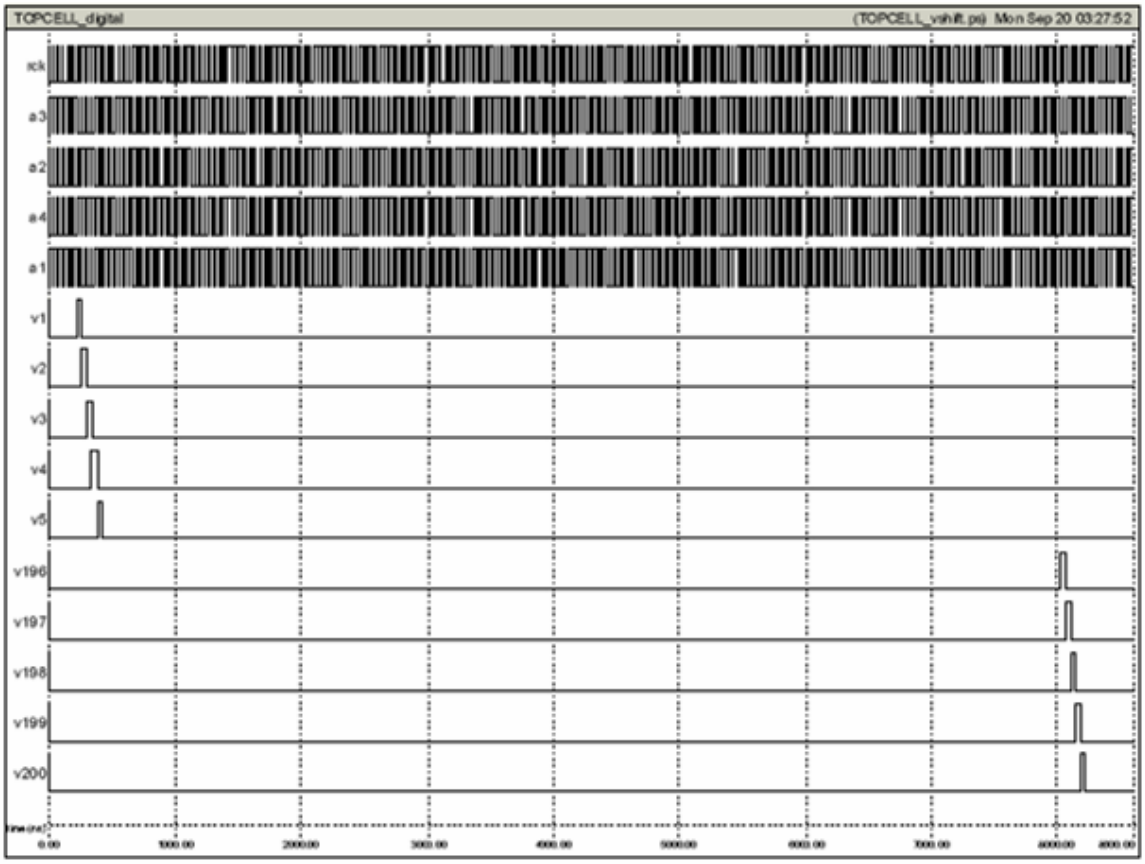
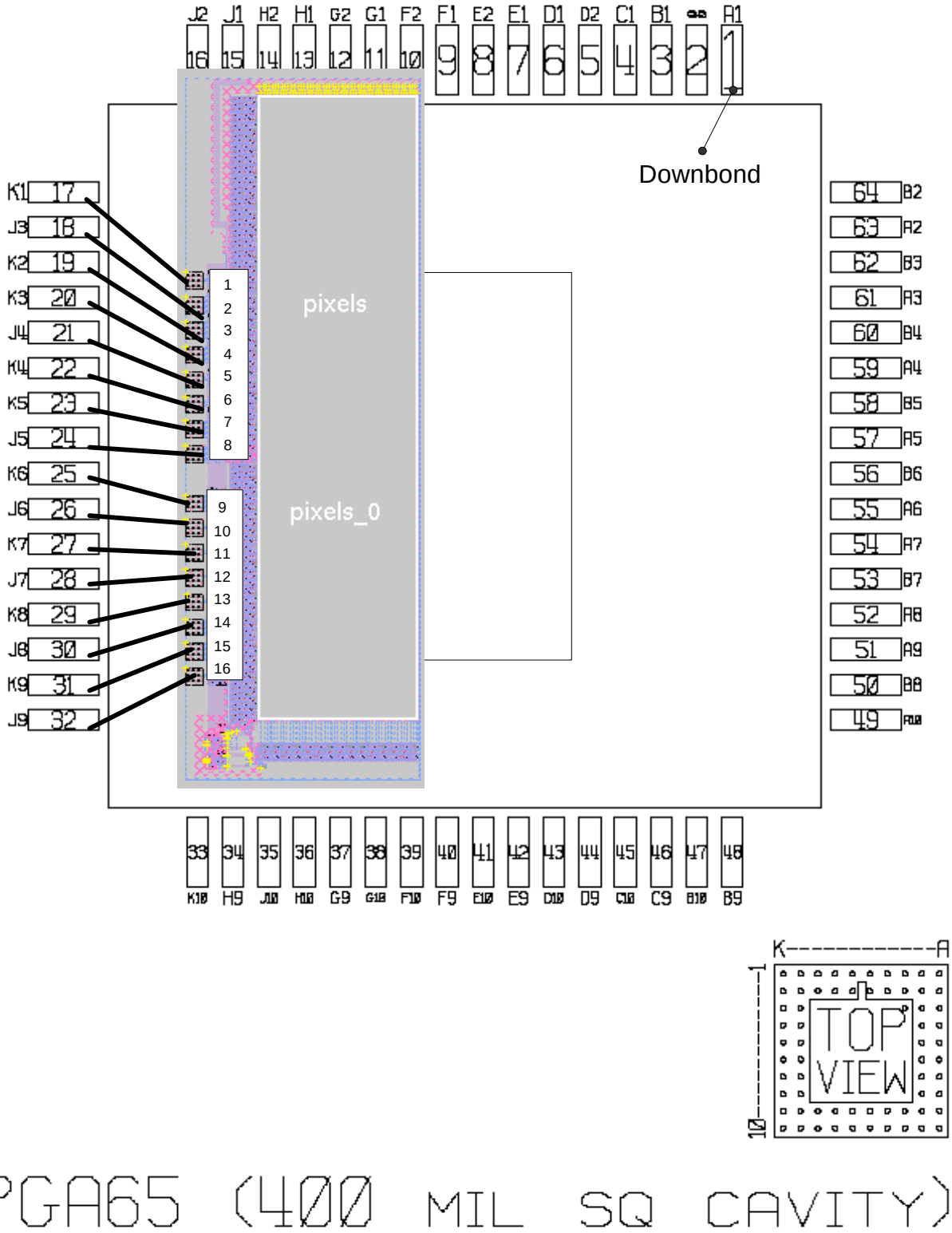


Irsim simulation of the 200 vshift

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