PIXEL CMOS PROJECT

MIMOSTAR PROTOTYPE TEST BOARD

MIMOSTAR_PCB2

Technical Documentation Version 0.2

User's Manual

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Support:

Web address: http://ireswww.in2p3.fr/ires/recherche/capteurs/index.html

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Important Information

Warranty:

The MIMOSTAR_PCB2 test board is warranted against defects in material and workmanship for a period of one year from the date of shipment, as evidence by receipts or other documentation. IReS laboratory will, at its option, repair or replace equipment that proves to be defective during the warranty period. This warranty includes parts and labor.

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Figures

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References

[1] MIMOSTAR2 USER MANUAL, C. Colledani, et al. , Institut de Recherches Subatomiques, France (2005)

Acronyms

About this manual

This is a user manual for MIMOSTAR2 Prototype Test Board.

Modifications Chronology

VERSION	MODIFICATIONS	CHAPTERS
0.1	Creation of the document.	All
0.2	Modifications/Corrections	All

Chapter 1: Introduction and Description

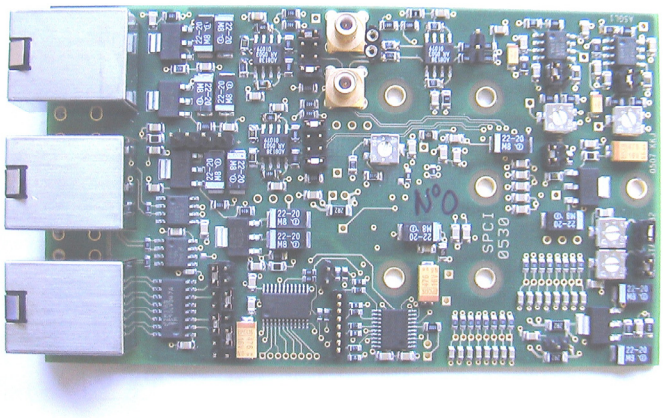


Figure 1.1 MIMOSTAR2 prototype Test Board (MIMOSTAR_PCB2).

MIMOSTAR2 Prototype Test Board (MIMOSTAR_PCB2) is developed in order to be able to test MIMOSTAR2 Prototype. This Prototype device is developed by CMOS group at IRES (Strasbourg, France).

The MIMOSTAR_PCB2 board includes the following functions:

- All the necessary power supplies required by MIMOSTAR Prototype to minimize requirements for external power supplies
- Buffered JTAG interface for the slow control
- LDVS inputs for the LVDS readout clock and the Sync signal (Readout input token)
- LVDS outputs for the digital signal monitoring (max. 4 MIMOSTAR digital signals at the same time)
- 2 Buffered differential analog voltage outputs for parallel output mode (Single-Ended/Differential)
- 1 Buffered differential analog voltage output for differential serial current output mode
- Optional CMOS input for the CMOS readout clock

The MIMOSTAR_PCB2 board is shown in Fig. 1.1.

Chapter 2: Functional Description

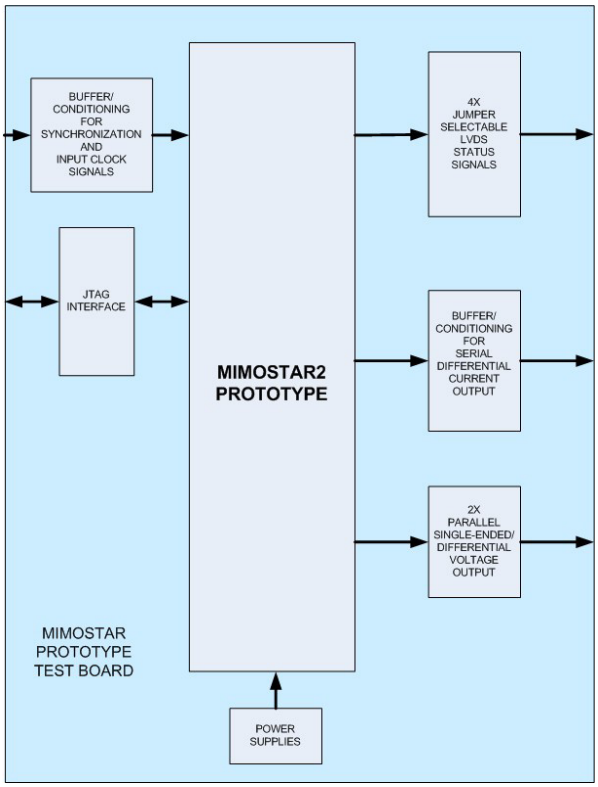


Figure 2.1: A block diagram of MIMOSTAR_PCB2 card.

In Fig. 2.1 is presented a block diagram of MIMOSTAR_PCB2 board. Basically MIMOSTAR_PCB2 board includes all the necessary buffering /conditioning for the digital input signals. The LVDS Clock input signal is buffered at the board level and the LVDS synchronization signal (SYNC) is converted to the CMOS standard signaling levels. The JTAG signals are buffered at the both sense.

To minimize the power supply requirements, the board is furnished with regulator units for the analog power supplies (-5.0V, 1.25V, 3.3V and 5.0V) and for the digital power supplies (3.3V and 5.0V). The board necessities only two power supply voltages: -8.0V ± 100 mV and 8.0V± 100 mV.

For monitoring of digital output signals of MIMOSTAR2 (CMOS level signaling), the board includes a jumper selection and a conditioning from CMOS levels to LVDS levels. More details of the jumper selection can be founded in Chapter 3.1 (Table 3.1.6).

The serial differential current output of MIMOSTAR2 is terminated to 1.25V with two 100 ohm resistances. A differential voltage Op-amp is used to buffer the voltage signal.

The selection of output mode (single-ended/differential) for parallel output is done by jumpers. The single-ended output signal is buffered. There is also possibility to adjust the offset level by a potentiometer or by an internal DAC of MIMOSTAR2 (IKIMO). The output signal is driven by a differential voltage output Op-Amp.

Chapter 3: Hardware Description

Chapter 3.1: FRONT-END INTERFACE

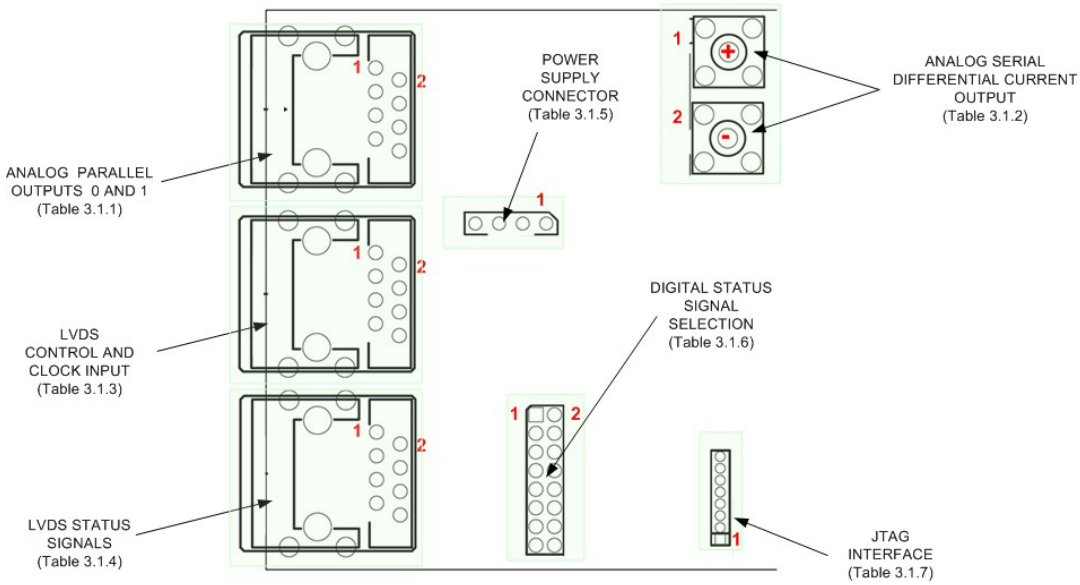


Figure 3.1: The Front-end interface of MIMOSTAR_PCB2 board (top view).

The Front-end interface of MIMOSTAR_PCB2 card is presented in Fig. 3.1. This interface groups all the necessary signals to acquire the data and to control the acquisition.

PIN	SIGNAL NAME	I/O	TYPE	DESCRIPTION
1	GND	-	ANALOG	GROUND
2	GND	-	ANALOG	GROUND
3	ASGL1P	O	ANALOG	DIFFERENTIAL PARALLEL ANALOG OUTPUT FOR MIMOSTAR PROTOTYPE SIGNAL ASGL1P (POSITIVE)
4	ASGL1N	O	ANALOG	DIFFERENTIAL PARALLEL ANALOG OUTPUT FOR MIMOSTAR PROTOTYPE SIGNAL ASGL1N (NEGATIVE)
5	GND	-	ANALOG	GROUND
6	GND	-	ANALOG	GROUND
7	ASGL0P	O	ANALOG	DIFFERENTIAL PARALLEL ANALOG OUTPUT FOR MIMOSTAR PROTOTYPE SIGNAL ASGL0P (POSITIVE)
8	ASGL0N	O	ANALOG	DIFFERENTIAL PARALLEL ANALOG OUTPUT FOR MIMOSTAR PROTOTYPE SIGNAL ASGL0N (NEGATIVE)

Table 3.1.1: Pin description of the signals for Analog Parallel Outputs 0 and 1.

PIN	SIGNAL NAME	I/O	TYPE	DESCRIPTION
1	AOUTP	O	ANALOG	SERIAL DIFFERENTIAL CURRENT ANALOG OUTPUT FOR MIMOSTAR PROTOTYPE SIGNAL AOUTP (POSITIVE)
2	AOUTN	O	ANALOG	SERIAL DIFFERENTIAL CURRENT ANALOG OUTPUT FOR MIMOSTAR PROTOTYPE SIGNAL AOUTN (NEGATIVE)

Table 3.1.2: Pin description of the signals for Analog Serial Differential Current Output.

PIN	SIGNAL NAME	I/O	TYPE	DESCRIPTION
1	CLKRDN	I	DIGITAL	LVDS READOUT CLOCK INPUT (NEGATIVE)
2	CLKRDP	I	DIGITAL	LVDS READOUT CLOCK INPUT (POSITIVE)
3	GND	-	DIGITAL	GROUND
4	GND	-	DIGITAL	GROUND
5	CLK10XP	I	DIGITAL	OPTIONAL LVDS READOUT CLOCK INPUT FOR CMOS CLOCK (POSITIVE)
6	CLK10XN	I	DIGITAL	OPTIONAL LVDS READOUT CLOCK INPUT FOR CMOS CLOCK (NEGATIVE)
7	SYNCP	I	DIGITAL	LVDS SYNCRONIZATION INPUT (POSITIVE)
8	SYNCN	I	DIGITAL	LVDS SYNCRONIZATION INPUT (NEGATIVE)

Table 3.1.3: Pin description of the signals for LVDS Control and Clock input.

PIN	SIGNAL NAME	I/O	TYPE	DESCRIPTION
1	LVDSOUT4N	O	DIGITAL	DIFFERENTIAL OUTPUT 4 (NEGATIVE)
2	LVDSOUT4P	O	DIGITAL	DIFFERENTIAL OUTPUT 4 (POSITIVE)
3	LVDSOUT3N	O	DIGITAL	DIFFERENTIAL OUTPUT 3 (NEGATIVE)
4	LVDSOUT3P	O	DIGITAL	DIFFERENTIAL OUTPUT 3 (POSITIVE)
5	LVDSOUT2N	O	DIGITAL	DIFFERENTIAL OUTPUT 2 (NEGATIVE)
6	LVDSOUT2P	O	DIGITAL	DIFFERENTIAL OUTPUT 2 (POSITIVE)
7	LVDSOUT1N	O	DIGITAL	DIFFERENTIAL OUTPUT 1 (NEGATIVE)
8	LVDSOUT1P	O	DIGITAL	DIFFERENTIAL OUTPUT 1 POSITIVE)

Table 3.1.4: Pin description of the signals for LVDS Status signals.

PIN	SIGNAL NAME	I/O	TYPE	DESCRIPTION
1	VPOWERP	I	-	POSITIVE POWER SUPPLY INPUT (8.0V ± 100 mV)
2	GND	-	-	GROUND
3	GND	-	-	GROUND
4	VPOWERN	I	-	NEGATIVE POWER SUPPLY INPUT (-8.0V ± 100 mV)

Table 3.1.5: Pin description of the signals for Power supply connector.

See the Chapter 3.1.2. for an example of the Digital Status signal selection.

PIN	SIGNAL NAME	I/O	TYPE	DESCRIPTION
1	LVDSOUT4	O	DIGITAL	INPUT SIGNAL FOR LVDSOUT4 SIGNAL
2	LVDSOUT4	O	DIGITAL	INPUT SIGNAL FOR LVDSOUT4 SIGNAL
3	CK10M	O	DIGITAL	10 MHZ CLOCK SIGNAL
4	MXFIRST	O	DIGITAL	MARKER SIGNAL FOR 100 MHZ MUX (WHEN FIRST COLON IS SELECTED FOR OUTPUT)
5	LVDSOUT3	O	DIGITAL	INPUT SIGNAL FOR LVDSOUT3 SIGNAL
6	LVDSOUT3	O	DIGITAL	INPUT SIGNAL FOR LVDSOUT3 SIGNAL
7	SSYNC	O	DIGITAL	RESPONSE TOKEN FOR SYNCRONIZATION REQUEST (SYNC)
8	LASTCOL	O	DIGITAL	MARKER SIGNAL OF THE LAST COLON
9	LVDSOUT2	O	DIGITAL	INPUT SIGNAL FOR LVDSOUT2 SIGNAL
10	LVDSOUT2	O	DIGITAL	INPUT SIGNAL FOR LVDSOUT2 SIGNAL
11	RSTMK	O	DIGITAL	RESET TOKEN FOR SYNCRONIZATION REQUEST (SYNC)
12	LASTROW	O	DIGITAL	MARKER SIGNAL OF THE LAST ROW
13	LVDSOUT1	O	DIGITAL	INPUT SIGNAL FOR LVDSOUT1 SIGNAL
14	LVDSOUT1	O	DIGITAL	INPUT SIGNAL FOR LVDSOUT1 SIGNAL
15	CK10M	O	DIGITAL	10 MHZ CLOCK SIGNAL
16	SSYNC	O	DIGITAL	RESPONSE TOKEN FOR SYNCRONIZATION REQUEST (SYNC)

Table 3.1.6: Pin description of the signals for Digital Status signal selection

PIN	SIGNAL NAME	I/O	TYPE	DESCRIPTION
1	TCK	I	DIGITAL	JTAG TCK SIGNAL (TTL/CMOS)
2	GND	-	DIGITAL	GROUND
3	TMS	I	DIGITAL	JTAG TMS SIGNAL (TTL/CMOS)
4	TDI	I	DIGITAL	JTAG TDI SIGNAL (TTL/CMOS)
5	GND	-	DIGITAL	GROUND
6	TDO	O	DIGITAL	JTAG TDO SIGNAL (TTL/CMOS)
7	GND	-	DIGITAL	GROUND
8	RSTB	I	DIGITAL	JTAG RESET SIGNAL (TTL/CMOS)

Table 3.1.7: Pin description of the signals for JTAG interface.

Chapter 3.1.1: ANALOG FRONT-END INTERFACE

The Analog Front-end consists of a differential voltage output for the serial output and two differential voltage outputs for the parallel outputs. The Parallel output mode (single-ended or differential) can be selected by jumper separately for each parallel output). In single-ended mode, the parallel outputs have a fixed gain of 4 at the board level. In differential mode, the gain of the parallel outputs is 2 at the board level. The jumper selections are shown in Fig. 3.2.

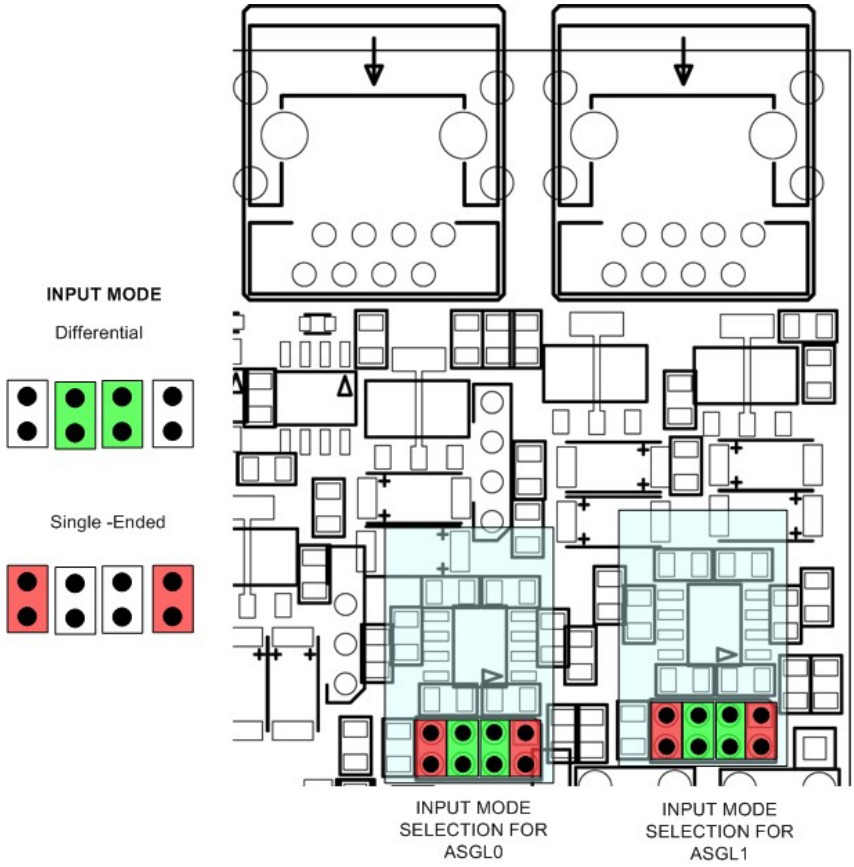


Figure 3.2: The jumper selections for the MIMOSTAR2 PROTOTYPE connection.

The Output signal offset adjustment for parallel outputs in single-ended mode can be selected by jumpers. These settings are shown in Fig 3.3. Each channel has a potentiometer (ref. P02 for signal ASGL0 and ref. P05 for signal ASGL1) for offset adjustment. There is also a common offset adjustment for outputs ASGL0 and ASGL1 by a DAC (IKIMO) of MIMOSTAR 2 device. For acquisition timing adjustment, “LAST_ROW” signal can be routed to the output ASGL1.

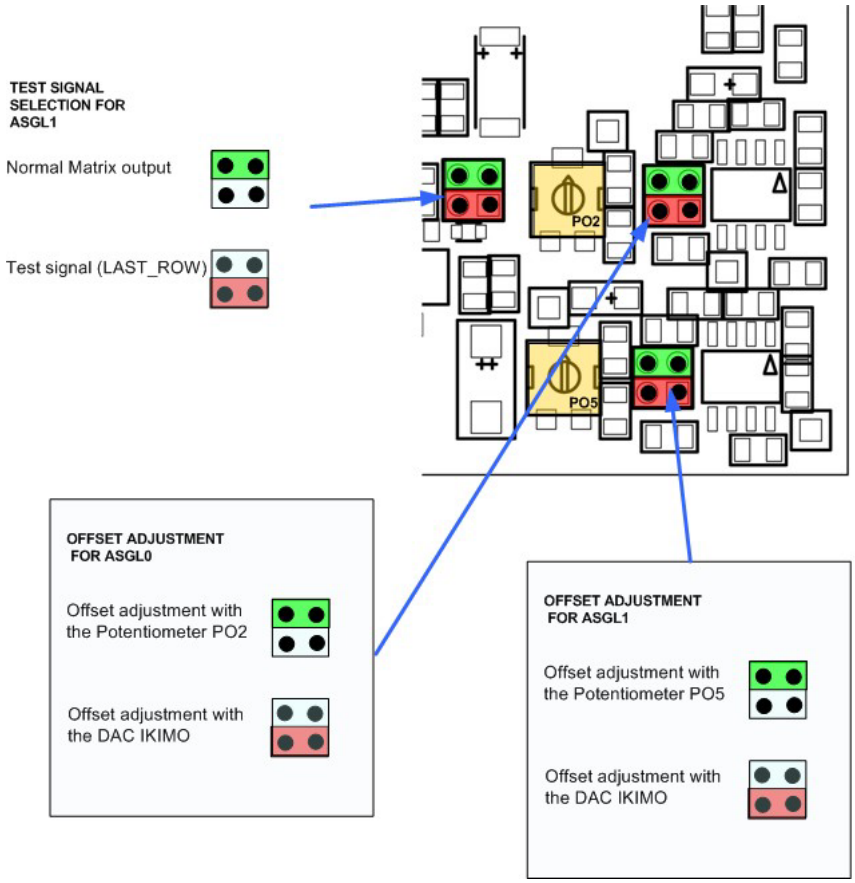


Figure 3.3: The jumper selections for the MIMOSTAR2 PROTOTYPE input selections.

The serial output has a fixed gain of 4 at the board level.

All the analog outputs should be terminated at the end of the signaling path with a 100 ohm termination resistance across the differential signal line. This configuration is shown in Fig. 3.4.

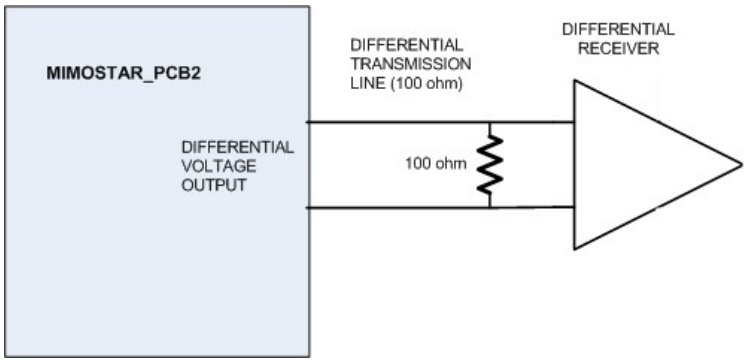


Figure 3.4: A Termination configuration of the differential voltage output for MIMOSTAR_PCB2.

Chapter 3.1.2: DIGITAL FRONT-END INTERFACE

The digital front-end interface consists of 4 LVDS status output signals and 2 LVDS inputs for clock signal (CLKRD) and a synchronization signal (SYNC). The LVDS input pairs are terminated to 100 ohm and the LVDS outputs should be terminated across the differential signal line at the end of the signaling path. The pinout for LVDS inputs are described at the beginning of the Chapter 3.1 (Table 3.1.3).

An example of the status signal configuration is shown in Fig. 3.5. The selection of the signals is summarized in Table 3.2.1. See the Chapter 3.1 (Table 3.1.6) for the jumper pinout.

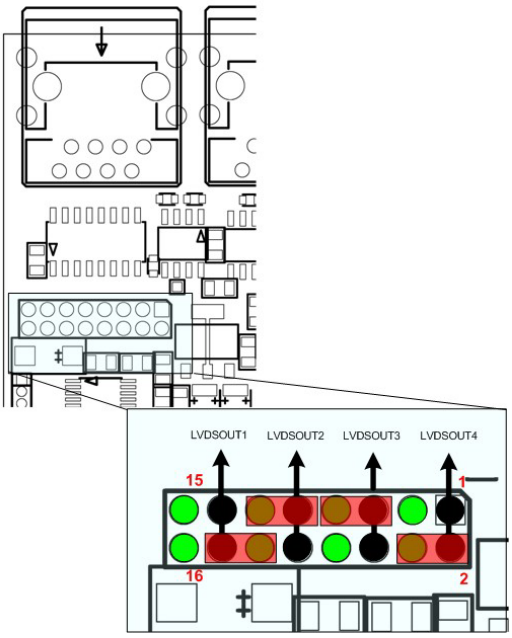


Figure 3.5: An example of the jumper selections for the LVDS status signals.

STATUS SIGNAL	STATUS SIGNAL INPUT
LVDSOUT1	LASTROW
LVDSOUT2	RSTMK
LVDSOUT3	LASTCOL
LVDSOUT4	CK10M

Table 3.2.1: An example of status signal selection.

Chapter 3.1.3: OUTPUTS OF INTERNAL DACS

Test points for internal DACS are shown in Fig. 3.6. Each of these test point is connected to the ground via 100 nF capacitor. For details of these test points, see the Chapter 3.2 “Biasing Mimostar2” of MIMOSTAR2 USER MANUAL (MIMOSTAR2 device user manual).

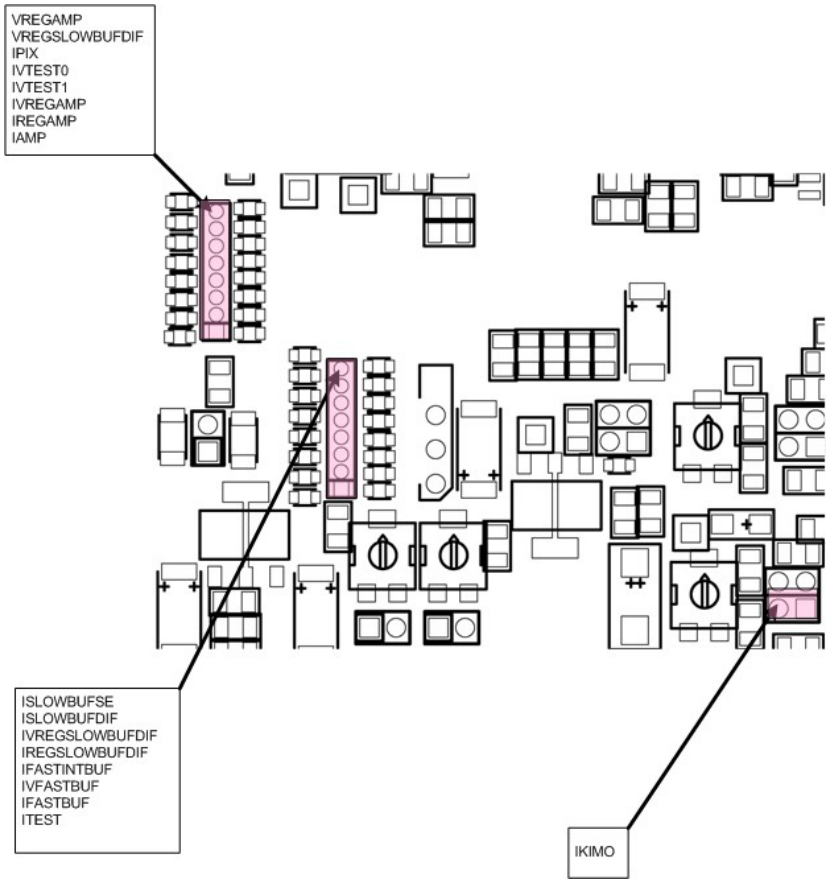


Figure 3.6: Locations of the test points for internal DACs.

Appendix A: Specifications for Usage

1. POWER REQUIREMENTS

PARAMETER	DESCRIPTION
+8V	TYPICAL 0.26 A (PARALLEL MODE) 0.30 A (SERIAL DIFFERENTIAL CURRENT MODE) MAX. 0.36 A
-8V	TYPICAL 0.11 A MAX. 0.16 A

2. PHYSICAL DIMENSIONS (PCB)

PARAMETER	DESCRIPTION
HEIGHT	1.6 mm (0.06 in.)
DEPTH	102 mm (4.01 in.)
WIDTH	60 mm (2.36 in.)

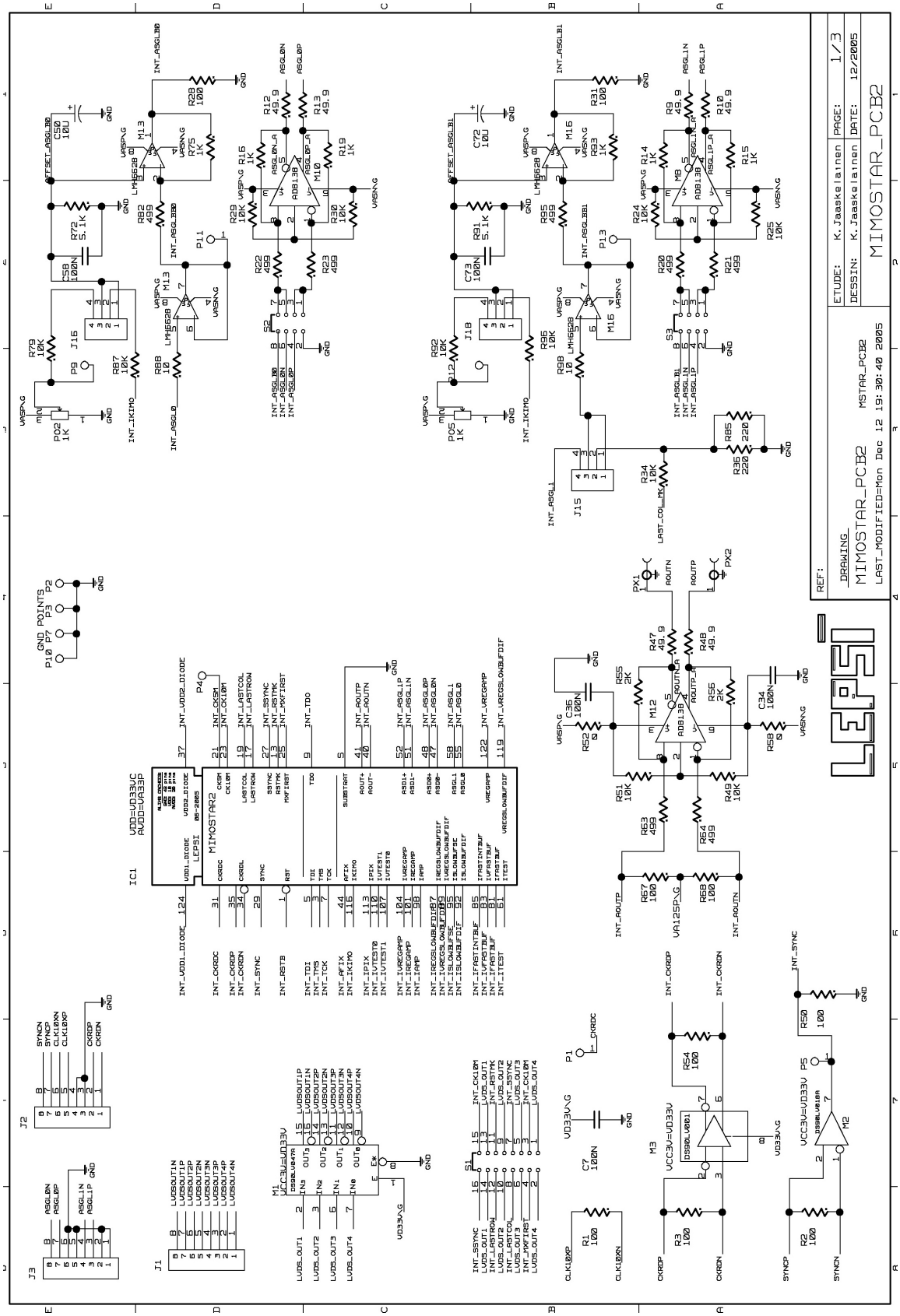
3. ENVIRONMENTAL

PARAMETER	DESCRIPTION
OPERATING TEMPERATURE RANGE	0 to 40 °C
RELATIVE HUMIDITY	To 70%

Appendix B: Component list

Line	Pcs	Reference	Value	Type	Size	Description	RefDes
1		Capacitor SMD					
2	45	CAPA	100N	0805		SMD 0805 Ceramic multi-layer	C1 C2 C3 C4 C5
3							C6 C8 C10 C13 C18
4							C19 C20 C21 C22 C25
5							C26 C27 C28 C29 C30
6							C33 C34 C35 C36 C38
7							C39 C40 C42 C47 C52
8							C53 C55 C56 C57 C58
9							C59 C61 C69 C70 C71
10							C73 C74 C75 C77 C80
11	17	CAPA	100N	0603		SMD 0603 Ceramic multi-layer	C7 C37 C41 C43 C44
12							C45 C46 C48 C49 C51
13							C60 C62 C63 C64 C65
14							C66 C68
15	2	CPOL	10U	TAN10V		SMD TANTAL size A	C50 C72
16	13	CPOL	22U	TAN20V		SMD TANTAL size C	C9 C11 C12 C14 C15
17							C16 C23 C24 C31 C54
18							C67 C76 C78
19	3	CPOL	47U	TAN16V		SMD TANTAL size C	C17 C32 C79
20							
21		Connectors					
22	6	CON2P		BAR-2X1-2.0MM-F	SAMTEC/SQT-101-01-L-D	connector 2x1 pins FEMALE 2mm	J7 J9 J11 J13 J19
23							J20
24	3	CON3P				connector SIL STRAIGHT, MALE 2.54mm (NOT MOUNTED)	J5 J10 J17
25	1	CON4P				connector SIL STRAIGHT, MALE 2.54mm	J4
26	3	CON4P		2X2MD-MTMM	SAMTEC/MTMM-102-08-T-D-255	connector 2mm MALE	J15 J16 J18
27	3	CON8P		RJ45	MOLEX/95121-2881	socket RJ45 8/8 SHIELDED R/A	J1 J2 J3
28	4	CON8P		BAR-D-M-T-1R	SAMTEC/TMS-140-01-S-S	connector SIL STRAIGHT, MALE 1.27 mm	J6 J8 J12 J14
29							
30		IC					
31	1	74LVC244A_TSSOP		TSSOP	TI/SN74LVC244APW	package TSSOP 20 pins	M11
32	1	74LVCC4245A_TSSOP		TSSOP	TI/SN74LVCC4245APW	package TSSOP 24 pins	M9
33							
34		IC SMD					
35	3	AD8138_SOIC		SOZ8_60	AD8138AR	package SMD 8 pins	M8 M10 M12
36	1	DS90LV001_SOIC		SOIC	NS/DS90LV001TM	package SMD 8 pins	M3
37	1	DS90LV018A_SOIC		SOIC	NS/DS90LV018ATM	package SMD 8 pins	M2
38	1	DS90LV047A_SOIC		SOIC	NS/DS90LV047ATM	package SMD 16 pins	M1
39	5	LM1117_SOT223	ADJ	SOT223	TI	variable output voltage, package SMD SOT223	M4 M6 M7 M14 M15
40	1	LM337MP	3.3V	SOIC LM337MP	NS	variable output voltage, package SMD SOT223	M5
41	2	LMH6628_SOIC		SOIC	NS/LMH6628MA	Small Outline Z-leaded 8 pins 6.0mm (MS12AA)	M13 M16
42							
43		Padstack, Test point					
44	2	PASCON		PIN100X100		test point padstack 1.0 x 1.0 mm (NOT MOUNTED)	P1 P5
45	11	PASCON		PASTILLE143		test point padstack 1.43mm hole 0.8mm (NOT MOUNTED)	P2 P3 P4 P6 P7
46							P8 P9 P10 P11 P12
47							P13
48							
49		Potentiometers SMD					
50	5	POT	1K	SMD1T	BOURNS-3314G-1-102E-IRES	potentiometer SMD	PO1 PO2 PO3 PO4 PO5
51							
52		COAX Connector					
53	2	PCOAX		PRISE-SMB_D	AMPHENOL	JACK, SMB PCB STRAIGHT	PX1 PX2
54							
55		Resistance SMD					
56	2	RGEN	0	0805		SMD 0805	R52 R58
57	16	RGEN	0	0603		SMD 0603	R59 R61 R62 R65 R66
58							R69 R70 R71 R73 R74
59							R76 R78 R83 R84 R86
60							R89
61	3	RGEN	2.2	1206		SMD 1206 250mW 5%	R35 R77 R80
62	6	RGEN	10	0603		SMD 0603 1% 100ppm	R32 R33 R38 R40 R41
63							R44
64	3	RGEN	10	0805		SMD 0805 1% 100ppm	R81 R88 R98
65	6	RGEN	49.9	0805		SMD 0805 1% 100ppm	R9 R10 R12 R13 R47
66							R48
67	5	RGEN	100	0603		SMD 0603 1% 100ppm	R1 R2 R3 R50 R54
68	9	RGEN	100	0805		SMD 0805 1% 100ppm	R7 R8 R18 R28 R31
69							R53 R67 R68 R94
70	1	RGEN	121	0805		SMD 0805 1% 100ppm	R5
71	2	RGEN	162	0805		SMD 0805 1% 100ppm	R11 R97
72	2	RGEN	220	0603		SMD 0603 1% 100ppm	R36 R85
73	3	RGEN	301	0805		SMD 0805 1% 100ppm	R4 R17 R90
74	1	RGEN	365	0805		SMD 0805 1% 100ppm	R6
75	10	RGEN	499	0805		SMD 0805 1% 100ppm	R20 R21 R22 R23 R43
76							R46 R63 R64 R82 R95
77	4	RGEN	510	0603		SMD 0603 1% 100ppm	R37 R39 R42 R45
78	6	RGEN	1K	0805		SMD 0805 1% 100ppm	R14 R15 R16 R19 R75
79							R93
80	2	RGEN	1K	0603		SMD 0603 1% 100ppm	R26 R27
81	2	RGEN	2K	0805		SMD 0805 1% 100ppm	R55 R56
82	2	RGEN	5.1K	0805		SMD 0805 1% 100ppm	R72 R91
83	10	RGEN	10K	0805		SMD 0805 1% 100ppm	R24 R25 R29 R30 R49
84							R51 R79 R87 R92 R96
85	1	RGEN	10K	0603		SMD 0603 1% 100ppm	R34
86	2	RGEN	100K	0805		SMD 0805 1% 100ppm	R57 R60
87							
88		Switches					
89	2	STRAP4		2.00	SAMTEC/TMM-104-XX-T-D	4 Straps 2.00mm	S2 S3
90	1	STRAP8		2.00	SAMTEC/TMM-108-XX-T-D	8 Straps 2.00mm	S1
91							
92		Others					
93	1	MIMOSTAR2_CHIP		CHIP		Mimostar2 device	IC1

Appendix C: Electronics Schematics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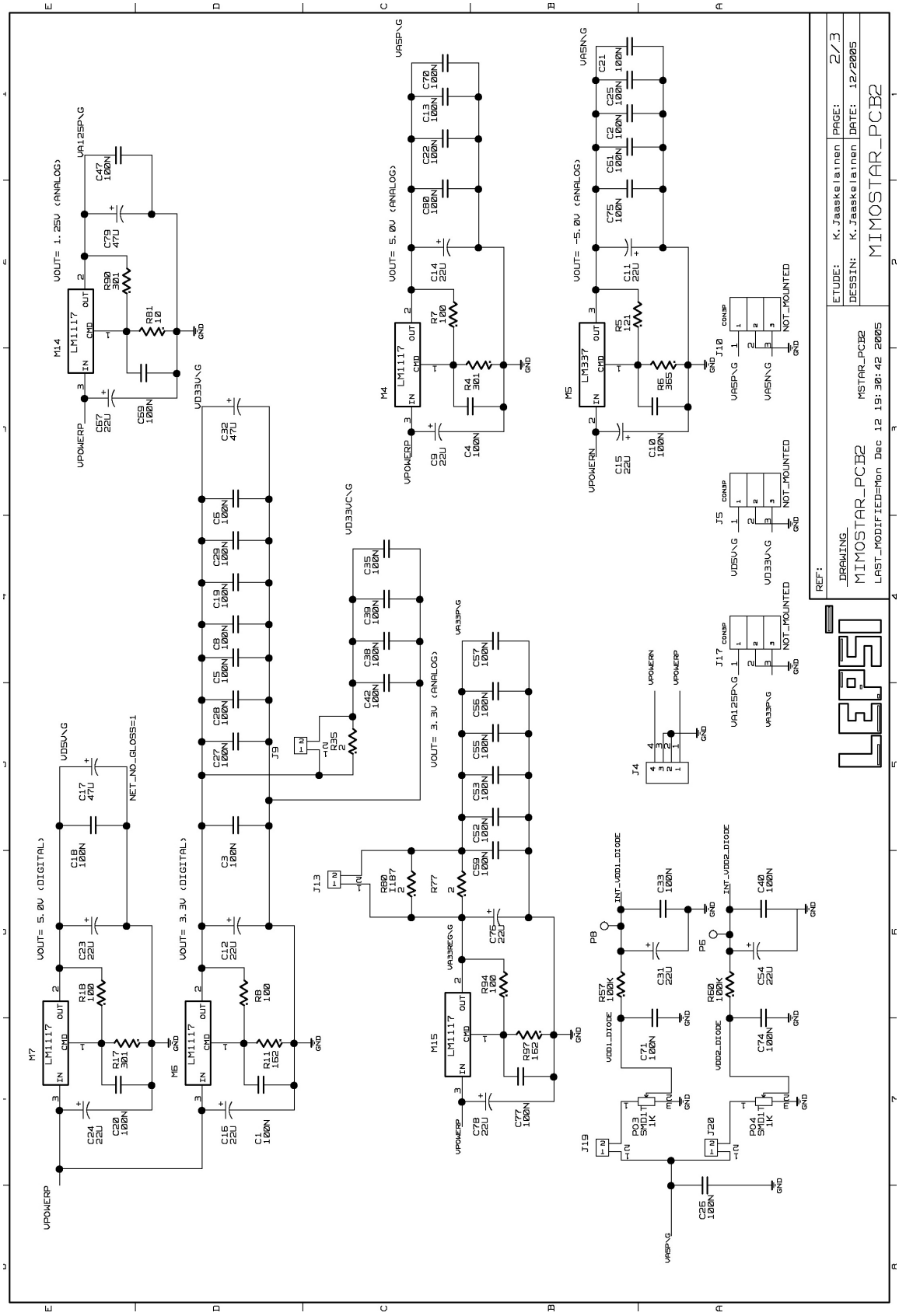
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VOUT= 3.3V (ANALOG)
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M4 LM1117
M5 LM337
M7 LM1117
M6 LM1117
M15 LM1117
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VPOWERN
VA125P\G
VASP\G
VASN\G
VD33V\G
VD33VC\G
VD5V\G
VA33P\G
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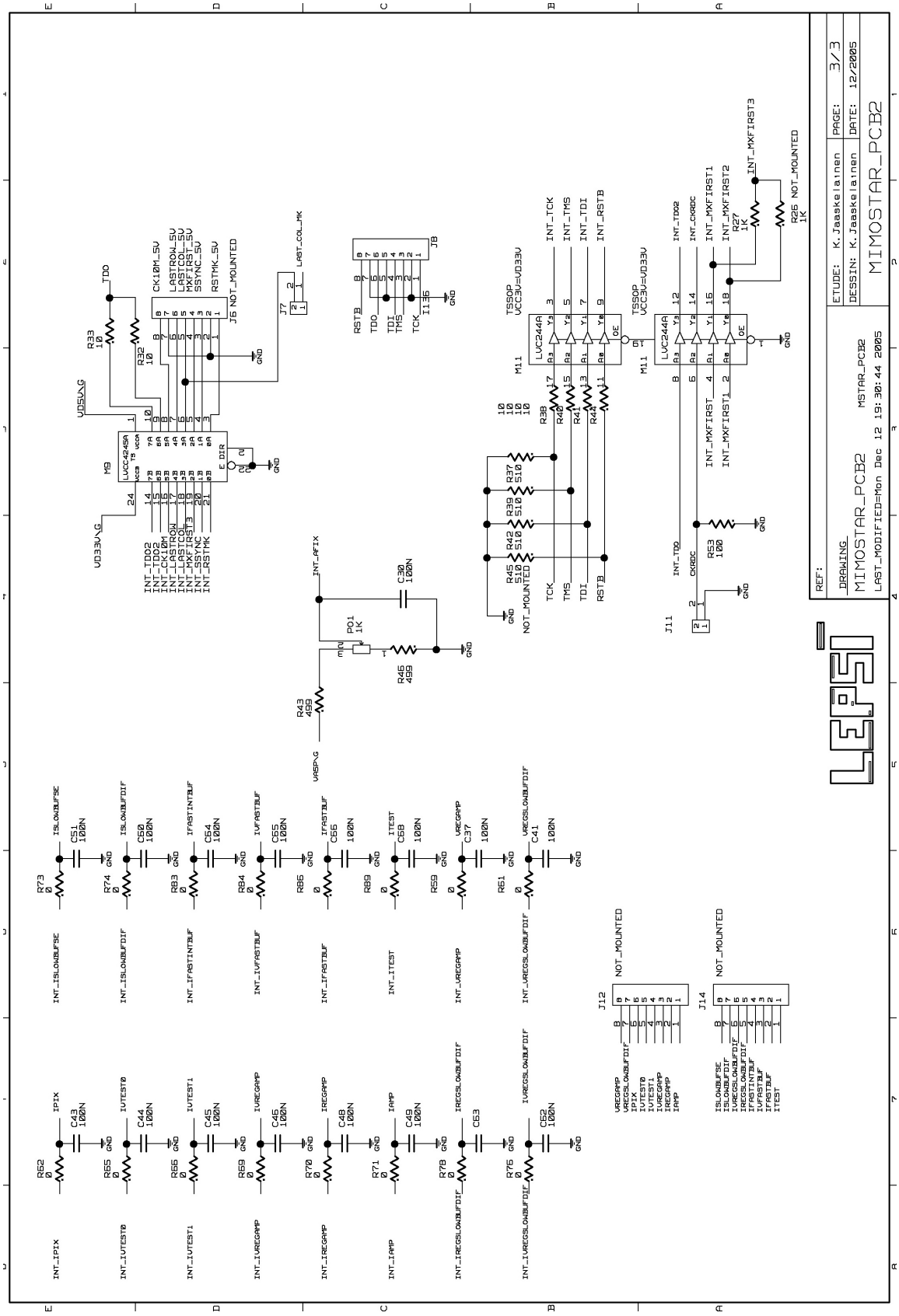
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ETUDE: K.Jaaskelainen
DESSIN: K.Jaaskelainen
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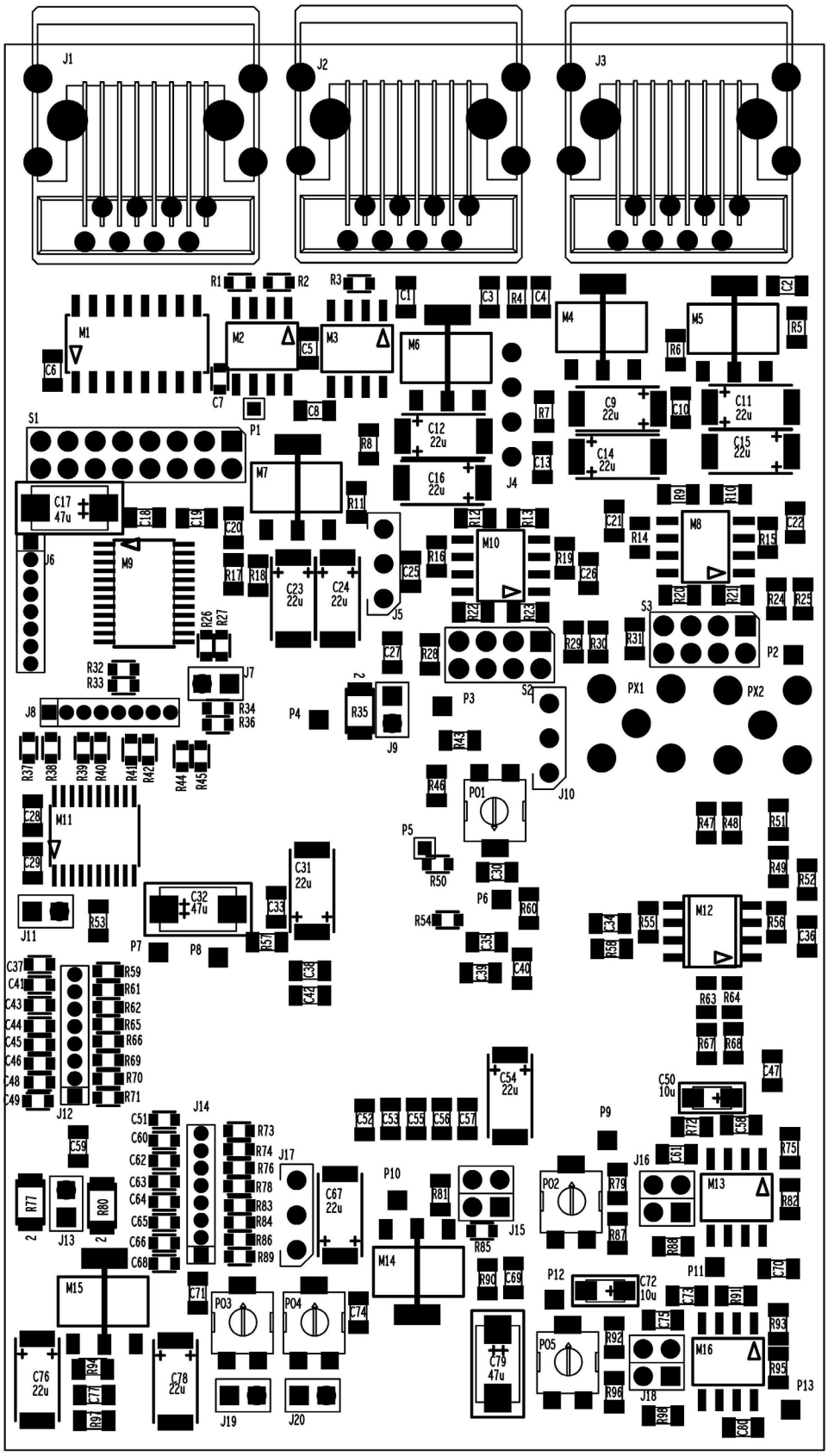
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