PIXEL CMOS PROJECT

MIMOSTAR PROTOTYPE TEST BOARD

MIMOSTAR_PCB2

Technical Documentation Version 0.2

Test Procedure

ATTENTION!

OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC DISCHARGE SENSITIVE EQUIPMENT.

Ref Number: IRES_CMOS_MIMOSTAR_PCB2_TEST_PROCEDURE_0601 (060118)

Support:

Web address: http://ireswww.in2p3.fr/ires/recherche/capteurs/index.html

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Important Information

Warranty:

The MIMOSTAR_PCB2 cards are warranted against defects in material and workmanship for a period of one year from the date of shipment, as evidence by receipts or other documentation. IReS laboratory will, at its option, repair or replace equipment that proves to be defective during the warranty period. This warranty includes parts and labor.

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Copyright:

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References

[1] MIMOSTAR_PCB2 User Manual

Acronyms

About this manual

This is a test manual for the MIMOSTAR2 Prototype Test Board (MIMOSTAR_PCB2) before the wire-bonding of the MIMOSTAR2 device.

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Modifications Chronology

VERSION	MODIFICATIONS	CHAPTERS
0.1	Creation of the document.	All
0.2	Modifications/Corrections	All

Chapter 1: Introduction

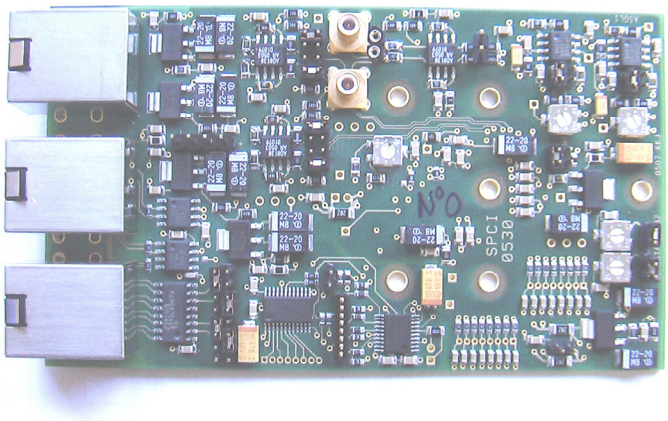

Figure 1.1: the MIMOSTAR2 prototype test PCB (MIMOSTAR_PCB2).

MIMOSTAR Prototype Test Board is developed in order to be able to test MIMOSTAR2 device. This Prototype device is developed by CMOS group at IRES-LEPSI (Strasbourg, France). In Fig 1.1 is presented a figure of the MIMOSTAR_PCB2.

Chapter 2: Tests Description and Scenario

Chapter 2.1: Material and software requirements

- a multi-meter (voltage, resistance, current measurements)
- an oscilloscope
- a waveform generator
- MIMOSTAR_PCB2 board
- Electronics schematics for the MIMOSTAR_PCB2 board (MIMOSTAR_PCB2 User Manual)

Chapter 2.2: Visual verifications

Check all the necessary components are soldered correctly. See Fig. 2.1. for component placements.

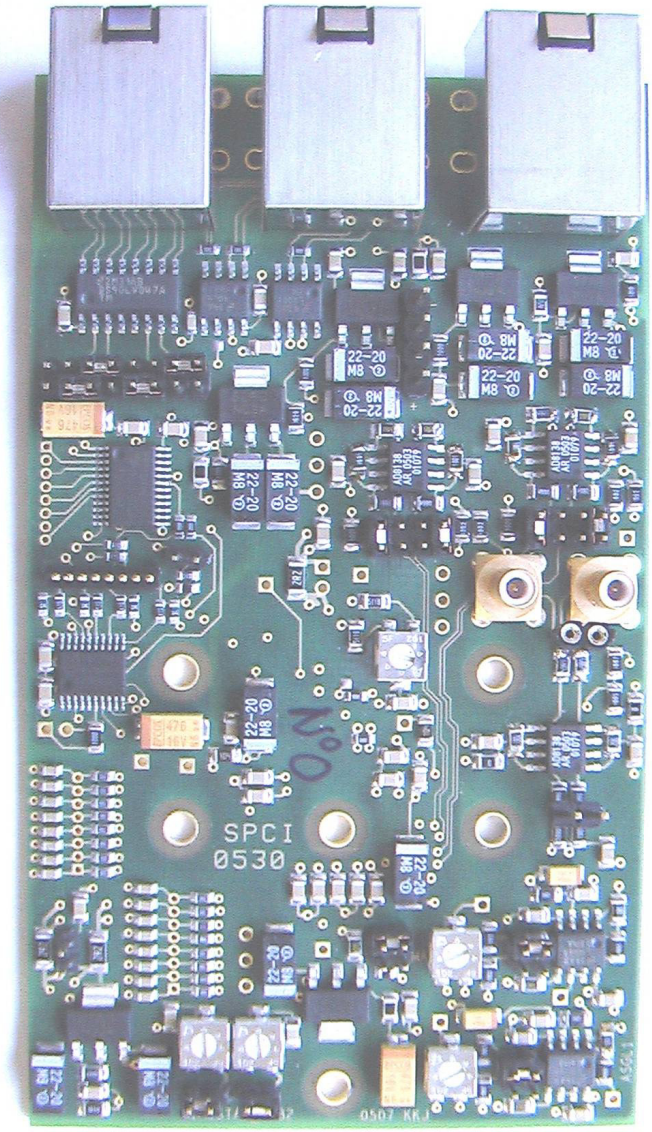

Figure 2.1: Overall view of the PCB with the components.

Check the polarity of capacitors. See the Figure 2.2 for the polarity of the capacitors. The positive voltage connection of capacitors is marked with color red.

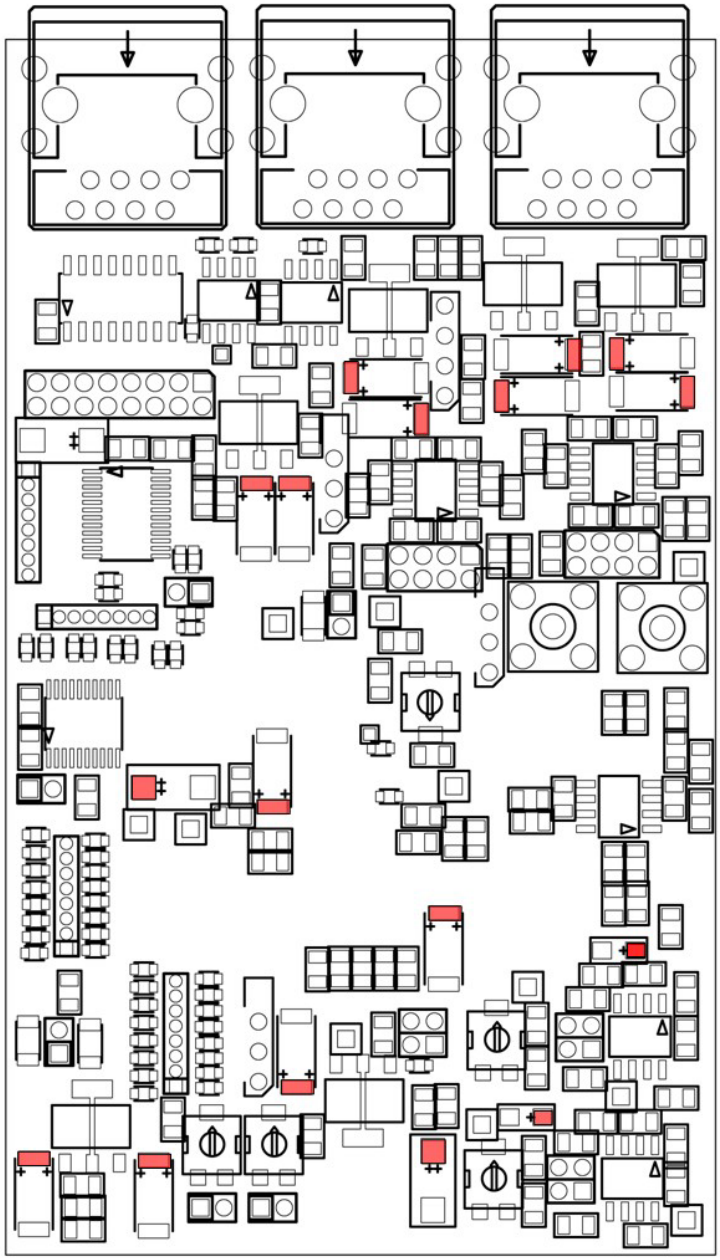

Figure 2.2: Polarity of capacitors for the top part of the PCB.

Chapter 2.3: Power off tests

Do not connect to the power supplies during this test!

- Measure the resistance between the power supplies and GND. The test points are shown in Fig. 2.3 and the values are listed in Table 2.1.

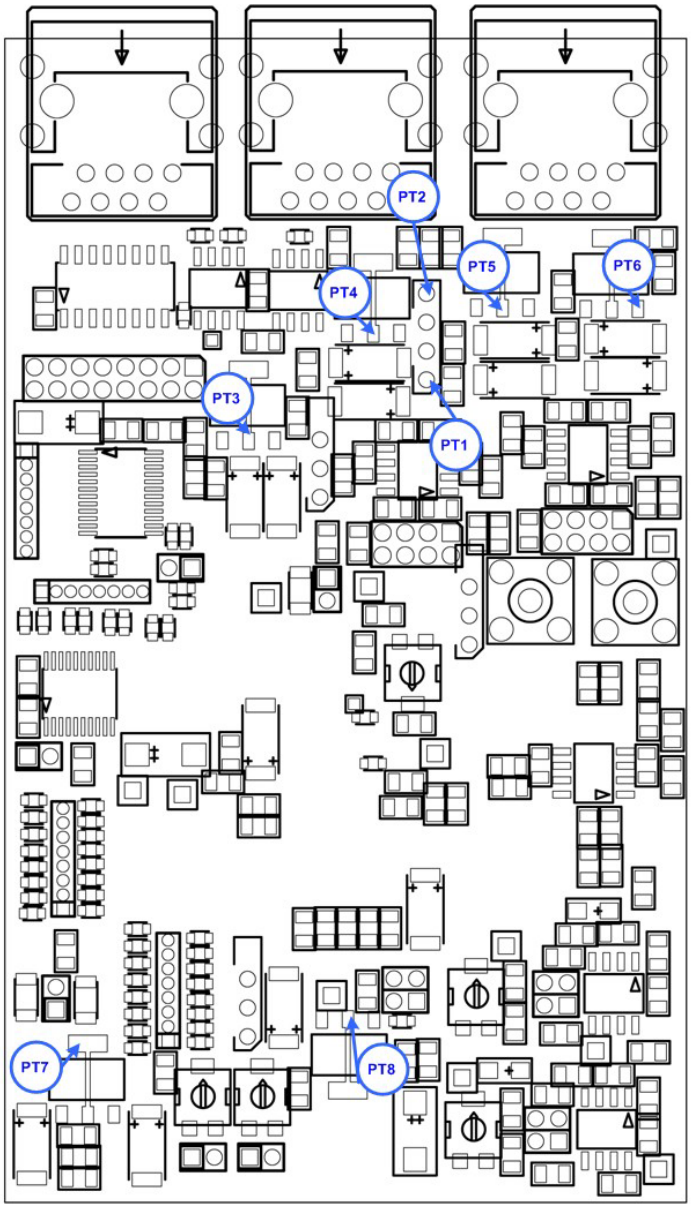

Figure 2.3: Test point to measure resistances between the power supply lines and GND.

NAME	POINT OF TEST	RESISTANCE (OHM) (± 10 %)
VPOWERN	PT1	> 1 M
VPOWERP	PT2	> 1 M
VD5P	PT3	400
VD33P	PT4	262
VA5P	PT5	193
VA5N	PT6	450
VA33P	PT7	262
V125P	PT8	320

Table 2.1: Resistance values between the power supply lines and GND.

Chapter 2.4: Jumper setting

The default jumper and switch setting is shown in Fig. 2.4.

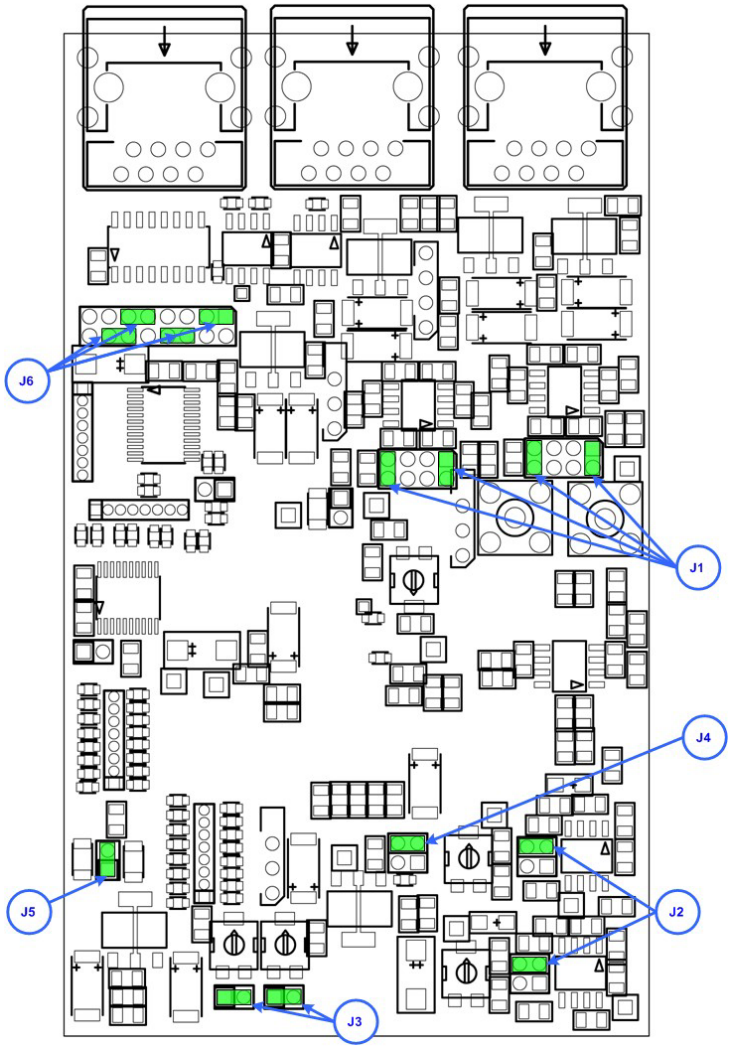

Figure 2.4: The default setting for the jumpers and switches.

These settings correspond following configuration (references J1-J5 are shown in Fig. 2.4) :

- parallel output mode: single-ended (*J1*)
- Adjustment of output offset level for single-ended output mode: on-board potentiometer (*J2)*
- Biasing voltages VDD_DIODE1 and VDD_DIODE2 are connected (*J3*)
- Output signal selection for ASGL1: Normal Matrix Output for Subframe1 (*J4*)
- Analog power supply (3.3V) for MIMOSTAR2 device is connected directly (*J5*)

- LVDS status signals (*J6*)

  LVDSOUT1: LASTROW

  LVDSOUT2: RSTMK

  LVDSOUT3: LASTCOL

  LVDSOUT4: CK10M

For details of signals, see the Chapter 3.6 “MimoStar2 Chronogram” of MIMOSTAR2 USER MANUAL (MIMOSTAR2 device user manual) and for the LVDS status signal jumper pinout, see the Chapter 3.1 “Front-End interface” of MIMOSTAR_PCB2 USER MANUAL.

Chapter 2.5: Corrections

Required corrections of the MIMOSTAR_PCB2 are presented in Fig. 2.5 and Table 2.2.

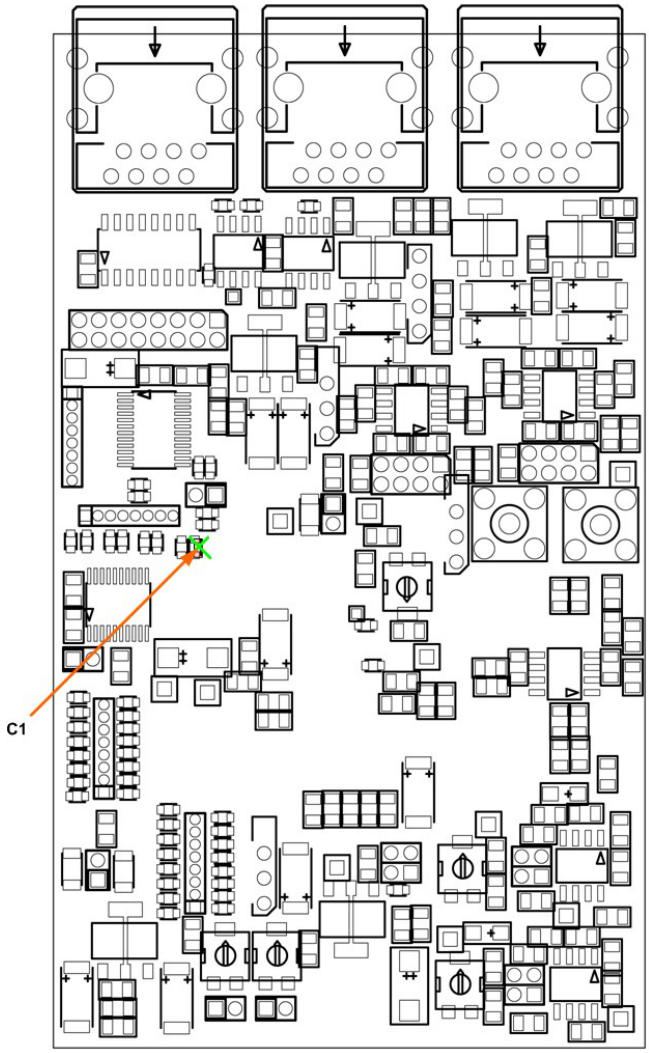

Figure 2.5: Required corrections for MIMOSTAR_PCB2.

CORRECTION	ERROR	REPAIR
C1	Termination of 500 ohm is not valid (signal RSTB).	Remove the resistance R45.

Table 2.2: Table of the required corrections.

Chapter 2.5: Power on tests

- Connect the power supply to the board and switch the power-on. In fo1lowing Table 2.3 is presented the typical current requirements for the board.

POWER SUPPLY VOLTAGE	CURRENT REQUIREMENT
+8.0V (± 100 mV)	350 mA (± 5 %)
-8.0V (± 100 mV)	150 mA (± 5 %)

Table 2.3: Typical current requirements for the board.

- Measure the voltages of the test points (P1…PT8) shown in Fig. 2.6. The voltage values are listed in Table 2.4.

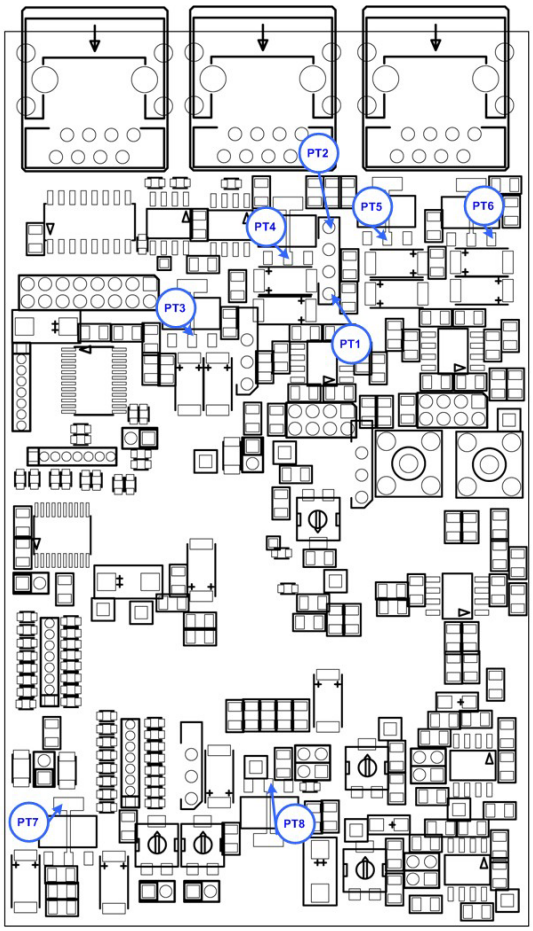

Figure 2.6: The test points for power supplies.

NAME	POINT OF TEST	VOLTAGE (V)
VPOWERN	PT1	-8.0±0.1
VPOWERP	PT2	8.0±0.1
VD5P	PT3	5.0±0.1
VD33P	PT4	3.3±0.1
VA5P	PT5	5.0±0.1
VA5N	PT6	-5.0±0.1
VA33P	PT7	3.3±0.1
V125P	PT8	1.25±0.1

Table 2.4: Voltage values for power supplies.

Chapter 2.6: Analog buffers test

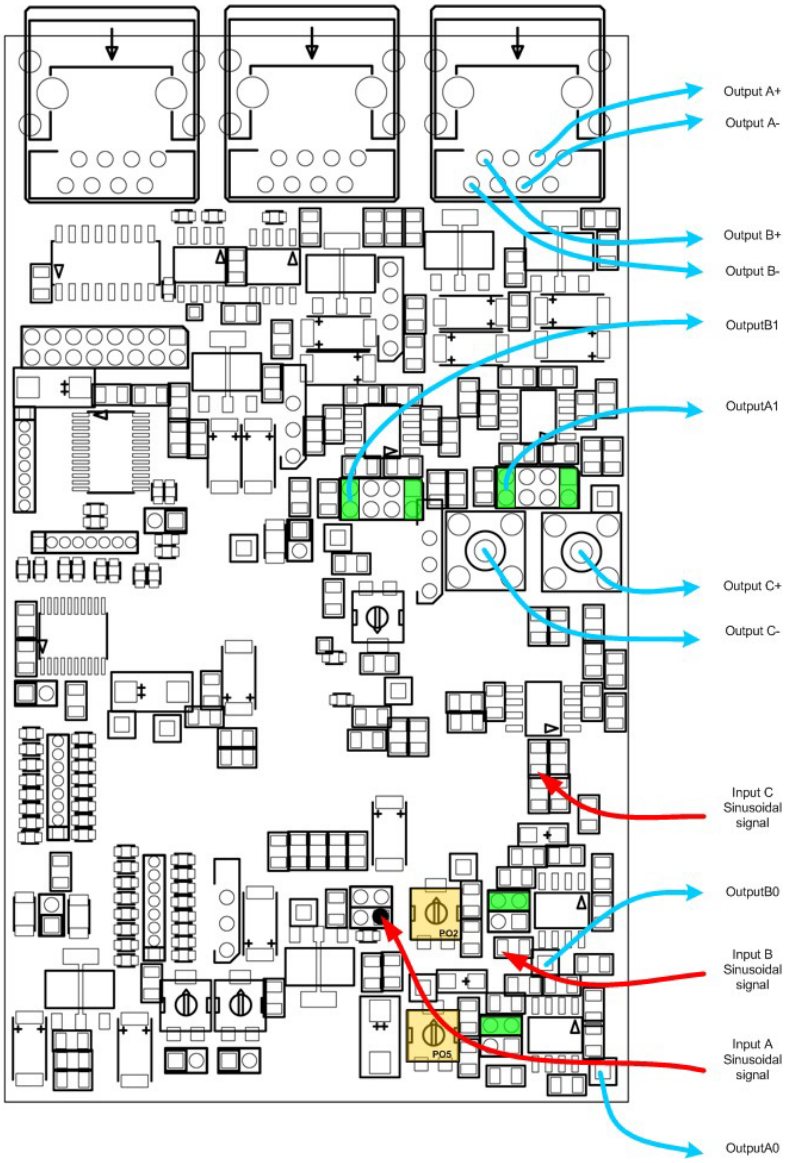

Figure 2.7: Test configuration for the analog buffers.

The MIMOSTAR_PCB2 is equipped with 3 analog buffers. In Fig. 2.7 is shown a test configuration for the analog buffers. This can be done by injecting a sinusoidal signal (frequency of 1 MHz with an amplitude of 1 Vpp and DC offset equal to 0V) to the input points Input A, Input B and Input C. A differential output signal should be available at the corresponding test points Output A± , Output B± and Output C±. The screen prints of the oscilloscope are shown in Fig. 2.8, 2.9 and 2.10. The output signals from the board are not terminated with termination resistance. The signals are observed with a standard oscilloscope probe (10 MΩ, 8 pF, 10X). **This test can be only done when the MIMOSTAR2 device is not mounted!**

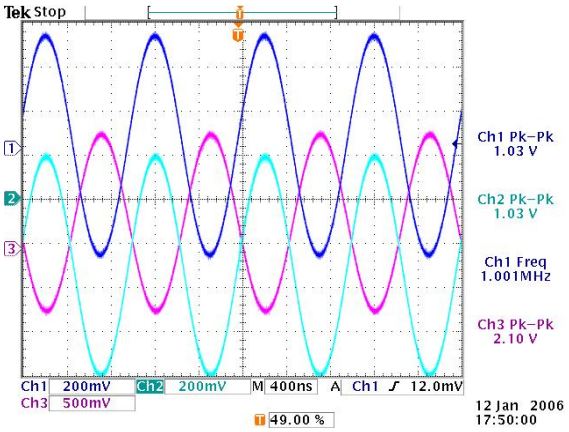

Figure 2.8: Oscilloscope screen print of the signals Input A (1), output A0 (2) and output A1 (3).

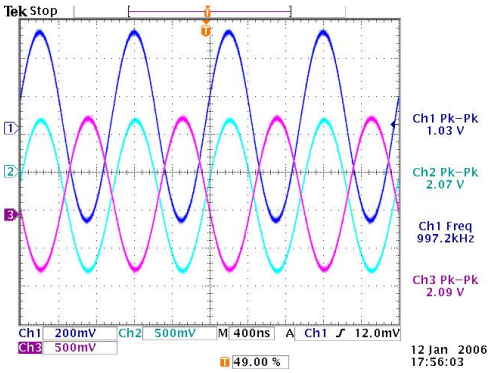

Figure 2.9: Oscilloscope screen print of the signals Input A (1), output A- (2) and output A+ (3).

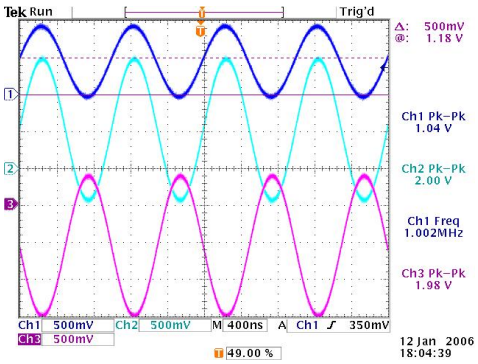

Figure 2.10: Oscilloscope screen print of the signals Input C (1), output C+ (2) and output C- (3).

Chapter 2.7: JTAG interface test

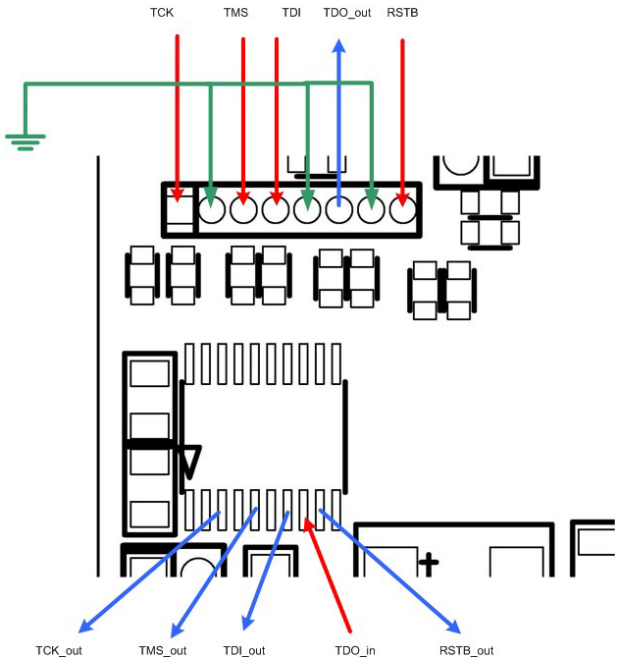

Figure 2.11: Test configuration for the JTAG interface.

In Fig. 2.11 is shown a test configuration for the JTAG interface. A standard TTL input test signal (a clock signal of 10 MHz) is injected to the inputs (TCK, TMS, TDI, TD0_in and RSTB) and the corresponding output signal is available at the output points (TCK_out, TMS_out, TDI_out, TDO_out and RSTB_out). The verification is done with a standard oscilloscope probe (10MΩ, 8pF, 10X). The screen print of the oscilloscope is shown in Fig. 2.12.

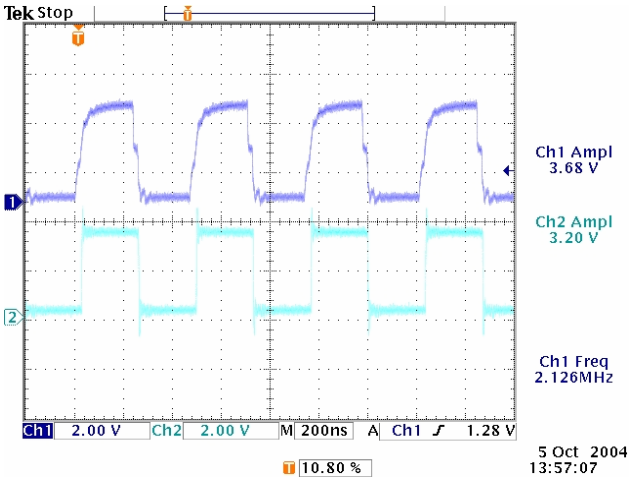

Figure 2.12: Oscilloscope screen print of the signals: RSTB (1) and RSTB_out (2).

Chapter 2.8: LDVS interface test

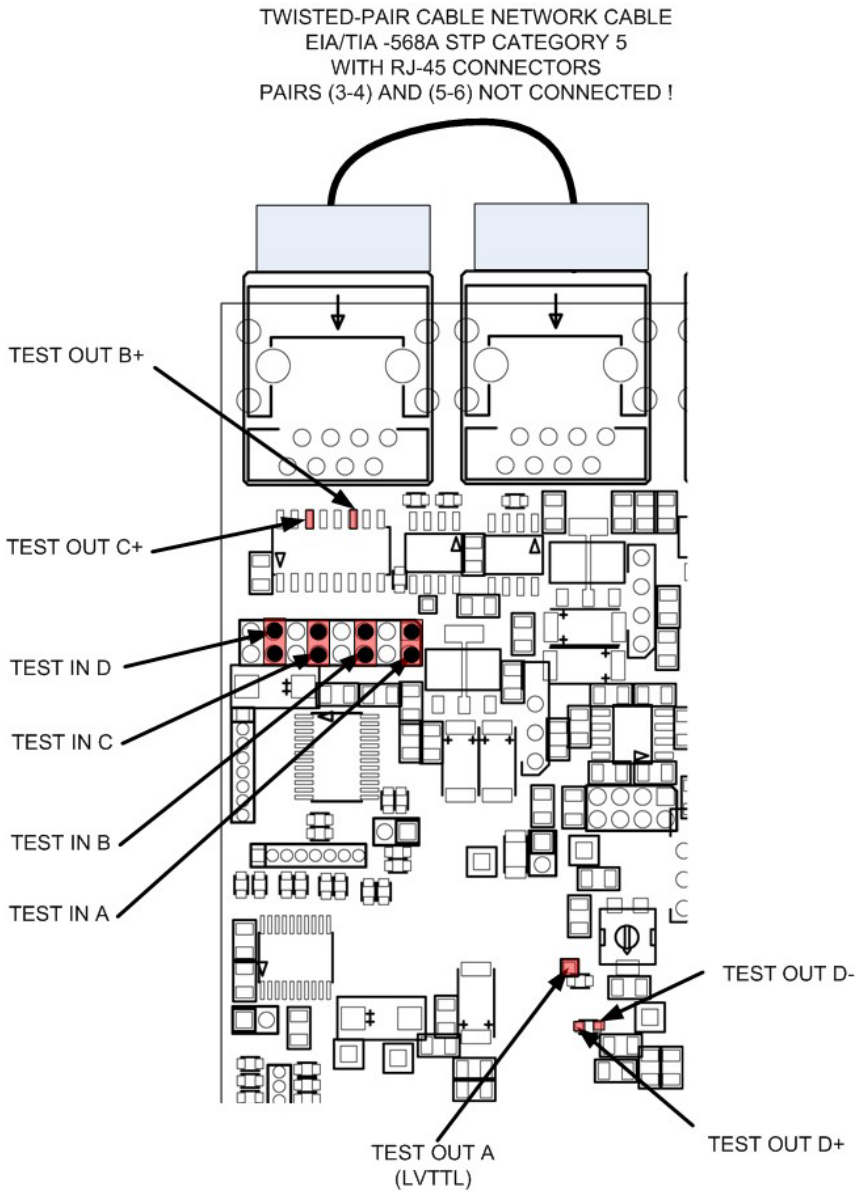

Figure 2.13: Test configuration for the LVDS interface.

In Fig. 2.13 is shown a test configuration for the LVDS interface. Two RJ-45 connectors are connected together by the standard twisted-pair network cable. A TTL-level input signal is injected to the test inputs (TEST IN A, TEST IN B, TEST IN C and TEST IN D) and the corresponding LVDS output signal is available at the test point (TEST OUT A, TEST OUT B+, TEST OUT C+ and TEST OUT D±). The screen print of the oscilloscope is shown in Fig. 2.14 for the signals TEST IN D and TEST OUT D±.

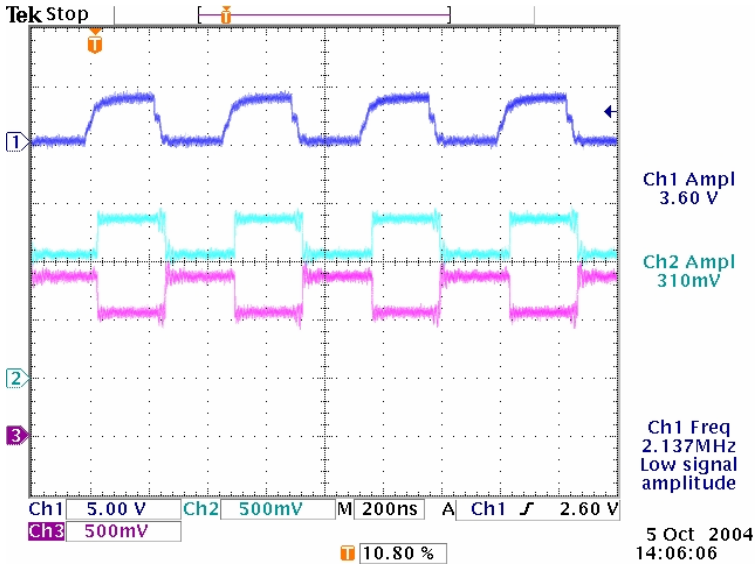

Figure 2.14: Oscilloscope screen print of the signals: TEST IN D (1), TEST OUT D+/- (2,3) .

Chapter 2.9: Adjustment of the AFIX voltage

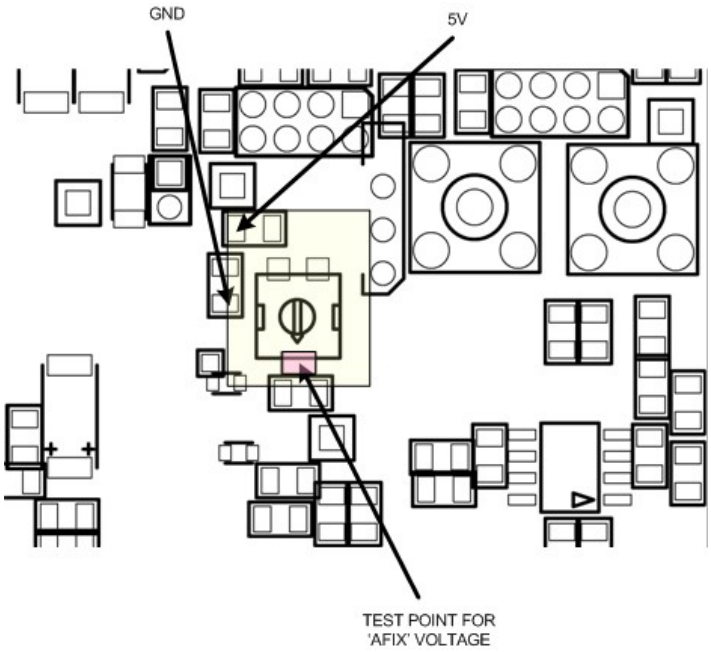

Figure 2.15: Adjustment of the AFIX voltage.

A polarity voltage AFIX is adjusted by using the potentiometer (ref. PO1) shown in Fig 2.15 The voltage at the test point 'AFIX' should be 1.5 V. The AFIX voltage is used to set voltage level for 8 non-existing subframes on serial output analogue data (For details, see the Chapter 3.5.1.2 "Serial Mode" of MIMOSTAR2 USER MANUAL).

Chapter 2.10: Adjustment of the VDD_DIODE BIAS voltages

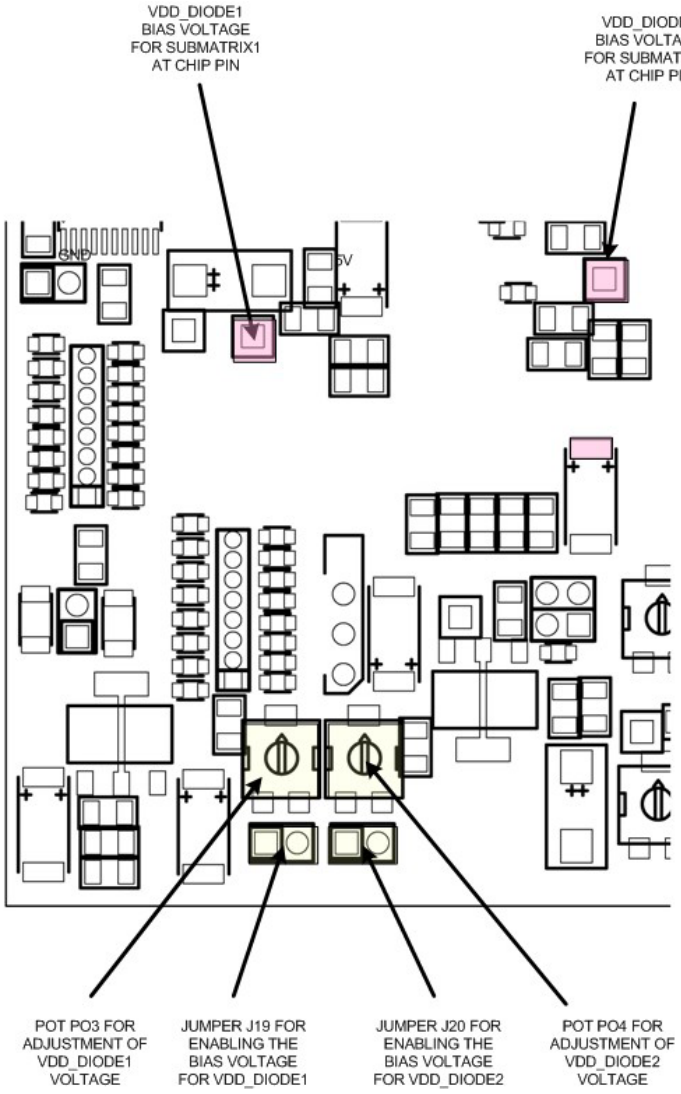

Figure 2.16: Adjustment of the VDD_DIODE BIAS voltages.

In Fig. 2.16 is shown the adjustment of the VDD_DIODE bias voltages. As a default, VDD_DIODE bias voltages are set to 3.3V. If the jumpers J19 and J20 are not mounted the VDD_DIODE bias voltages are 0Vand the subframes are not biased.

Appendix A TEST REPORT (MODEL)

TEST DATE AND USER	VALUE
NAME	Kimmo JAASKELAINEN
DATE	31/08/2005

1. BOARD IDENTIFICATION

BOARD IDENTIFICATION PARAMETER	VALUE
BOARD NUMBER	MIMOSTAR_PCB2 No 1
BOARD DATE	30/08/2005

2. POWER-OFF AND POWER-ON TESTS

Power supply voltages and currents on stand-by state

POWER SUPPLY	MEASURED VOLTAGE (V)	MEASURED CURRENT (mA)
+8.0V	+8.0V	350
-8.0V	-8.0V	145

Measurement of the power supply voltages and resistances

NAME	NOMINAL VOLTAGE (V)	POINT OF TEST	MEASURED RESISTANCE (Ohm)	MEASURED VOLTAGE (V)
VPOWERN	-8.0V	PT1	> 1 MOhm	8.0
VPOWERP	8.0V	PT2	> 1 MOhm	-8.0
VD5P	5.0V	PT3	400	5.08
VD33P	3.3V	PT4	365	3.28
VA5P	5.0V	PT5	193	5.07
VA5N	-5.0V	PT6	450	-5.00
VA33P	2.5V	PT7	365	3.28
V125P	1.25V	PT8	320	1.31

2. FUNCTIONAL TESTS

TEST	STATE	DESCRIPTION
ANALOG BUFFERS	OK	Input signal 1.0 Vpp
JTAG INTERFACE TEST	OK	Input signal 1MHz clock signal (TTL level)
LVDS INTERFACE TEST	OK	Input signal 1MHz clock signal (TTL level)
SETUP AFIX VOLTAGE	OK	1.5V
ADJUSTMENTS OF VDD_DIODES	OK	3.3V for VDD_DIODE1 and VDD_DIDODE2