Documentation of CDS1 chip

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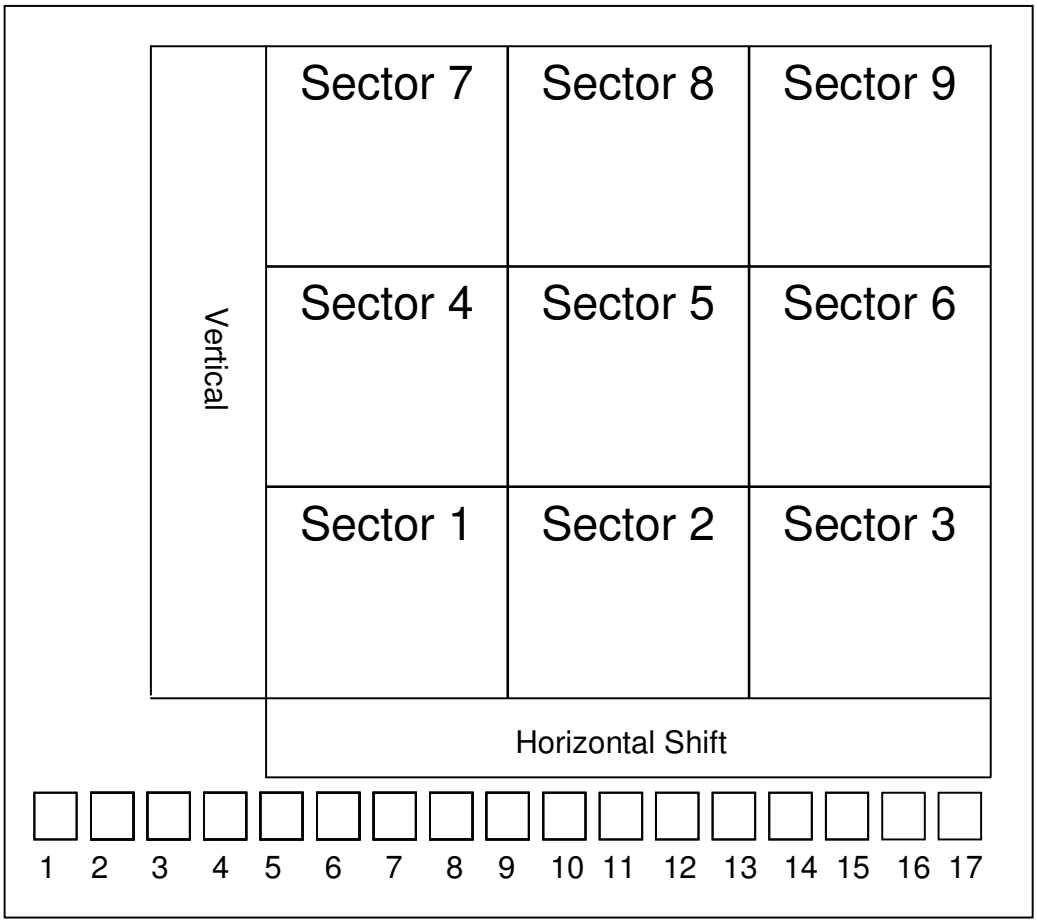
Chip Layout:



The chip is divided into 9 sectors with each sector containing 32x32 pixels. The total of all the 9 sectors is 96x96 pixels. The total area of the chip is 9.855 sq. millimeters. The x and y dimensions are as follows: 3055x3227 microns.

The technology used: Austriamicrosystems 0.35 micron CMOS opto process C35B4 (4 metal).

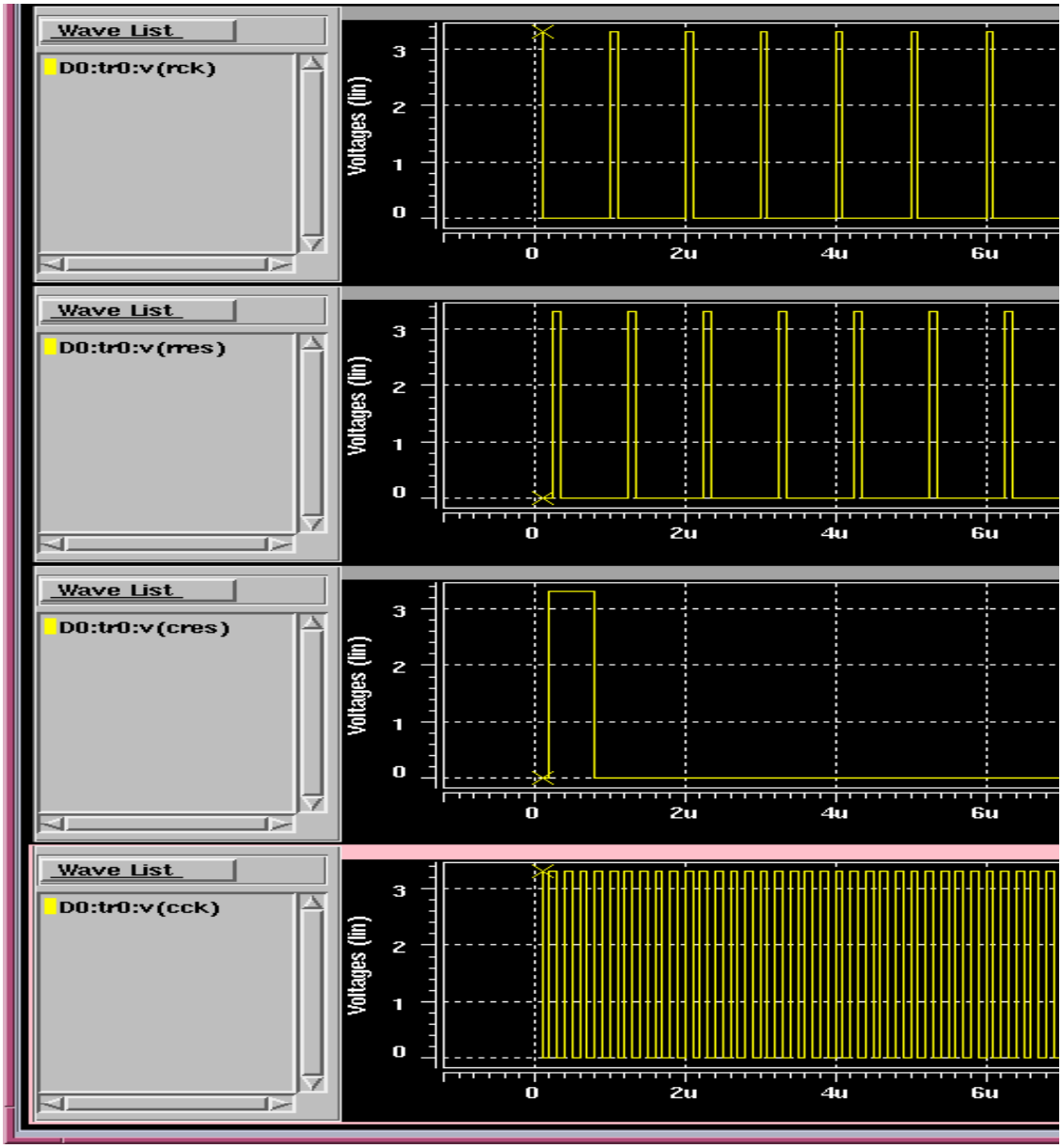
Pad List

Bonding #	Pad #	Description
61	1	Digital Power Supply, Vdd 3.3 V
62	2	Row shift register reset, rres
63	3	Column shift register reset, cres
64	4	Row clock-in, rck
65	5	Column clock-in, cck
66	6	Gnd (Digital)
67	7	Gnd (for column current source and output pad)
68	8	Output pad
1	9	Vdd (for in-pixel source follower and output pad) 3.3V
2	10	Iout for source follower in output pad
3	11	Iin for column current source 100u
4	12	Sample
5	13	Reset 1
6	14	Reset 2
7	15	Pixel bias .7V
8	16	Gnd
9	17	Gnd

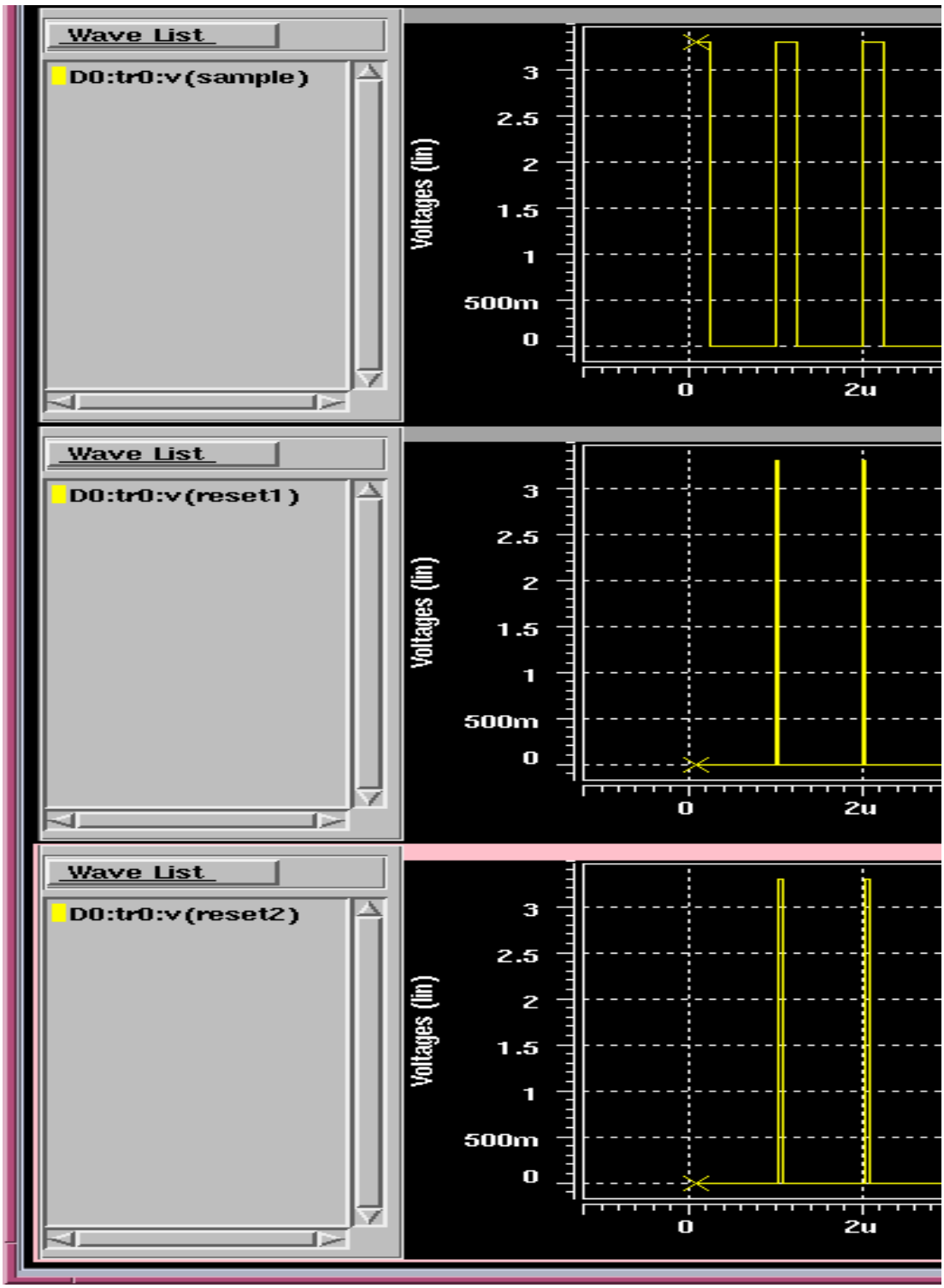
Sector List

Sector #	Description
1	CDS (Correlated double sampling) with diode size 12x12 lambda and optimum capacitor size, C2=224fF C3=238.4fF
2	CDS with diode size 12x12 lambda and $\frac{1}{2}(C2, C3)$ C2=113.6fF C3=120.3fF
3	CDS with diode size 12x12 lambda and $\frac{1}{4}(C2, C3)$ C2=55fF C3=60.2fF
4	CDS with diode size 17x17 lambda and optimum capacitor size
5	CDS with diode size 24x24 lambda and optimum capacitor size
6	CDS with diode size 32x32 lambda and optimum capacitor size
7	APS (Active Pixel Sensor) with diode size 17x17 lambda
8	APS with diode size 24x24 lambda
9	APS with diode size 32x32 lambda

Timing Diagrams



Hspice:
V1 rres GND pulse(0 3.3 250n 0n 0n 100n 1000n)
V2 cres GND pulse(0 3.3 200n 0n 0n 600n 25u)
V3 rck GND pulse(0 3.3 0n 0n 0n 100n 1000n)
V4 cck GND pulse(0 3.3 0 0n 0n 100n 200n)
V5 sample GND pulse(0 3.3 0 0n 0n 250n 1000n)
V6 reset1 GND pulse(0 3.3 0 0n 0n 40n 1000n)
V7 reset2 GND pulse(0 3.3 20n 0ns 0ns 60ns 1000ns)


Wave List
D0:tr0:v(sample)
Voltages (lin)
3
2.5
2
1.5
1
500m
0
0
2u
Wave List
D0:tr0:v(reset1)
Voltages (lin)
3
2.5
2
1.5
1
500m
0
0
2u
Wave List
D0:tr0:v(reset2)
Voltages (lin)
3
2.5
2
1.5
1
500m
0
0
2u

Background Information:

Definitions: *Active-pixel sensors* reduce the noise associated with passive-pixel sensors. It is this active circuitry that gives the active-pixel device its name. The performance of this technology is comparable to many charge-coupled devices and also allows for a larger image array and higher resolution. *Correlated Double Sampling* is a method to read the differential magnitude of a charge packet, thereby canceling a source of FPN, as well as the kTC noise that is caused by the reset of the charge packet[1].

Correlated Double Sampling, or CDS, is a method employed to improve the signal to noise ratio (S/N) of integrating image sensors. By subtracting a pixel's dark or reference output level from the actual light-induced signal, static fixed pattern noise (FPN) and several types of temporal noise are effectively removed from the sensor's output.

In an optical sensor the photocharge is generally collected on a capacitor. The signal amplitude is read as the voltage over that capacitor (V=Q/C). With the CDS procedure the signal voltage Vs=Qs/C is compared with the "dark" or "empty" or "reset" level voltage Vr = Qr/C that is obtained when all charges of C have been channeled off to a fixed potential. Thus for each pixel the final output V = Vs-Vc = (Qs-Qr)/C.

Spatial and temporal noises that are *common* to Vr and Vs disappear from the result:

- fixed pattern noise (spatial noise, static non-uniformity)
- KTC noise of the photodiode's capacitance, on the condition that this capacitance is not reset inbetween measuring Vs and Vr: if the capacitor is reset inbetween the two sampling instants, their noises are uncorrelated and kTC noise persists. (One sometimes calls this method of readout Double Sampling, DS, in contrast to CDS.

Presenting a pixel's pre-exposure reset level and post-exposure actual signal simultaneously to a subtractor, requires that the pixel memorise one or both of these signals for a certain period of time: analogue pixel memory is needed.

[1] Reference: FillFactory Image Sensors

Design Procedure:

Reference paper: V. Douence, et al. "Hybrid Image Sensor with Multiple On-chip Frame Storage for Ultra High-speed Imaging" High-Speed Photography and Photonics, Proc. Of SPIE Vol. 5580

Input referred noise power with the proposed CDS approach is given by the following equation:

$$< Q >_n^2 \sim \left(\frac{C\,\mathrm{int}}{Asf} \right)^2 \left[\frac{5}{3} kT / C2 + kT / C3 \right] = kTC\,\mathrm{int} \left[\frac{5C\,\mathrm{int}}{3Asf^2 C2} + \frac{C\,\mathrm{int}}{Asf^2 C3} \right]$$

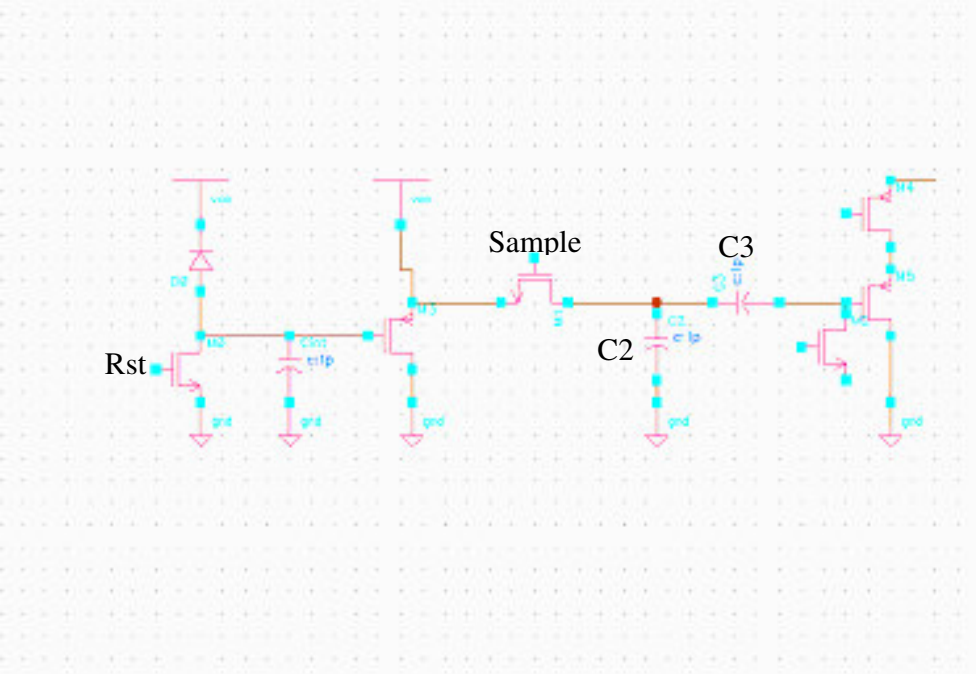
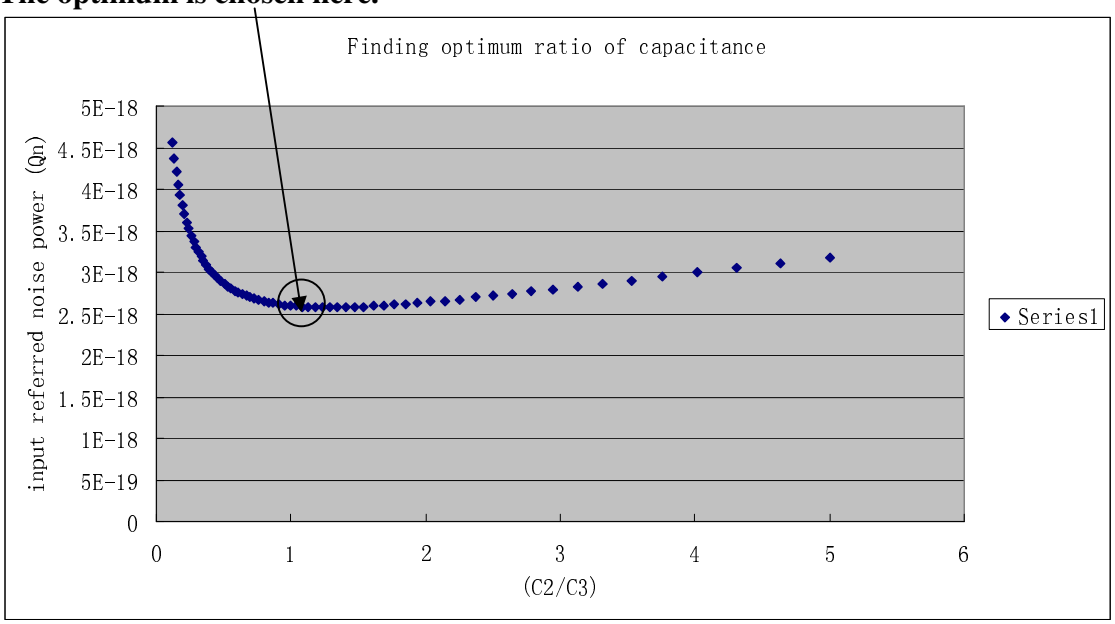


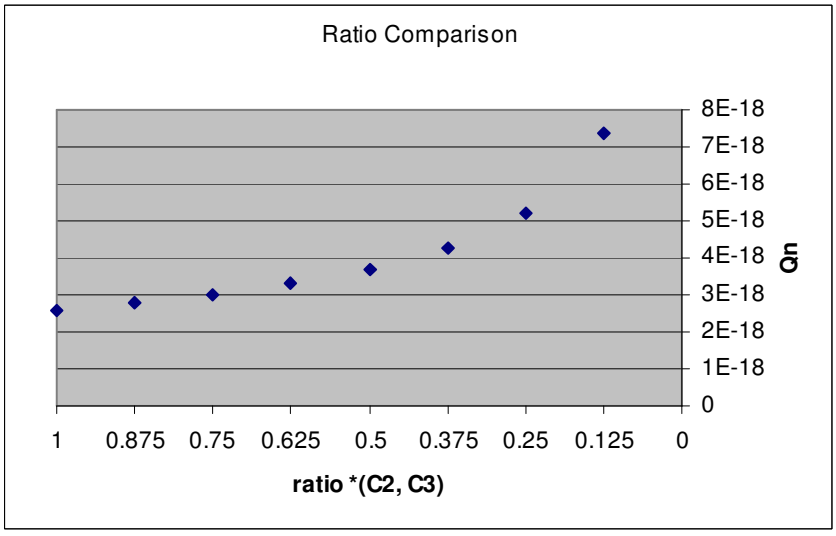
Fig 1. Pixel schematic with an Input Source Follower

The source follower buffers the integration node with the sampling capacitors C2/C3. Cint is the total integration capacitance.

The maximum area in the layout that we can have for capacitance is roughly 462fF. The optimum is chosen here.

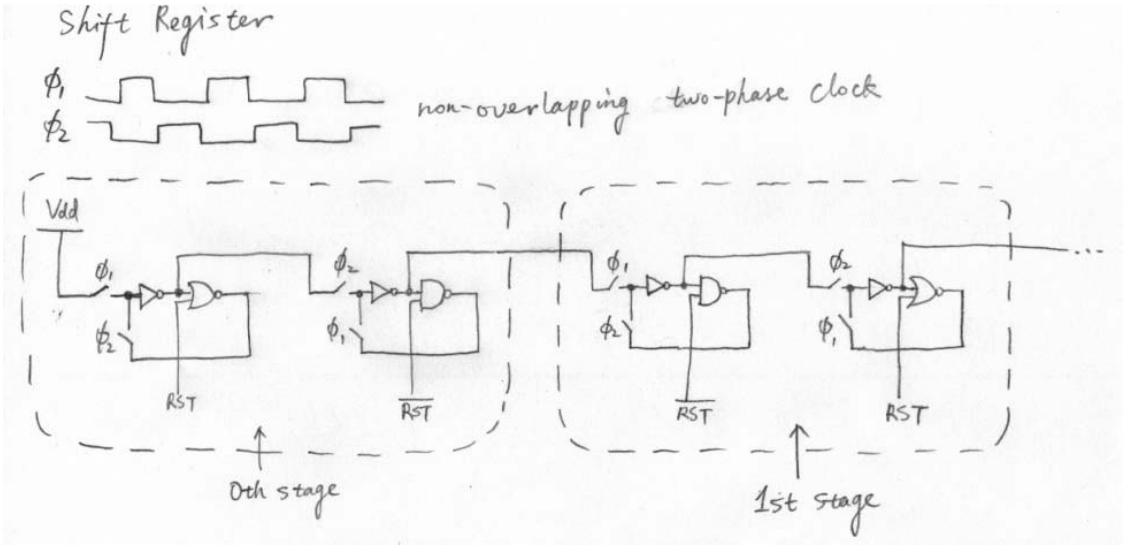


After taking the optimum capacitive sizes, we multiplied it with different ratios to see its effects.



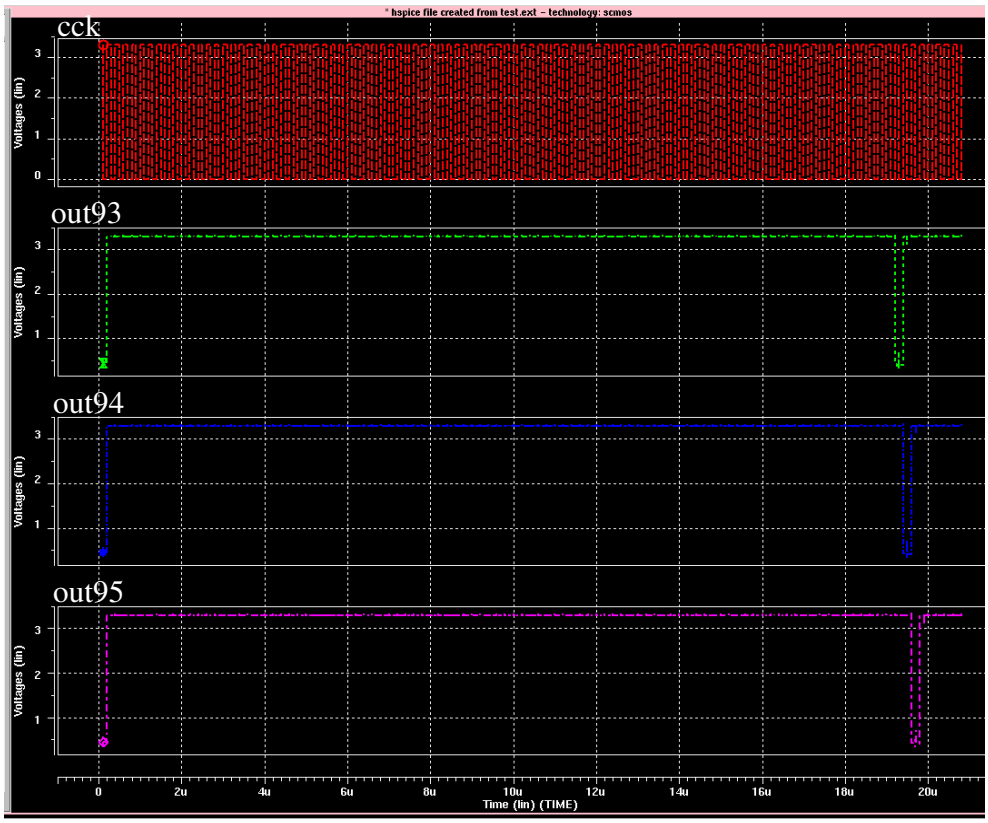
We decided to use equal ratios of (1/2) and a (1/4) which you see in sectors 2 and 3.

Shift Registers:



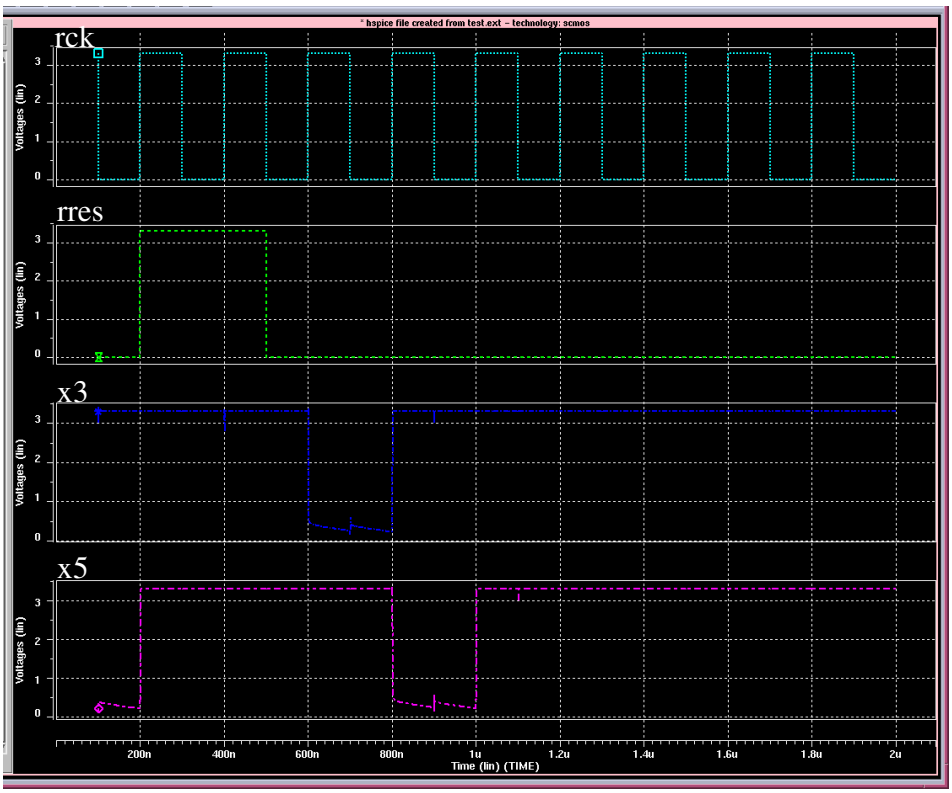
Simulations:

Horizontal Shift Register simulations show that it is operating normally.



Vertical Shift Register:

Verification that the vertical shift registers is operating correctly.



Current-source requirements, such as what value resistance to use, and which way it's hooked up.

Conclusion:

Test results will show what needs to be done for future study.