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May 2009 Latch up tests - report

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LU & SEU testing goals

The new MAPS prototypes that have recently become available (Phase-1 and SUZE) feature sensor and electronics architectures that are very similar to what is going to be used in the PIXEL detector in STAR. The primary reason to measure latch up in these prototypes was to quantify their sensitivity to latch up and single event upsets and to compare these results to the previously studied MimoSTAR2 [1].

Latch up test goals:

1. Measure latch up cross-section in Phase-1 and SUZE
2. Measure single event upsets (SEU) in Phase-1
3. (Optional) Measure latch up and possible SEU in Mimosa 22 (small scale predecessor of Phase-1)

The SEU measurements were added to the testing plan to allow for qualitative and quantitative study of soft errors that do not result in latch up. Evidence of such effects was observed in the digital marker/analog readout monitoring system during the tests of MimoSTAR2. However, at the time of MimoSTAR2 tests, the test system was limited to registering latch up events only.

Goals of SEU analysis

- Measure onset of errors
- Check for the likelihood of corruptions 0-to-1 and 1-to-0
- Check if bit corruptions are equally likely in different registers and at different positions in registers

1 http://rnc.lbl.gov/hft/hardware/docs/latchup/Latch_up_tests_doc_v2.pdf

Test procedure

The testing procedure was designed based on the experience obtained with MimoSTAR2 tests in summer 2006 at TVDG SEU test facility at Brookhaven National Laboratory.

The ion species used in the test were chosen for delivering the appropriate LET ranges are shown in the table:

Ion	Energy MeV	LET(Si) MeV cm^2/mg
O-16	126	2.58
F-19	140	3.38
O-16	80	3.47
F-19	90	4.42
F-19	70	5.06
F-19	65	5.25
F-19	50	5.94
Si-28	182	7.97
Cl-35	199	11.73
Cl-35	70	16.67
Ni-58	256	26.58
Br-81	278	37.47

The time for the test was planned assuming 15 minutes for changing a beam type (and/or energy) and a typical exposure time of 2 min. Reaching vacuum in the test system takes only about 5 minutes. It was decided to perform LET scans for one sensor at a time to optimize handling of the prototype devices. The testing time reserved for each ion beam and per sensor was 15 min, totaling at 30 minutes per scan point per sensor. The total time for latch up and SEU tests for the three prototypes was 16 hours. We scheduled testing time at the BNL Tandem SEU test facility to do latch up testing on May 14-15, 2009. The reserved time was sufficient and, at the same time, efficiently used.

The majority of the measurements were performed with the chips programmed and running – the condition that is closest to the real operating condition. A couple of tests were dedicated to verifying if the latch up rate depends is different if the sensor is fully operational than if it is only powered on.

Measurement of SEU was based on the periodic sending/reading of a JTAG programming sequence to/from the device under test and checking for corrupted bits in the returned sequence. The frequency of JTAG programming was varied between 3, 5, and 10 seconds to check if the data refreshing rate would affect the measured SEU rate.

Test setup

The diagram of the test setup used in the test is presented in Figure 1. The system was assembled mostly with components that had been developed for the PIXEL detector. This includes:

1. The RDO board assembly that was designed to control and read out four detector ladders (40 sensors) [2]. The system featured an adapter board that provides an interface to single-sensor test boards that was used in the latch up tests in this configuration. The RDO board provided the JTAG programming module for the programming of the tested sensors.
2. The power supply boards that provide 3.3 V power to sensors and feature latch up detecting circuitry [3]. When current delivered to the sensor exceeds an adjustable threshold, the system cuts the power off and signals this by asserting a logical "1" on a dedicated digital signal line. Power is restored when the digital control/monitor line is forced to a logical "0". Each power supply board delivers two 3.3 V sources. However for this test, we used separate boards for analog and digital power supplies. Power boards are designed to mate with a mass termination board whose primary purpose is to provide latch up monitored power and digital signal buffering to/from 4 ladders of the PIXEL detector [4]. This board provides unregulated 6V power to the power supply boards.

In addition to the hardware developed for the PIXEL detector, the system contained:

3. Latch up monitoring/resetting circuitry based on a National Instruments USB-6800 DAQ. This allowed for easy interfacing of the monitoring signals to a PC for automated registering and resetting of latch up events in the LabView environment [5].
4. PC running LabView software for automated registering of latch up events and resetting power to DUT as well as initializing the JTAG programming and checking for SEU errors in the returned data stream.

A set of cables was developed to provide compatibility between standard feedthrough in the vacuum tank and standard cables used for sensor testing in laboratory conditions [6]. The connection of a Phase-1 sensor in the test setup is shown in Figure 2.

The latch up detection thresholds were set to the following values:

Chip	VDA (chip running)	VDD (chip running)	VDA LU threshold	VDD LU threshold
Phase-1	132 mA	162 mA	200 mA	235 mA
SUZE	(FIFO) <3 mA	60 mA	60 mA	108 mA
Mimosa-22	70 mA	52 mA	120 mA	100 mA

2 http://rnc.lbl.gov/hft/hardware/docs/Phase1/Pixel_RDO_main_V5_int_motherboard.pdf
3 http://rnc.lbl.gov/hft/hardware/docs/latchup/LU_POWER_PCB.pdf
4 http://rnc.lbl.gov/hft/hardware/docs/Phase1/PIXEL_RDO_MASS_TERM_V1.pdf
5 http://rnc.lbl.gov/hft/hardware/docs/latchup/Latch_up_tests_2009_schematic_page2.pdf
6 http://rnc.lbl.gov/hft/hardware/docs/latchup/Latch_up_tests_2009_schematic_page1.pdf

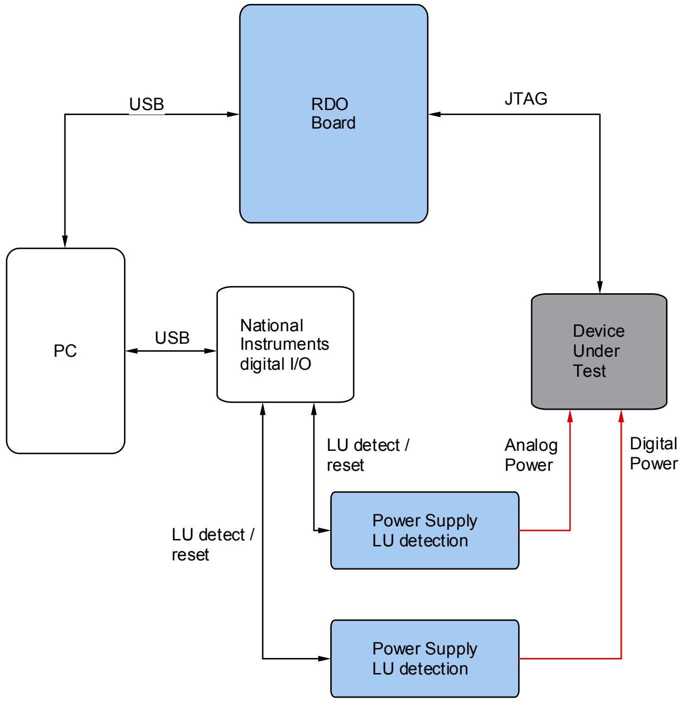


Figure 1 Diagram of the test setup used for Phase-1, SUZE and Mimosa22 latch up tests.

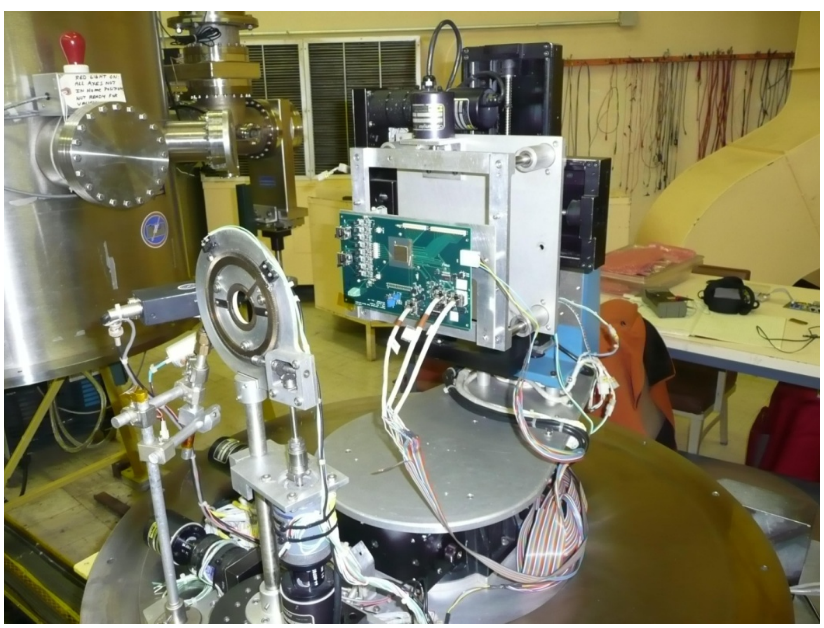


Figure 2 Phase-1 test board mounted to a support frame with sensor facing the iris that allows users to adjust the test beam diameter. The table on which the system is mounted is the bottom part of a vacuum tank visible in the background on the left.

Latch up test results

The measured latch up cross-sections are summarized in Figure 3. The results obtained or Phase-1, SUZE, and Mimosa22 are compared with the latch up cross-section measured for MimoSTAR2. Data points at 1e-10 indicate that the measurement was performed at the given LET but no latch up events were registered.

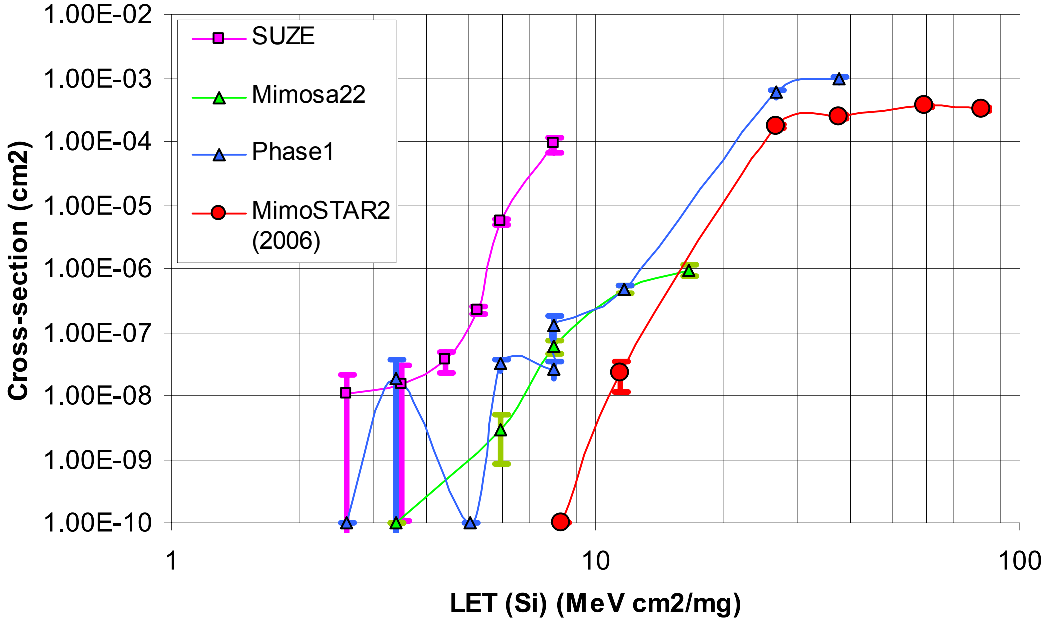


Figure 3 Latch up cross-sections for Phase-1, SUZE, and Mimosa22 compared with results obtained for MimoSTAR2 in tests conducted in 2006.

Data in the plot is a subset of all measurements that were performed. The runs with latch up events occurring at the reset frequency of the test system (a few Hz) have been removed from the data pool to avoid biasing measurements. An example of such biased data is presented in Figure 4.

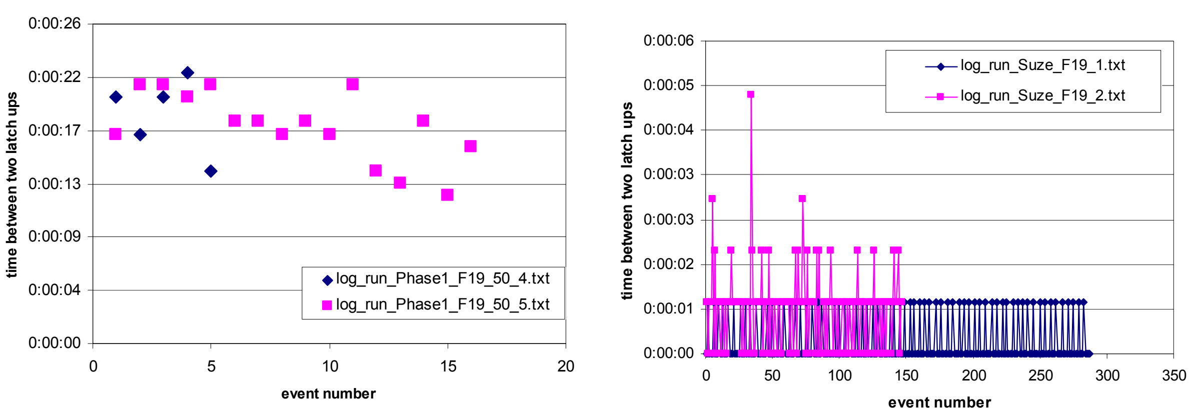


Figure 4 Examples of latch up measurements with appropriate frequencies of events (a) and frequencies of events that are limited by the system reset time (b). Time between consecutive latch up events is shown as a function of the event number during an exposure to an ion beam.

It is clearly visible from Figure 3 that the digital chip, SUZE, has the lowest value of latch up cross-section. It is about a factor of 5 more sensitive than the MimoSTAR2 sensor. All latch-up detected in SUZE occurred on the VDD-FIFO supply line.

The latch up events that were registered for Phase-1 and Mimosa22 can be separated into events associated with analog and digital power lines. This is shown in Figure 5 and Figure 6. Error bars are not shown because they are smaller or similar in size to the marker points used in these plots.

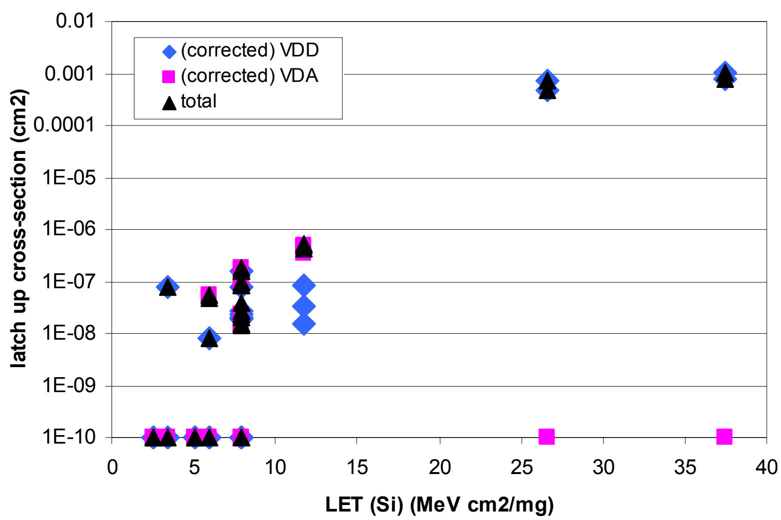


Figure 5 Latch up cross-section measured for Pahse-1 with distinction between latch up events registered on the analog and digital power supplies.

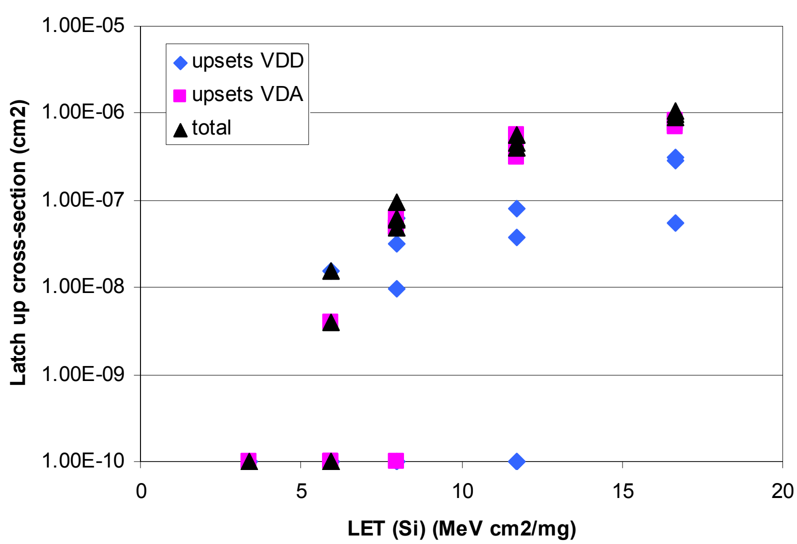


Figure 6 Latch up cross-section measured for Mimosa22 with distinction between latch up events registered on the analog and digital power supplies.

A dependency of the latch up cross-section in analog vs. digital power supply can be observed in both sensors. In case of Phase-1, it appears that it is more likely to have a latch up on an analog rather than digital power supply for LET values below 15 MeV cm^2/mg. The dependency is reversed for higher LET values.

Similarly, for Mimosa22 the latch up cross-sections seem to invert above approximately 7 MeV cm^2/mg. However, in this case, unlike for Phase-1, the cross-section of latch up events on the analog power supply dominates above the threshold.
This effect is not understood and could be related to the geometry of the sensors or a strange artifact in the measurements.

SEU test results

Measured SEU cross-sections are summarized in Figure 7. Data points at 1e-10 for Phase-1 and 1e-8 for Mimosa22 indicate that a measurement was performed at the given LET but no SEU events were registered.

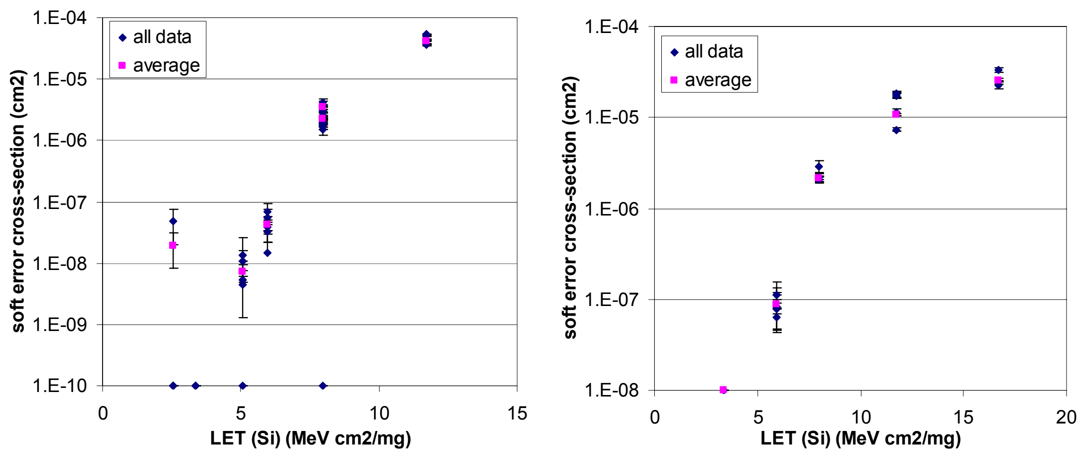


Figure 7 SEU cross-section measured for Phase-1 (a) and Mimosa22 (b). Points at 1e-10 (Phase-1) and 1e-8 (Mimosa22) indicate measurements that yielded no errors.

Complete sets of runs for different ion species and in different sensor configurations are presented in Figure 8 and Figure 9 for Phase-1 and Mimosa22 prototypes, respectively. The plots show the ratio of error rates for bits originally set to 0 over bits originally set to 1 as a function of LET.
Data is arranged with the LET of ion beams increasing, and within each set a chronological order is shown. The LET scan was not performed in a chronological order because it had to be adjusted on-the-fly based on the observations made during the allocated testing time.

Different operating configurations were tested in different runs, including:

- 10, 5, and 3 second JTAG refreshing time - denoted with the number 10, 5, and 3 above data points)
- Runs with data patterns with extra "1" that would not be used in normal operation (disable column register, discriminator test patterns) - denoted with the letter "P" above data points
- Runs with sensors programmed but not running (no START signal sent) – denoted with the letter "N" above data points

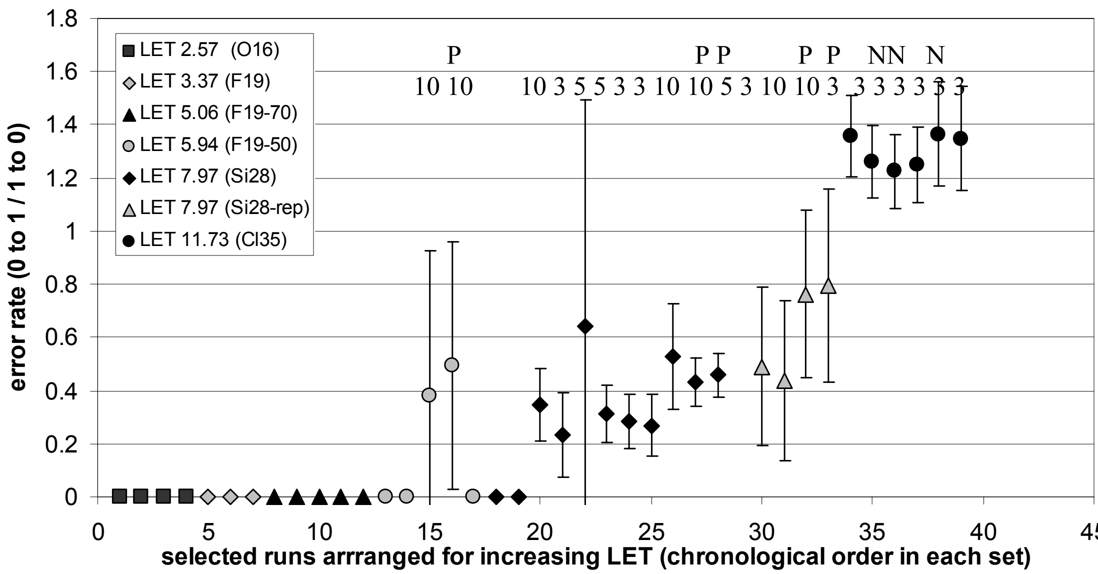


Figure 8 Ratio of error rates (0-to-1 over 1-to-0) for Phase-1 as a function of different LET of ion beams and different operating configurations.

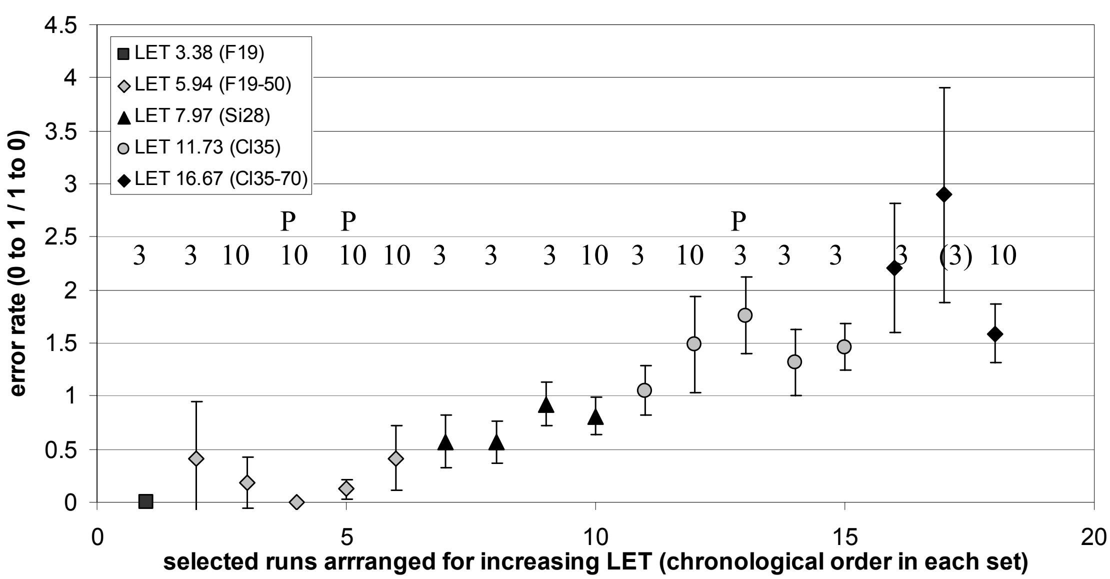
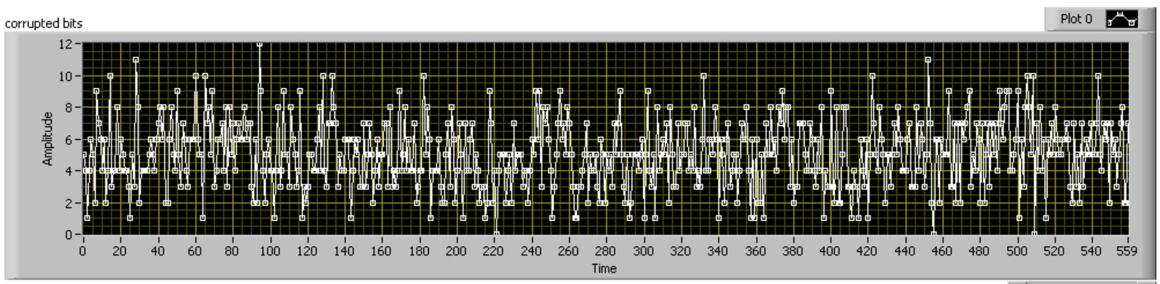


Figure 9 Ratio of error rates (0-to-1 over 1-to-0) for Mimosa22 as a function of different LET of ion beams and different operating configurations.

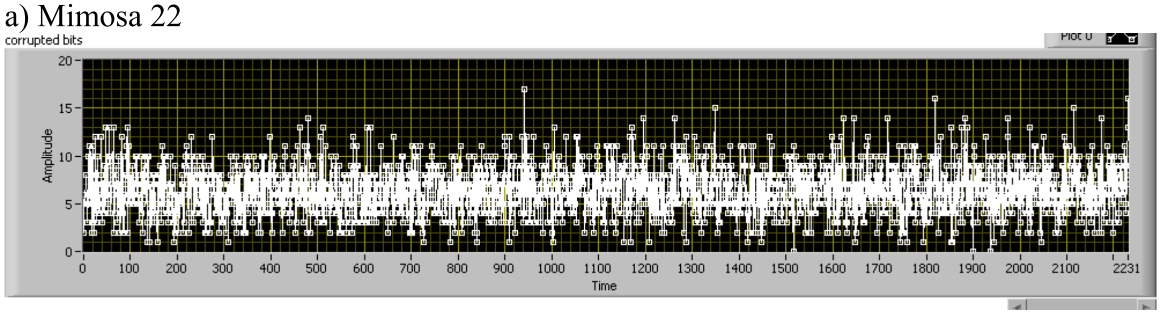
The obtained results indicate that there is no difference within error bars in error rates, whether the sequence contains more 0s or 1s for the given beam type. This means that both corruptions, 1 to 0 and 0 to 1, are equally likely for the same beam type.

However, the measurements indicate that there is a dependency of the corruption type on the LET of the ions in the test beam. It is clear from Figure 8 and Figure 9 that as the LET increases the ratio of error rates increases. This indicates that there is a preference for “0 to 1” corruptions at higher LET values. At this time, it is only an observation without any known consequences for the sensor development or operation.

Figure 10 shows the number of corruptions in each bit in the programming sequence of Mimosa22 and Phase-1 obtained during the whole test (for more details see Appendix A – glitch in JTAG sequence). The plots indicate that the distribution is random and uniform.



a) Mimosa 22



b) Phase-1

Figure 10 Number of corruptions in each bit throughout the whole test for Mimosa22 (a) and Pahse-1 (b). Number of bits for each chip corresponds to a complete programming sequence of all in-chip control registers i.e. 560 bit for Mimosa 22 and 2232 bits for Phase-1.

Poisson distribution fits to the data presented in Figure 10 are shown in Figure 11. It is clearly visible that the distribution of registered errors closely represents counting statistics for both sensors.

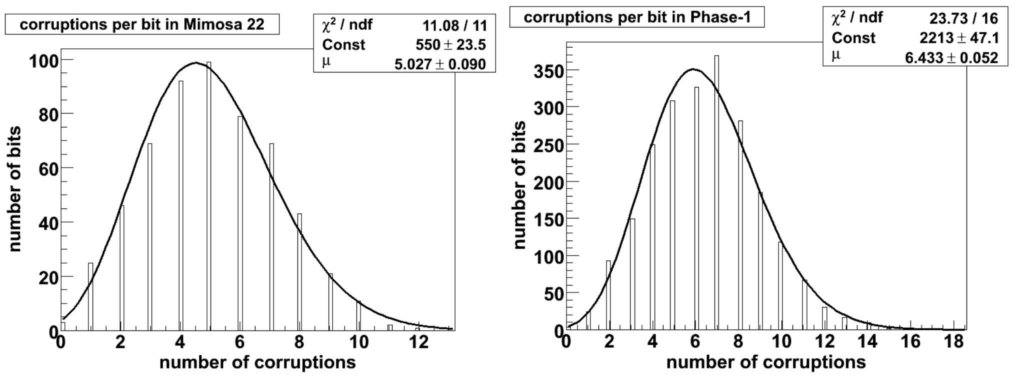


Figure 11 Distribution of corruptions per bit in Mimosa22 and Phase-1 prototypes. The histograms represent data shown in Figure 10. Poisson distribution fit shows good agreement with data.

Observations and comments

All 3 prototypes are more susceptible to latch up than MimoSTAR2. SUZE is more susceptible to latch up by a factor of ~5. In general, we are not expecting to see these levels of LET during normal running conditions at STAR. Possible exceptions would be unusual events such as beam dumps and during beam injection. The possible values for particle densities for these unusual conditions are being studied.
Phase-1 was tested in three configurations to check if the latch up rate depends on the sensor operating conditions. The amount of collected data was small and doesn't definitively answer the question. It appears though, that in all three cases (sensor powered but not running, sensor powered and programmed but not running, and sensor fully operational) the measured cross sections are the same within error bars. This indicates that a sensor that is being tested for latch up doesn't necessarily have to be fully operational.
Soft error analysis revealed that the onset of these types of upsets is very close to the onset of latch up events.

During the test of the Phase-1 prototype with a Cl and Ni beams, we observed a couple of latch up events that the system could not properly recover from. The system went into oscillations between resetting and reporting a latch up. The effect stayed even after the exposure to the beam ended. The system could be restarted after disconnecting manually both analog and digital power supplies. With the Ni beam, the effect was also visible through an increase in the current consumption, and the continuous latch up reporting was only removed after increasing the latch up detection threshold to 350 mA.
It is not clear if this resulted in a damage to the sensor, but it has been verified that the chip was permanently damaged either during (more likely) or around the test time. More details are available in Appendix B – damaged Phase-1 sensor.

Appendix A – glitch in JTAG sequence

During the test we noticed a certain number of events that resulted in a large number of corrupted bits in a JTAG sequence read back. These types of events were observed throughout the test even in runs with low LET ions and appeared to happen randomly.
An example of such an event is shown in Figure 12 in the programming sequence 29.

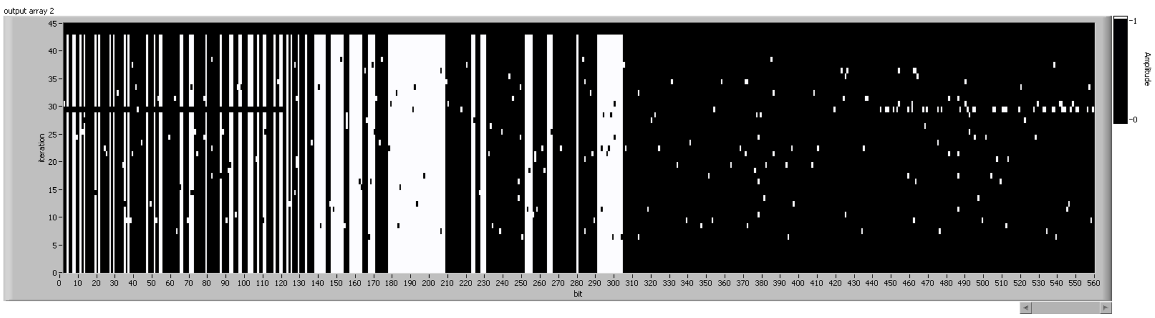


Figure 12 Example of a set of 43 programming sequences (in rows) for Mimosa-22 during a run with a Cl35 ion beam. White and black areas represent bits set to 1 and 0, respectively. The sensor was exposed to the beam in time between sequences 6 and 38. Randomly scattered errors are clearly visible. Programming sequence 29 returned multiple and non-randomly distributed errors.

These corrupted sequences occurred at the rate of 2.2% of all sequences for Phase-1 and 3.5% of all sequences for Mimosa22. At the same time, they accounted for 56% and 35% of the total number of bit corruptions in Phase-1 and Mimosa22, respectively. The corrupted sequences had to be removed from data analysis to avoid biasing the result.

After the test, it was confirmed that the JTAG programmer implemented in the Virtex5 FPGA occasionally corrupted the outgoing bit sequence at the rate of a few percent. The bug was removed by making small modifications in the VHDL code of the JTAG programmer.

Appendix B – damaged Phase-1 sensor

After latch up tests chip D2 seems to be broken:

Measured IKIMO VREF2 and VREF1 :
IKIMO – within 2 mV of the previous measurement from before the latch up test
VREF2 has an increasing discrepancy from ~4mV (@30DAC) up to 18mV (@210 DAC)
VREF1- @ 60 VREF2 => 8mV DC offset
VREF1- @ 80 VREF2 => 10mV DC offset
VREF1- @ 100 VREF2 => 12mV DC offset
But in all cases the crossing point (VREF2=VREF1) is at the same value => 110 DAC

For reasonable settings and digital readout

- No response to light
- No response to discriminator test pattern
- Fixed pattern at the digital outputs
- No response to modifications of the control pattern (read, calib, reset) except for the Latch signal (when disabled there is no more pattern at the output pins
- Disable all discriminators – no effect
- **No digital marker for synchronizing the readout system**

Power consumption when

	fully operational	140 mA (dig)	99 mA (ana)

other chips:

E4,D1	= >fully operational	110 mA (dig)	97 mA (ana)
F4	= >fully operational	100 mA (dig)	96 mA (ana)

Analog output signal seems to be OK.
But when the scan pixel mode is disabled, it behaves as if it had a problem with synchronization (when there is enough light to see pixel signal levels vary).