Description and Results of latch up tests May 24, 25 2006

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The goal

Test the vulnerability of the MimoStar2 chip to latch up failures.
(Observe the latch up cross section for the analog and digital parts of the chip separately.)

Place

The Single Event Upset Test Facility at BNL's Tandem Van de Graaff Accelerator Facility (http://tvdg10.phy.bnl.gov/) provides the user with a flexible and user friendly system for investigating single upset failures (see Figure 1). The detailed system description that is available on the web site allows preparing tests in advance and to efficiently spend the beam time focusing on necessary tests. The user of the system has a lot of freedom in conducting the tests and is also quite independent from the local operators. The beam can easily be switched on/off and the exposure time of the DUT can be easily set. The only necessary interaction with the facility staff is when the ion species or the beam flux needs to be changed. After each exposure time, the number of upsets registered by the user's test bench is typed into the setup control software. The software returns all important information in the form of a table (see Table 1). After the tests we can say that it was a good choice.

Figure 1 SEUTF at BNL. The MimoStar2 test setup is visible in the front. Visible in the back is vacuum chamber open to allow fixing the device under test.

Table 1 Example of the run results from the SEUTF at TVDG BNL

SEU Test Facility

Run #	Date/Time	DeviceID	Ion	Energy MeV	Range um	LET(Si) MeV.cm2/mg	Tilt deg	Roll deg	Time sec	Flux #/cm2/sec	Fluence #/cm2	Dose RAD(Si)	TotalDose RAD(Si)	Upsets	CrossSec cm2	Left %	Top %	Bottom %	Right %	Align %	Center %
3	24May06 09:29	MIMOSTAR2_1	Si-28	186	76.3	7.878	0.0	0.0	100.1	1.561E+04	1.563E+06	1.981E+02	2.355E+02	0	0.000E+00	-3.3	+1.9	+6.6	-5.1	93.3	A
4	24May06 09:40	MIMOSTAR2_1	Si-28	186	76.3	7.878	0.0	0.0	300.1	1.547E+04	4.641E+06	5.883E+02	8.238E+02	0	0.000E+00	-3.9	+2.1	+6.9	-5.0	93.0	A
0	24May06 09:56	Flux	Ni-58	265	42.2	26.58	0.0	0.0	10.2	1.594E+04	1.623E+05	0.000E+00	0.000E+00	0	0.000E+00	-9.8	+6.2	+8.1	-4.6	89.3	+11.5
5	24May06 09:58	MIMOSTAR2_1	Ni-58	200.6	32.14	28.41	0.0	0.0	37.0	1.609E+04	5.956E+05	2.517E+02	1.076E+03	1	1.679E-06	-9.8	+6.0	+8.3	-4.6	89.3	C
6	24May06 10:04	MIMOSTAR2_1	Ni-58	200.6	32.14	28.41	0.0	0.0	10.1	1.643E+04	1.660E+05	7.590E+01	1.151E+03	1	6.023E-06	-10.4	+4.3	+11.0	-4.9	88.5	C
7	24May06 10:04	MIMOSTAR2_1	Ni-58	200.6	32.14	28.41	0.0	0.0	10.1	1.681E+04	1.700E+05	7.772E+01	1.229E+03	10	5.882E-05	-9.1	+5.0	+9.8	-5.7	89.0	C
8	24May06 10:08	MIMOSTAR2_1	Ni-58	200.6	32.14	28.41	0.0	0.0	10.1	1.694E+04	1.710E+05	7.817E+01	1.307E+03	10	5.848E-05	-8.8	+4.5	+10.3	-5.9	89.0	C
9	24May06 10:09	MIMOSTAR2_1	Ni-58	200.6	32.14	28.41	0.0	0.0	10.1	1.657E+04	1.674E+05	7.650E+01	1.384E+03	10	5.975E-05	-7.4	+3.0	+11.3	-6.9	89.1	C
10	24May06 10:11	MIMOSTAR2_1	Ni-58	200.6	32.14	28.41	0.0	0.0	10.1	1.690E+04	1.709E+05	7.812E+01	1.462E+03	10	5.851E-05	-8.0	+4.8	+9.1	-5.8	89.7	C

Test setup

Detection of a latch up condition was based on the fact that the current consumption of the chip should increase significantly during a latch up. The power supplies for the chip were set with a relatively low over current protection. Increase of the current consumption resulted in a decrease of the voltage on the power line for chip current demands over the current threshold setting. Detection of this decrease was considered as a latch up event. In response to the latch up event, the software developed in the LabView environment disconnected power supplies from the chip. For this purpose fast solid state relays were used. After powering down the chip, the LV software restored the power supplies to the chip and initiated the MimoStar2 operation. Two cases were foreseen:

1) Detecting latch up failures in the digital part only – the operation of the chip was initiated by sending the RSTB signal generated from the USB-6800 DAQ. The CLK (differential and single-ended) and SYNC signals were constantly delivered by the USB2 Imager Card. This assured proper operation of the digital part of the chip.
2) Detecting latch up failures in the analog and digital part – the operation of the chip was restored reprogramming full JTAG sequence. It was possible thanks to a trigger feature of the JTAG software version developed at IRES for beam tests. JTAG programming was initiated by a TTL signal from the USB-6800 DAQ sent to the parallel port of the controlling PC. This procedure assured proper operation of both the analog and digital parts of the chip.

The device under tests was MimoStar2 placed on the Mimostar_PCB2 card by IRES. The card was placed inside a vacuum tank. The chip was exposed to a uniform beam of ions with a defined flux, energy and exposure time.
The architecture of the test system is schematically presented in Figure 2. Detailed description of all connections and modifications to the daughter card is presented in Figure 3.

(Detailed documentation for the setup can be found at http://www.lbnl.leog.org/latchup/index.html)

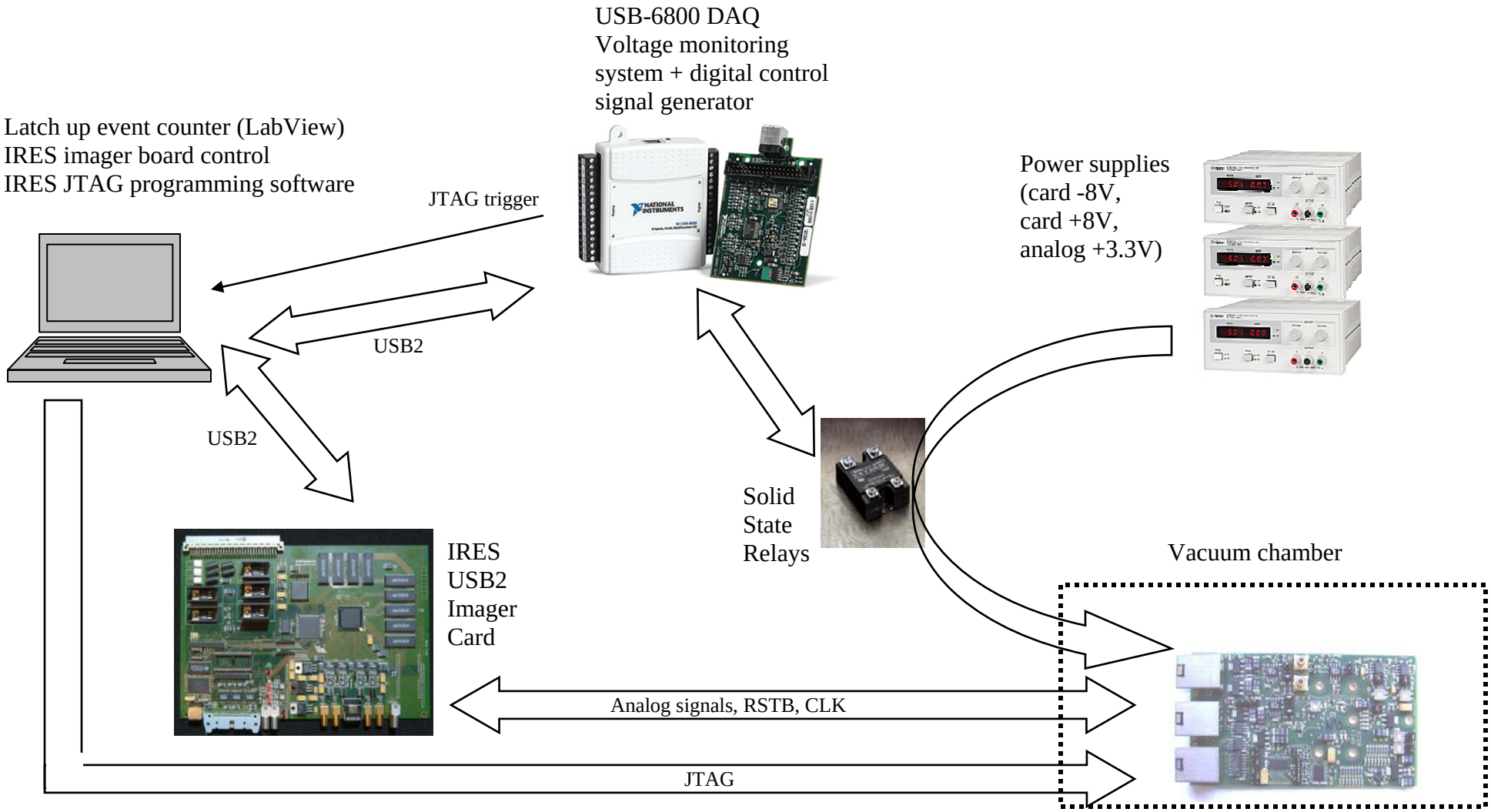

Figure 2 The architecture of the test setup

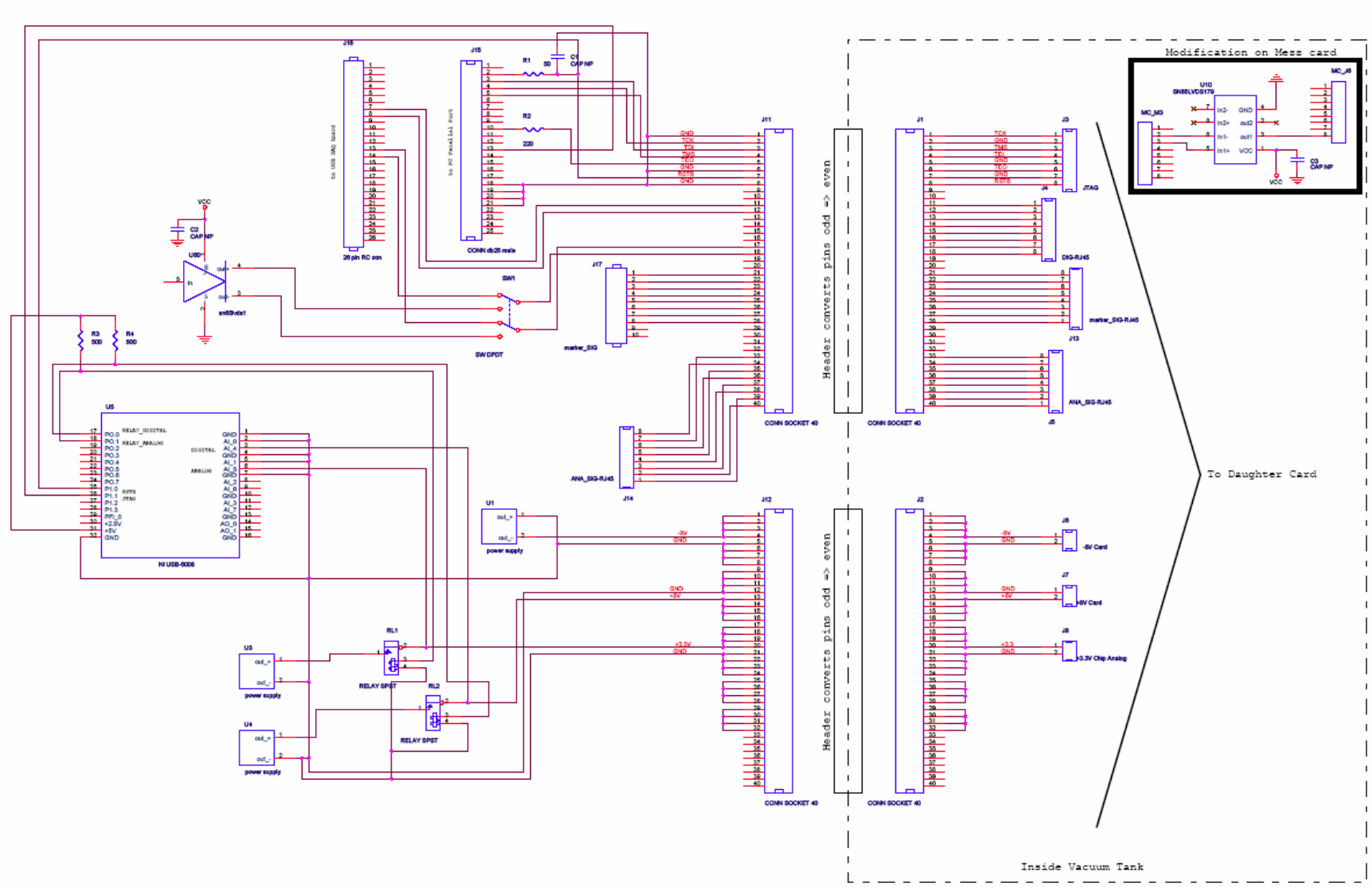

Figure 3 Detailed schematic of all hardware connections and the daughter card modification

Testing Procedure

1) We started with LET 7.8 MeV.cm2/mg (Si-28) and observed no events.
2) In the next step we used LET 28.41 MeV.cm2/mg (Ni-58) and started to observe some latch up events. Unfortunately we had to spend some time debugging the setup and the implemented procedures.
3) We made a sweep of LET going through ~28, ~56, ~38, ~64, ~12 MeV.cm2/mg (Ni-58, I-127, Br-81, Au-197, Cl-35)
4) During tests with Cl-35 we started observing some strange behavior on our digital marker signals and on the analog signal monitoring screen (see the next section)
5) Next day we continued tests with Cl-35 and tried to count number of upsets observed that were not recognized as latch up.
6) Going down with LET to ~3, ~5, ~8 MeV.cm2/mg (0-16, F-19, Si-28) resulted in NO upsets observed

As a result of 4), a study of upsets was based on observations of the:

1) digital marker from the chip (first pixel)
    a. time shifts in the pattern are referred to as “glitches”
    b. frequency changes in the marker length are referred to as “states”
2) analog signal displayed on the PC by the data acquisitions software with the monitoring feature
    a. patterns observed on the signal are referred to as “analog”

REMARK: Although results with “glitches” are presented in Figure 5 it is difficult to say how reliable they are. Certain number of glitches was also observed without any beam (5 in 2 min). With the beam of Cl-35 75 glitches were found in the same time period.

Test results are summarized in Figure 4 and Figure 5 where cross sections are presented in function of LET (upper plots) and in function of corresponding MIP number (bottom plots). For converting from LET to number of MIPs an assumption of ~1.6 MeV.cm2/mg per 1000 MIPs was made.

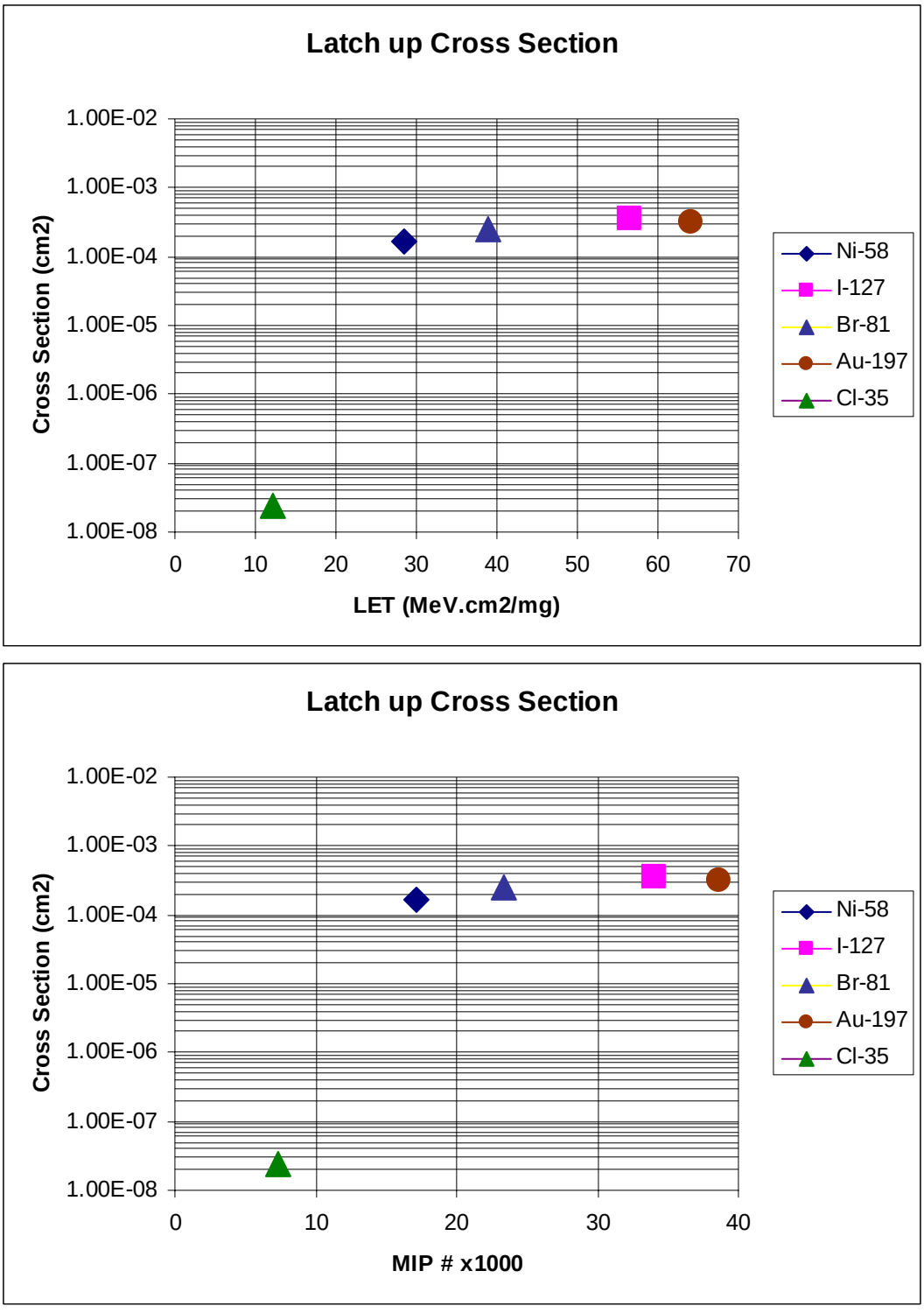

Figure 4 Latch up cross sections measured in function of LET (upper plot) and corresponding number of MIPs (lower plot)

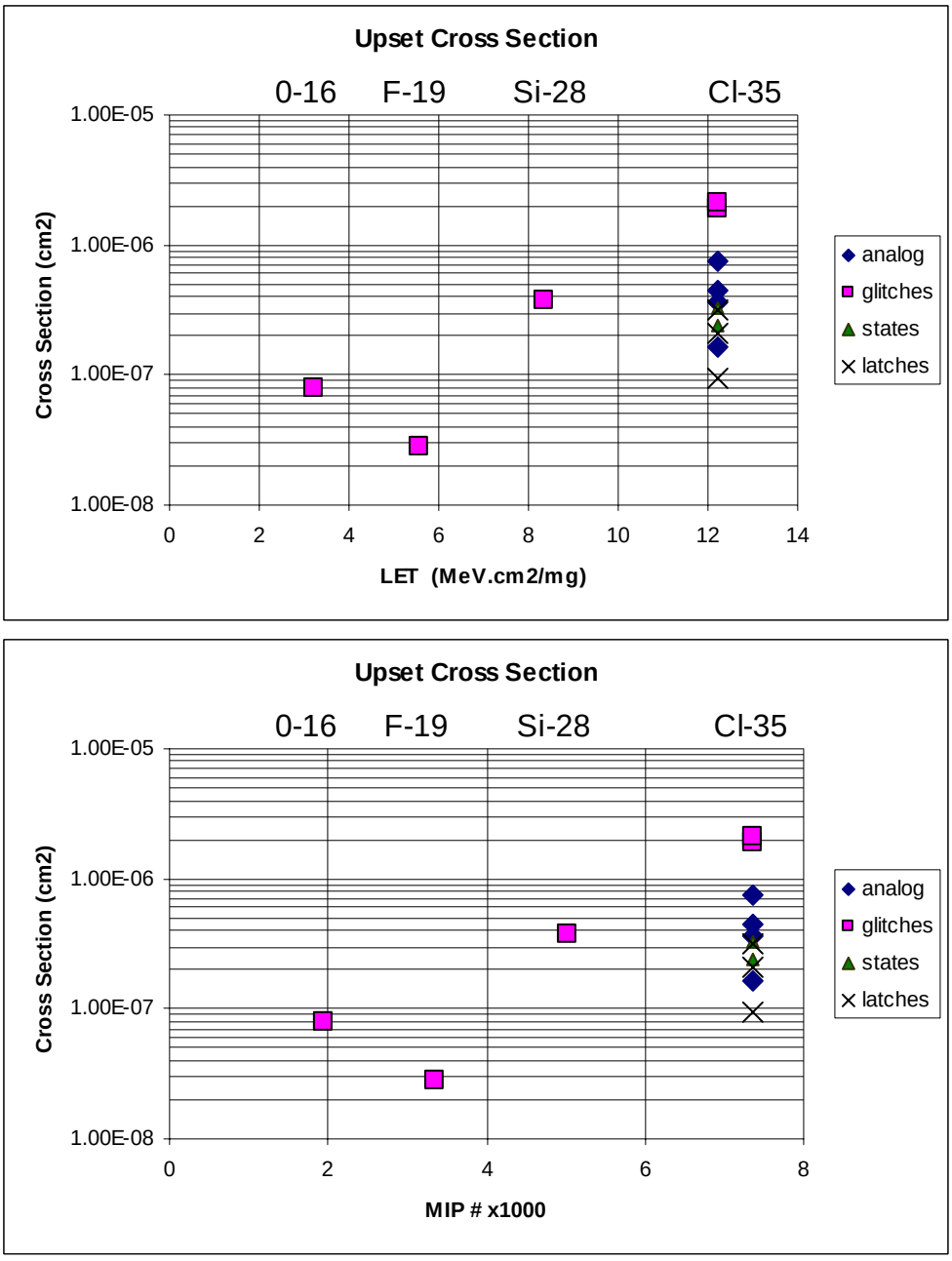

Figure 5 Non-latch up upset cross sections measured in function of LET (upper plot) and corresponding number of MIPs (lower plot)

Running the Test

The latch up detection and recovery procedure was planned to be performed in 3 steps:

1) Detection of the voltage drop on the power supply line resulting in disconnecting power supplies from the chip
2) Waiting for the supply voltage of the chip to drop below a user defined level (~0V). Satisfying this condition resulted in reconnecting power supplies.
3) Waiting for the voltage level to reach operational value (close to the default value for all power supplies separately).

With frequent events the software tended to go into an infinite loop when during recovery time another event occurred between step 2 and 3. Therefore, the 3rd step had to be removed.

In the later tests some upsets resulting in relatively low current consumption increase were observed. For example, observing the power supplies indications, we saw that 2 or 3 gradual increases of the current were needed before the software was capable of detecting a latch up. Unfortunately there was no possibility to measure these events in an automatic way for the following reason. The power supply for the card (+8 V) and the digital power supply for the chip (+3.3 V) were not separated[1]. Therefore, the power consumption of the digital line was added to the consumption of the PCB card. Large differences (few tens of mV) between the after-power-on state and the operating state (after sending RSTB and SYNC) prevented from setting the over current protection at a very low level (DC + ~10 mV).
Such tries resulted in oscillations between false latch ups and operating conditions.

Conclusions

We experienced some problems running our system in the real environment and we spend few hours debugging and adopting all procedures. Even though, we managed to fit into time schedule of 12 hours divided 8+4 in two days. We have managed to obtain all the results that had been planned. We even measured more than we had foreseen as not only latch up events but also other upsets were observed and investigated. For studying other than latch up events we were not prepared. In the future, another approach based on reading back the JTAG settings should be applied.

The latch up cross section measured in our tests is between (2×10^{-8}) 9×10^{-8} and 2×10^{-7}cm2 for LET ~12 MeV.cm2/mg.
We also observed SEU with a cross section of about 2×10^{-7} to 7×10^{-7} cm2 for the same LET. There is some slight indication that SEU might exist for lower LETs but basing on our results such a conclusion not be considered as reliable.

[1] See “Mimostar 2 - Oddities during testing” for more details