CMOS Sensors for EUDET Telescope: Progress Report

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on behalf of DAPNIA-Saclay & IPHC-Strasbourg

OUTLINE

- General remarks
- Analog output sensors (short term)
- Progress report on digital output sensors
- Milestones until final design $\longrightarrow$ fabrication plans until 2009
- Summary

Development Strategy

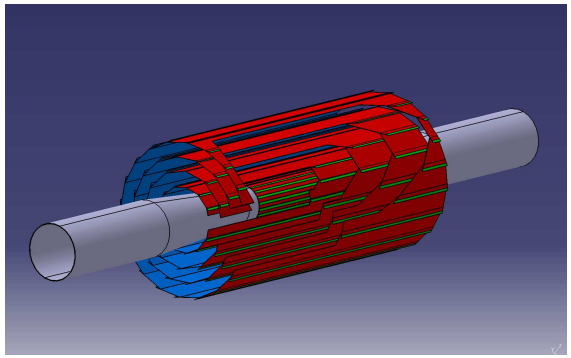
- 2 consecutive steps corresponding to increasingly demanding requirements:
  - analog output sensors (1 for arms, 1 for DUT) $\rightarrowtail$ 1 kf/s
  - digital output sensors (for the arms) with integrated $\emptyset$ $\rightarrowtail$ $\gtrsim$ 10 kf/s

- exploit synergy of requirements and schedules of other applications $\rightarrowtail$ increased resources
  - STAR Heavy Flavour Tagger (HFT)
    - demonstrator (2008): analog output, similar constraints as EUDET demonstrator
    - final sensors (2010): similar architecture and requirements as EUDET
  - CBM Micro-Vertex Detector (MVD)
    - demonstrator (2007/08): analog output, uses EUDET demonstrator chip
    - final sensors ($\gtrsim$ 2010): much faster and rad.tol. than for EUDET
  - ILC vertex detector $\rightarrowtail$ probe ladder (2010)
    - outer layer sensors: $\sim$ EUDET final sensor but diff. pitch and integ. ADC
    - inner layer sensors: like outer layer sensors but $\sim$ 50 % faster clock frequency
  - Imaging applications

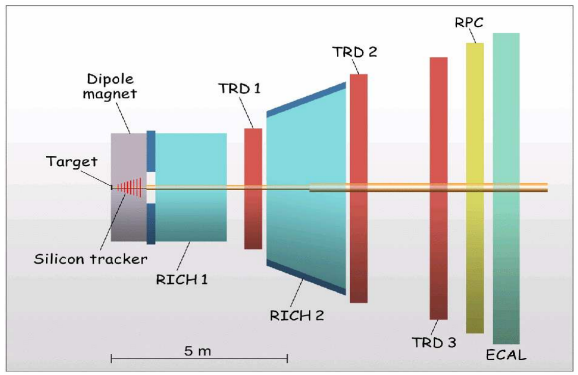
Vertexing Applications of MIMOSA Sensors

- **Vertex Detector upgrade for STAR expt at RHIC**
  - ≙ 2 cylindral layers : $\sim$ 2000/3000 cm^2
  - ≙ $\sim$ 500 millions pixels ($\leq$ 30 μm pitch)
  - ≙ 2 steps : 2008 (analog outputs) & 2011 (digital outputs)

- **ILC vertex detector (option)**
  - ≙ 5–6 cylindrical layers : $\gtrsim$ 3000 cm^2
  - ≙ 300-500 milion pixels (20–40 μm pitch)
  - ≙ 1st complete ladder prototype $\sim$ 2010



- **CBM vertex detector (FAIR/GSI)**
  - ≙ 3 rectangular layers : $\sim$ 2000 cm^2
  - ≙ 200–300 milion pixels ($\sim$ 20–30 μm pitch)



List of Tasks Entering the Realisation of Sensors

- **Sensor design and simulation of sensing and micro-circuits (chip designers, physicists)**

  ⟶ **requires typically 6 months**

- **Fab. of sensors: small proto. in multiproject run or large sensor in engineering run (industry)**

  ⟶ **requires typically 2–3 months**

- **Steering, read-out and DAQ boards:**

  ⟶ **design (lab engineers), PCB fab. (industry) & assembly (lab techniciens) & tests (lab engineers, phys.)**

  ⟶ **needs typically 3–6 months (not counting DAQ firmware)**

- **Characterising chips (and eventually wafers) in lab (^{55}Fe) and with beam (DESY, CERN)**

  ⟶ **needs typically 3–6 months**

- **Thinning in industry**

EUDET funding addresses only (part of) the sensor fabrication

(all the rest - foundry & boards, etc. - is payed by IN2P3, DAPNIA, CBM, STAR, etc.)

AMS 0.35 OPTO engineering run (fabricated in Summer 2006):

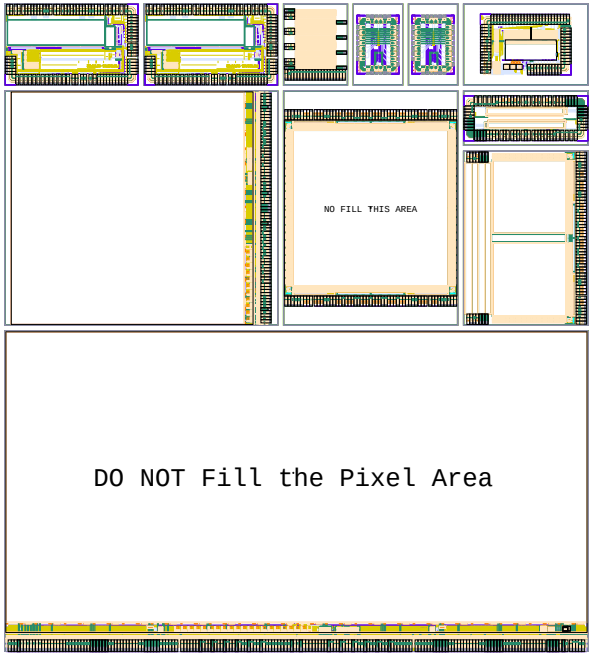
≙ 2 + 4 wafers (8" ⇒ 50 reticles/wafer) ⇔ 2 epitaxy thicknesses : $\sim$ 11 & 15 μm ⇔ "14 μm" & "20 μm" options

◇ triggered by MIMO★-3 (= MIMOSA-20) fabrication :

200 kpixels, $\sim$ 2 cm^2, 2 // outputs, t$_{r.o.}$ $\lesssim$ 4 ms

◇ includes 8 other chips :

- ✳ MIMOSA-16 : fast col. // archi. like MIMOSA-8
- ✳ MIMOSA-17 (MIMO★-3M) : 0.8 x 0.8 cm^2, rad.tol., 800 μs
  - ⟶ EUDET beam telescope arms, CBM Vx Det. demonstrator
- ✳ MIMOSA-18 (IMAGER) : precision $\lesssim$ 1 μm (EUDET: DUT)
- ✳ MIMOSA-19 bio-med. imaging: special diode shape
- ✳ test structures : in-pixel amplification, discrimination, ...
- ✳ ADCs: flash from LPCC



< $\sim$ 20 mm >

◇ funding: CBM (1/2), STAR (1/4), EUDET (< 1/10), IN2P3 & DAPNIA (rest)

Status of tests:

◇ 2 wafers tested in 2006 (1 with "14" & 1 with "20" μm epitaxy) ⟼ fab. mistake (non uniform effect on sensors)

⟶ not dramatic: "20 μm" option was characterised with ^{55}Fe source

◇ Second batch fabricated in 2007 ⟼ 2 wafers presently under test

- **New** *working horse*, **superseeding MIMOSA-5 :**

  Faster, much easier to operate, ionising rad. tol., etc.

  ⇛ **equip EUDET telescope & MVD demonstrators**

- **Medium size copy of STAR final sensor prototype :**

  (65 000 pixels instead of 205 000)

  ※ **manufactured in AMS 0.35 μm OPTO techno.**

  with $\gtrsim$ 11 μm and $\sim$ 15 μm epitaxial thickness

  $\longmapsto$ **tests started at IPHC (and DESY)**

  ※ **ionising rad. hard pixel design (validated with MIMOSA-11/-14)**

  ※ **4 matrices of 64 x 256 pixels (30 μm pitch) treated in //**

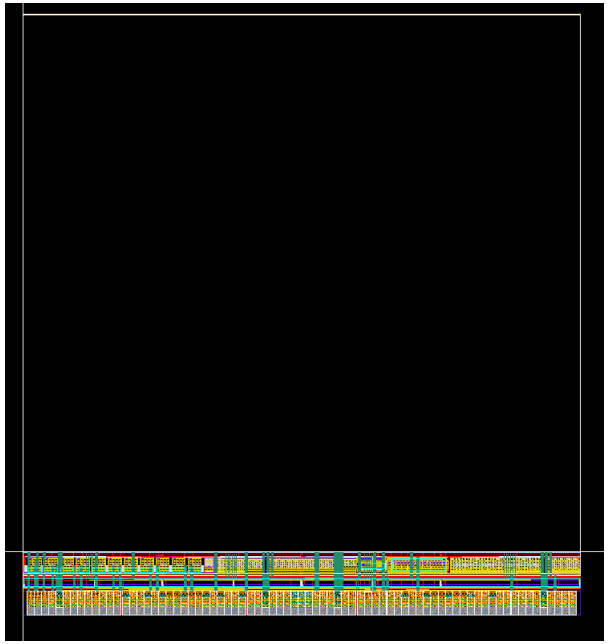
  $\longmapsto$ **active area of $\sim$ 8 x 8 mm^2**

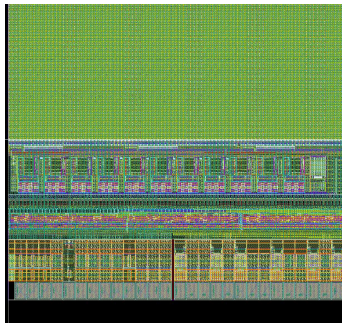
  ※ **4 parallel analog outputs at 10 (or 20) MHz**

  $\longmapsto$ **frame r.o. time = 1.6 ms (or 800 μs)**

  ※ **integrated JTAG logic for steering**

  ※ **works at room temperature**





- **MIMOSA-17 (**& MIMOSA-18**) qualified for 1st demonstrator tests of tele. arms (**& sub-μm resolution**)**

  $\longmapsto$ **commissionning in Summer 2007 at DESY**

Development of Final Sensor

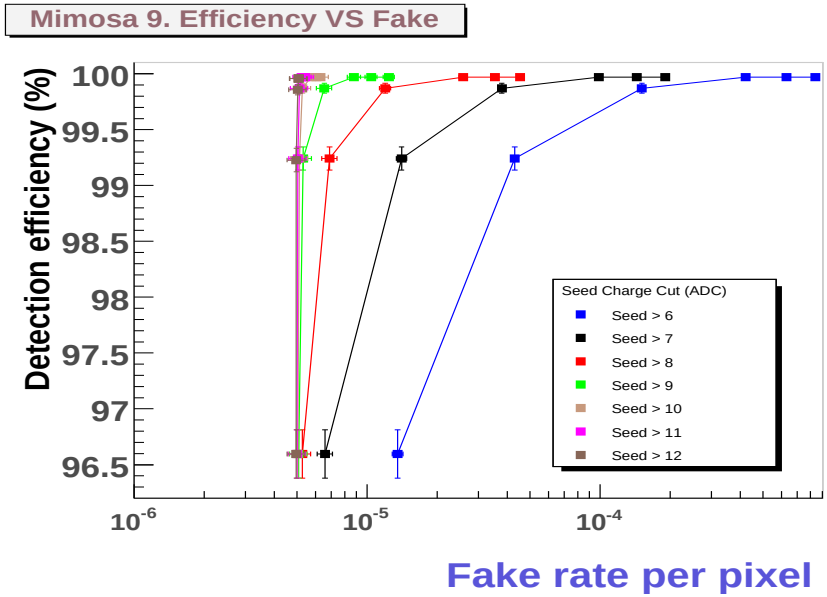
Essential Improvements Provided by Final Sensors

⇛ **Improvements focus on sensors equipping the arms (not DUT surface) :**

- **Increase of read-out speed by one order of magnitude :**
  - Demonstrator provides frame read-out time of 1.6 ms (possibly 800 μs)
  - Final sensors will provide frame read-out time $\sim$ 100 μs (possibly $\gtrsim$ 60 μs)
- **Extension of sensitive area by factor 3.5 :**
  - Demonstrator sensitive area : 7.68 x 7.68 mm^2
  - Final sensor sensitive area : $\sim$ 20. x 10. mm^2
    - $\longmapsto$ encompasses width of ILC-VD sensors
- **Integrate several other improvements resulting from R&D progress**
  - ($\longmapsto$ signal amplification, data compression, output memories, etc.)

Expected Data Rate per Sensor

- **Baseline assumptions :**
  - sensor made of 1024 col. of 512 pixels $\longrightarrow \sim 5{\cdot}10^5$ pixels / frame
  - $t_{r.o.}$ = 100 μs $\longrightarrow$ 10 kfps (can be twice more or twice less)
  - $\lesssim$ 5 hits / frame
  - noisy pixel rate $>$ threshold $\lesssim 10^{-4}$ $\longrightarrow$
  - pixel data size = 2 Bytes
    (10 bits of address & 5 bits for charge)



- **Data rate from pixel noise :**
  - 50 pixels / frame $\longrightarrow$ 1 MB/s

- **Data rate from beam particle hits :**
  - 5 hits of 9 pixels / frame $\longrightarrow$ 1 MB/s

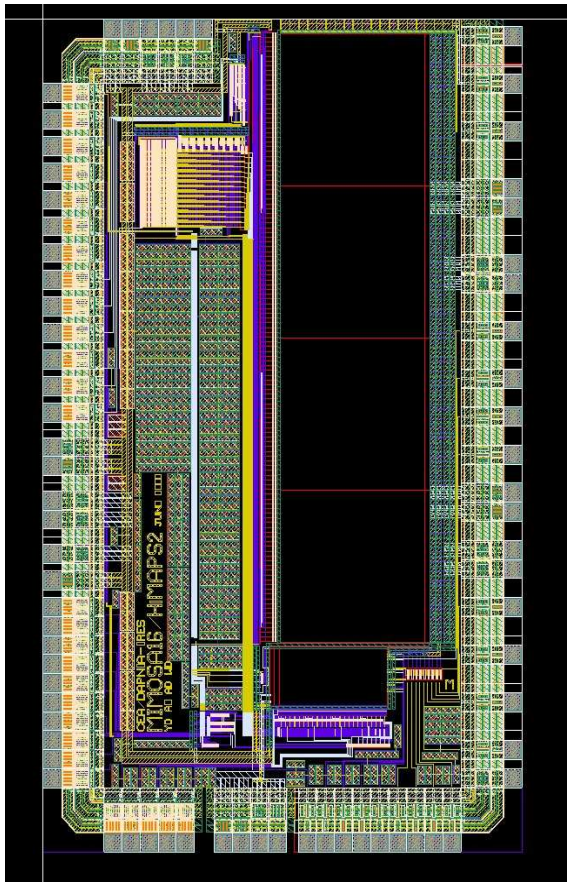
$\Rrightarrow$ **Total $<$ 1 kB/frame $\longrightarrow$ few MB/s only**

Simplified Architecture with Binary Output

- **Geometry :**
  - $\sim$ 1100 columns of $\sim$ 550 pixels
  - $\sim$ 18 μm pitch ($\rightarrowtail$ $\sigma_{sp} \sim$ 5 μm)
    - $\hookrightarrow$ MIMOSA-8 tests at CERN-SPS (Aug. '06) $\rightarrowtail \sigma_{sp} \sim$ 7 – 8 μm (25 μm pitch : 7.2 μm)
  - Sensitive area $\sim$ 20 x 10 mm^2
- **Functionnalities :**
  - pixels with integrated CDS (and DS at end of column)
  - column ended with integrated discriminator $\rightarrowtail$ binary encoding of charge
  - $\emptyset$ micro-circuit integrated downstream of discriminators
- **Read-out speed (adapted to DESY beams):**
  - default $\mathbf{t_{r.o.}} \sim$ 550 lines / 5.5 MHz = 100 μs
  - flexible clock frequency : e.g. 1 – 10 MHz $\rightarrowtail \mathbf{t_{r.o.}} \sim$ 550 – 55 μs

$\Rrightarrow$ **Less development needed to finalise sensor than with integ. ADC $\Rrightarrow$ available earlier**

- **MIMOSA-16 design features :**
  - AMS-0.35 OPTO translation of MIMOSA-8
    $\hookrightarrow \sim$ 11–15 μm epitaxy instead of $<$ 7 μm
  - 32 // columns of 128 pixels (pitch: 25 μm)
  - on-pixel CDS (DS at end of each column)
  - 24 columns ended with discriminator
  - 4 sub-arrays :
    - S1 : like MIMOSA-8 (1.7x1.7 μm^2 diode)
    - S2 : like MIMOSA-8 (2.4x2.4 μm^2 diode)
    - S3 : S2 with ionising radiation tol. pixels
    - S4 : with enhanced in-pixel amplification
      (against noise of read-out chain)



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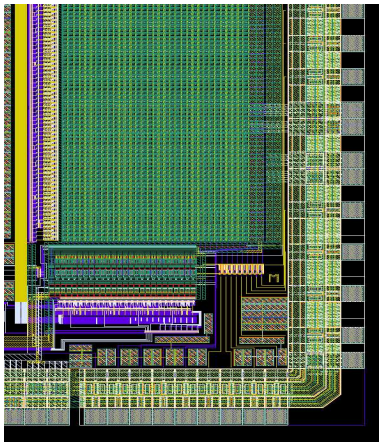
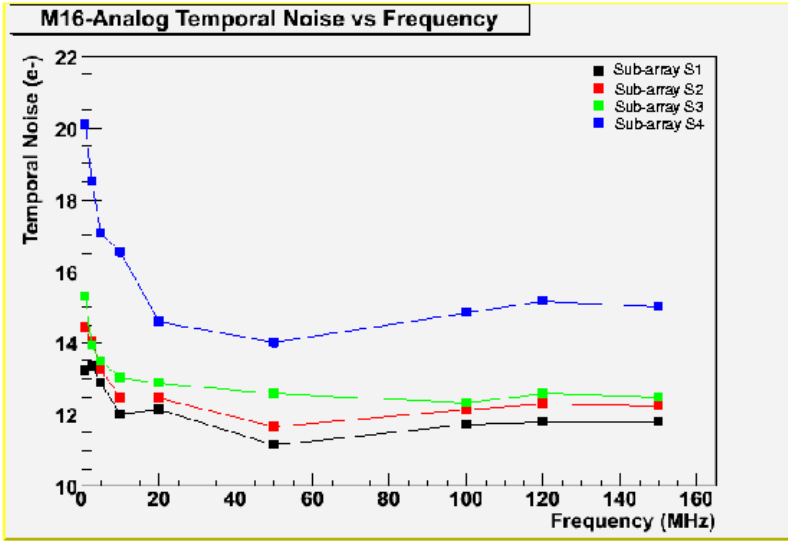


- **Preliminary tests of analog part ("20 μm" epitaxy) performed in Saclay:**
  - sensors illuminated with ^{55}Fe source and F$_{r.o.}$ varied up to $\gtrsim$ 150 MHz
  - measurements of N(pixel), FPN (end of column), pedestal variation, CCE (3x3 pixel clusters) vs F$_{r.o.}$
- **Tests of analog part ("14 μm" epitaxy) started in Saclay** $\longrightarrow$ first results (CCE)
- **Next steps :** digital part $\geq$ June at IPHC beam tests $\gtrsim$ 4 Septembre at CERN (T4 – H6)
- **Later in 2007 :** tests of sensors produced in 2nd batch

Pixel noise and charge collection efficiency for "20 μm option :

Temporal noise vs Frequency
Chip#0 (old mezzanine board)
Columns 28-31



08/01/07 Résumé résultats Mimosa-16 chip#0

Charge Collection Efficiency vs Frequency
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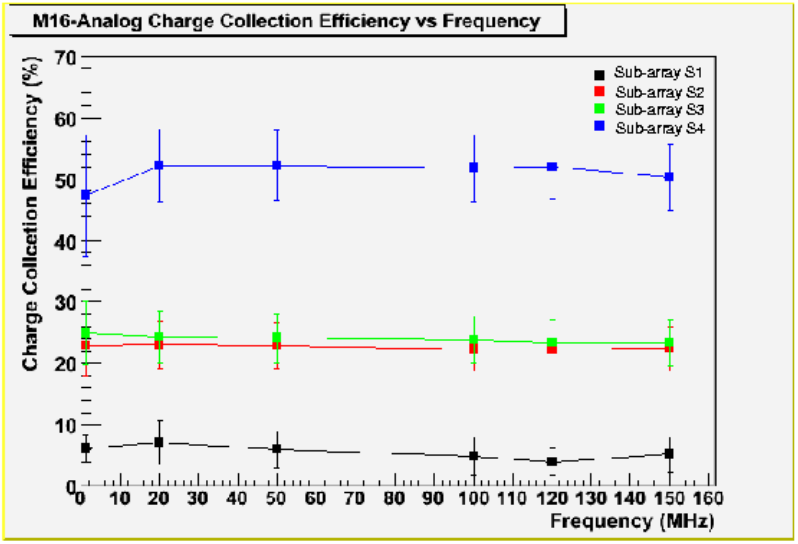
Columns 28-31



08/01/07 Résumé résultats Mimosa-16 chip#0 4

⇛ **Noise performance satisfactory (**like MIMOSA-8 and -15**)**

⇛ **CCE: very poor for S1 (**1.7x1.7 μm^2**) & poor for S2/S3 (**2.4x2.4 μm^2**)**

⟶ **already observed with MIMOSA-15 but more pronounced for "20 μm" option**

↪ suspected origin: diffusion of P-well, reducing N-well/epitaxy contact, supported by CCE of S4 (4.5x4.5 μm^2 diode)

IPHC Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

Réunion Capteurs CMOS, lundi 26 fevrier 2007

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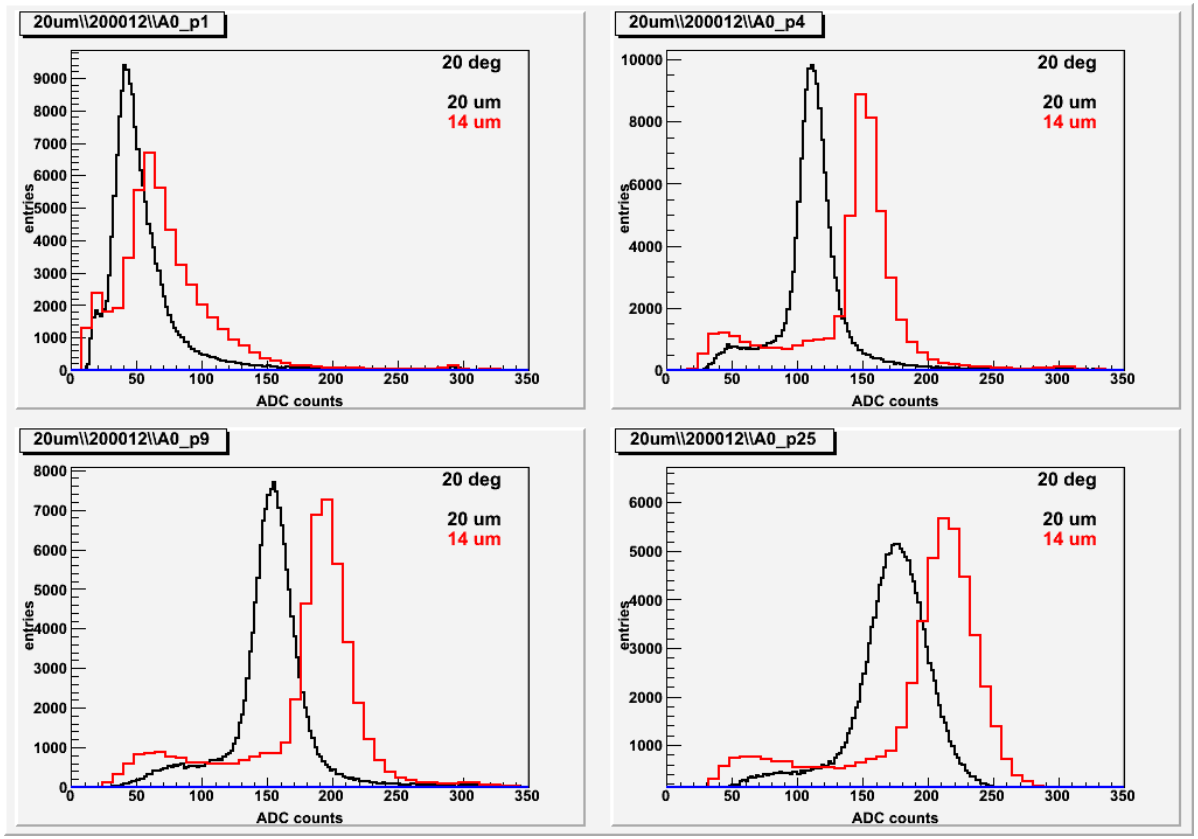
Comparaison pour Mimosa20 entre les deux types de couches épitaxie

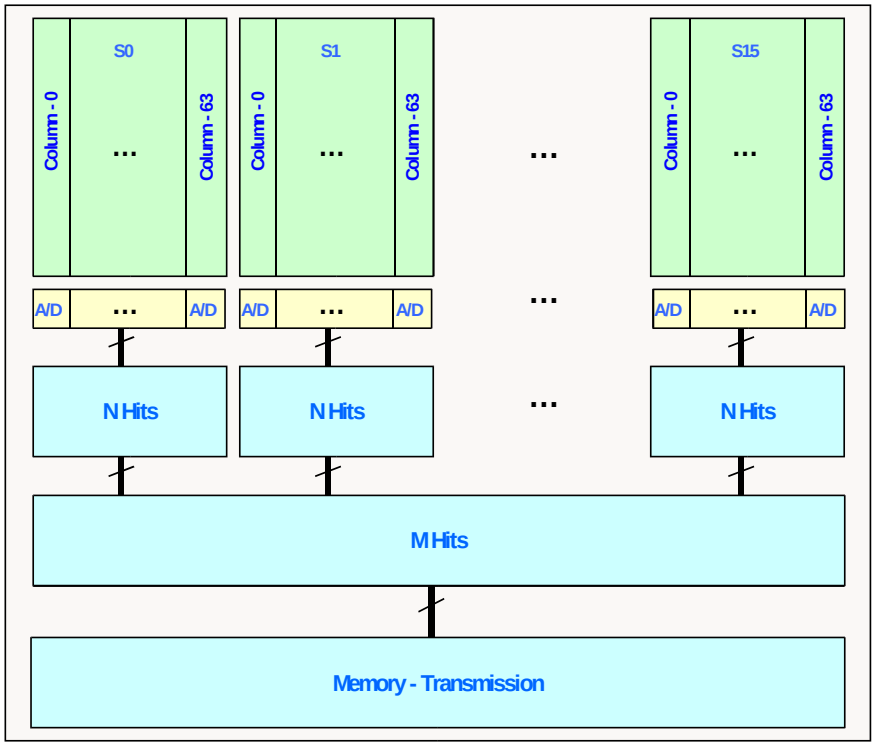


IPHC, 23 rue du Loess BP 28, 67037, Strasbourg Cedex 02, France

- MIMOSA-20 (”14” & ”20” μm epitaxy) illuminated with ^{55}Fe source
  - $\longrightarrow$ charge collected in seed pixel, 2x2, 3x3 and 5x5 clusters
  - $\longrightarrow$ **CCE (”14” μm) $\sim$ 30–40 % higher than CCE (”20” μm)**

Zero Suppression : Block Diagram

Chip readout architecture including digitization and zero suppression



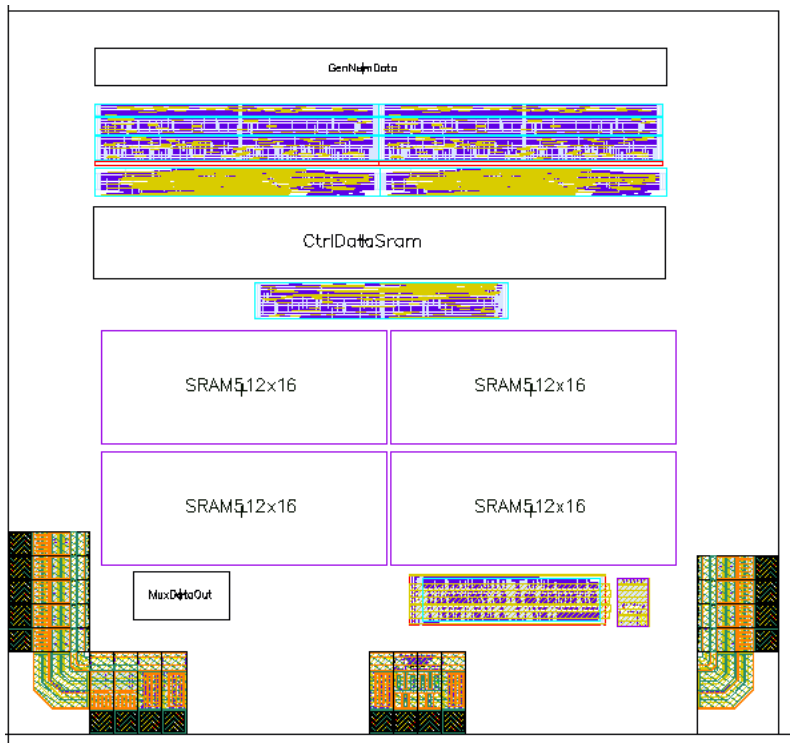
Block diagram of readout architecture

- Pixel array : 1024x1024 pixels Readout row by row The row is divided into 16 groups
- Analog to digital conversion at the bottom of each column (Discriminator or ADC)
- <u>Zero suppression algorithm :</u>
- Find N Hits for each group
  Find M Hits for each row
  (With N and M determined by pixel array occupancy rate)
- Memory wich stores M hits and serial transmission

- Submission of a small size fully digital prototype in AMS 0.35 µm in June 2007

1st chip (SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :

- 2 step, line by line, logic :
  - step-1 (inside blocks of 64 columns) :
    identify up to 6 series of $\leq$ 4 neighbour pixels per line
    delivering signal $>$ discriminator threshold
  - step-2 : read-out outcome of step-1 in all blocks
    and keep up to 9 series of $\leq$ 4 neighbour pixels
- 4 output memories (512x16 bits) taken from AMS I.P. library
- surface $\sim$ 3.6 x 3.6 mm^2 $\longrightarrow$ $\sim$ **8 keuros (EUDET budget)**



Status :

- design under way
- submission scheduled for end of June
  $\hookrightarrow$ back from foundry end of Septembre
- tests completed by end of year

PLANS for 2007–2009

Milestones bridging the gap with the Final Chip

Pixel design :

- adapt existing pixel architectures from 25 μm to $\sim$ 18 μm pitch
- adapt sensing diode dimensions to maximise CCE (surface $\nearrow$) & gain (surface $\searrow$) : optimum $\sim$ 10–15 μm^2
- ▶ find optimal pixel pitch : single point resolution (pitch $\searrow$) against reliable design (pitch $\nearrow$)

Column read-out architecture :

- adapt existing S&H and discriminators from 25 μm to $\sim$ 18 μm pitch
- integrate $\emptyset$ and output memories

Raw and pixel steering (consequences of large surface) :

- adapt pixel steering (speed) inside column to avoid capacitance due to large nb of switches $\longrightarrow$ pixel design
- adapt raw steering to their length (2 cm)

Sensor autonomy and testability :

- JTAG + bias DAC $\longrightarrow$ programmable chip steering
- 2 or 3 additionnal DC voltages to emulate pixel's output for independent discriminator performance assessment

Means needed to deliver final chip commissioned by 2009 :

- human resources for designs ($\gtrsim$ 4 – 5 FTE) and tests ($\gtrsim$ 2 – 3 FTE)
- equipment for designs and tests (presently essentially at IPHC ...)
- funding : $\lesssim$ 100 keuros (devt) & $\gtrsim$ 100 keuros (prod.) $\longrightarrow$ **EUDET : 36 keuros (devt) & 70 keuros (prod)**

♣ **Extension of MIMOSA-16 ⟶ larger surface, smaller pitch, optimised pixel, JTAG, more testability**

Pixel characteristics (still under study) :

- pitch : 18.4 μm (compromise resolution/pixel layout)
- diode surface : $\sim$ 10–15 μm^2 to optimise charge coll. & gain
- 64 columns ended with discriminator
- 4–8 columns with analog output for test purposes
- $\geq$ 6 sub-matrices : $\geq$ 3 pixel designs w/o ionising rad. tol. diode

  ⇛ active digital area : 64 x 384–576 pixels (8.3–12.5 mm^2)

Testability (still under study) :

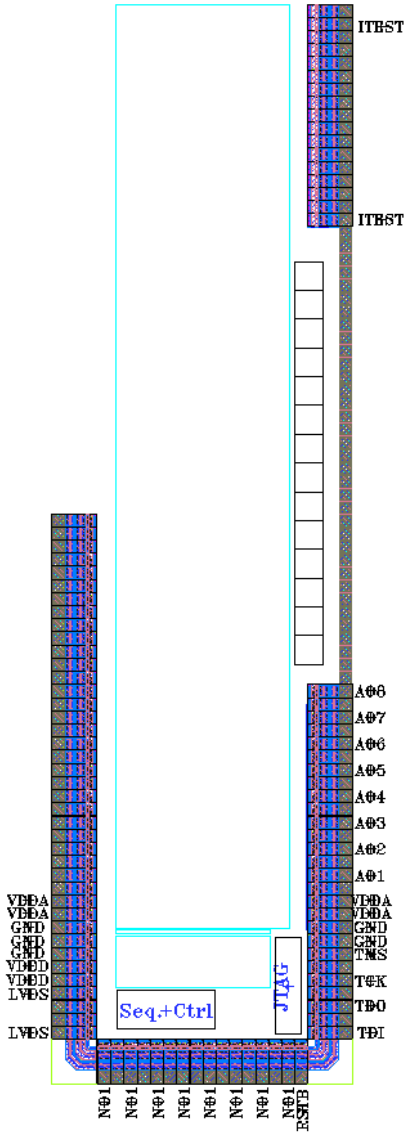
- JTAG + bias DAC ⟶ programmable chip steering
- 2 additionnal DC voltages to emulate pixel's output

  for independent discriminator performance assessment
- output frequency $\leq$ 40 MHz

Status :

- Design under way at IPHC (soon also at DAPNIA ?)

  ↪ submission end of Sept. '07 (?)
- Funding (20–30 keuros) via IPHC ressources for STAR & CBM

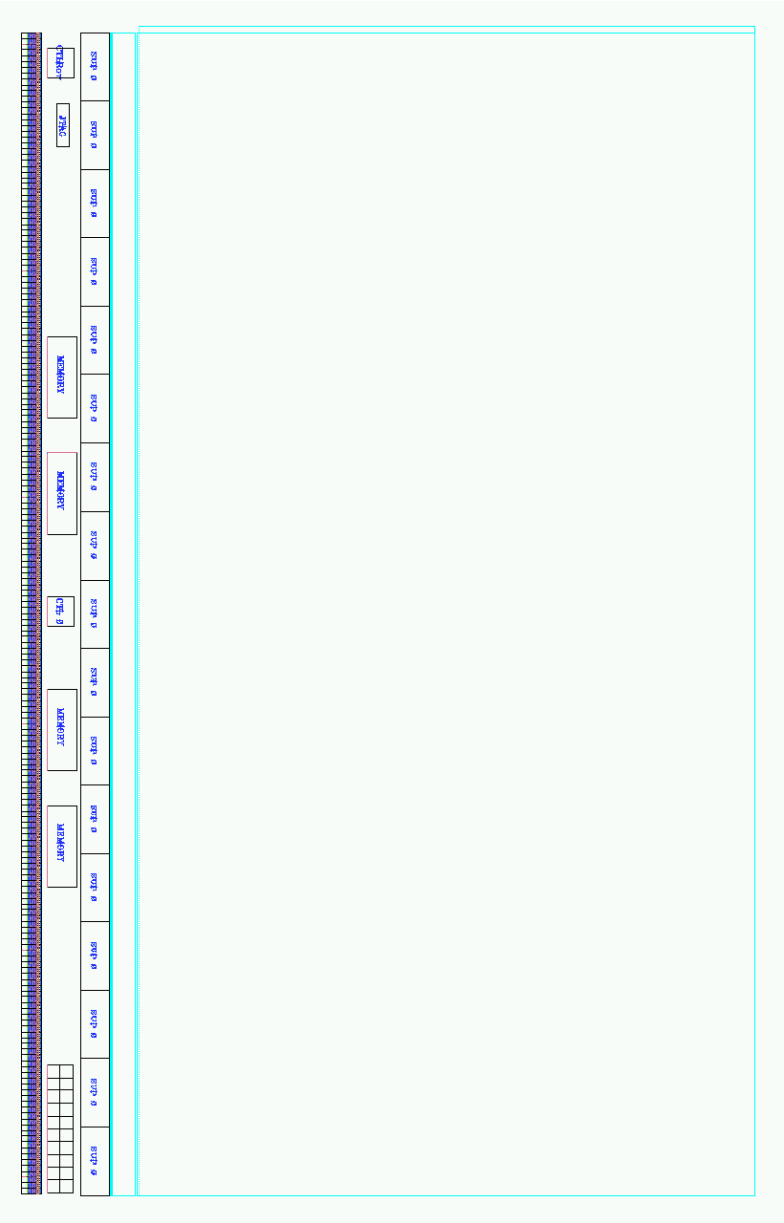


Spring 2008 : MIMOSA-22+ (LP)

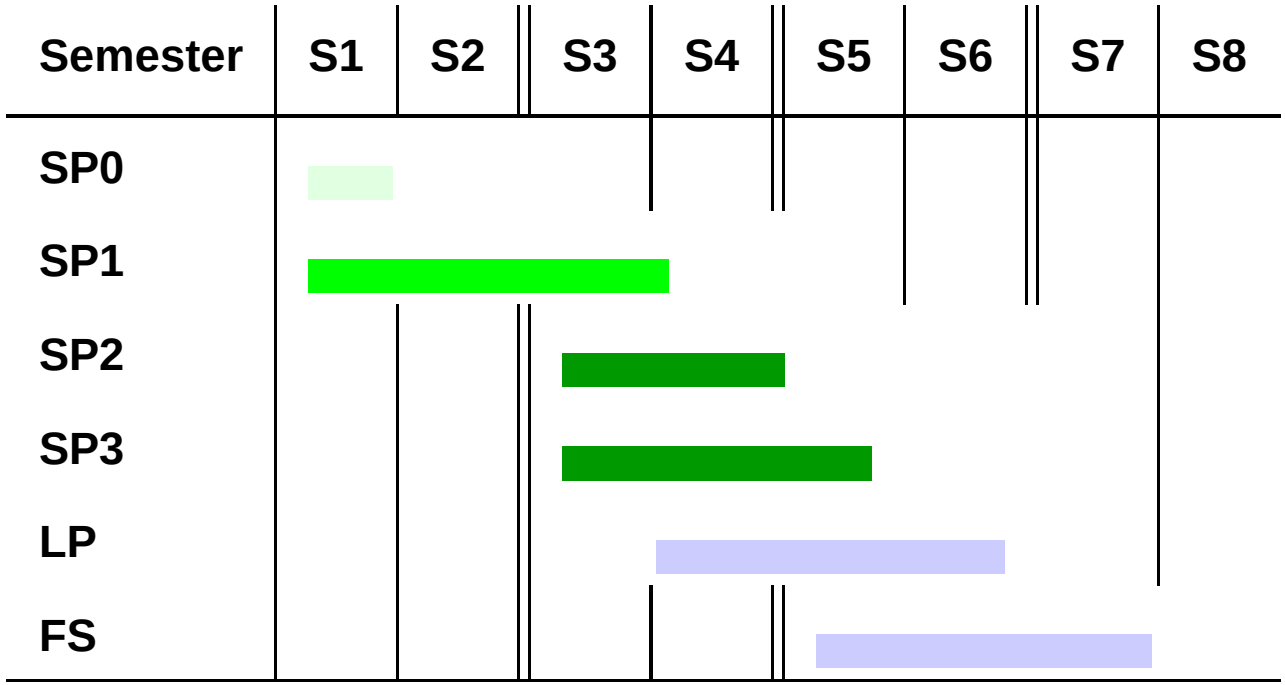
- MIMOSA-22 complemented with $\emptyset$ (SUZE-01)
- 1 or 2 sub-arrays (best pixel architectures of MIMOSA-22)
- larger surface : active surface $\sim$ 0.5 cm^2
  - $\hat{=}$ final column depth (544–576 pixels)
  - $\hat{=}$ $\gtrsim$ 1/4 of final number of columns ($\geq$ 256 / 1088)
- total surface $\lesssim$ 5.5 x 12 mm^2 $\longrightarrow$ 50 – 55 keuros
  - $\hookrightarrow$ available funding : **EUDET (27 keuros)** $\&$ STAR/CBM (rest)
- ▶ opportunity for engineering run (100 keuros) combining various chips

End 2008 / early 2009 : Final chip (FS)

- Extension of MIMOSA-22+
- Active surface : 1088 columns of 544–576 pixels (20 x 10 mm^2)
- Read-out time $\lesssim$ 100 μs
- Chip dimensions : 20 x 12 mm^2
- Engineering run : $\sim$ 120 keuros for 6 diced and thinned wafers
  - $\hookrightarrow$ available funding : **EUDET (70 keuros)** & STAR/CBM (50 keuros)



Tentative Schedule of Sensor Delivery



- **Sensor production based on 5 steps** (perhaps only 4, i.e. SP3 included in LP) :
  - **MIMOSA-8 $\equiv$ SP-0 : 25 μm pitch, epi $<$ 7 μm**
  - **MIMOSA-16 $\equiv$ SP-1 : 25 μm pitch, epi $\sim$ 11 or 15 μm, rad. tol., enhanced ampli.**
  - **SUZE-01 $\equiv$ SP-2 : $\emptyset$ μcircuit with integrated output memories**
  - **MIMOSA-22 $\equiv$ SP-3 : like SP-1 but 18 μm pitch, optimised pixels, 64+8 col. of $\sim$ 500 pixels**
  - **M22+ $\equiv$ LP : like SP-3 but $\geq$ 256 col. of $\sim$ 550 pixels and integ. $\emptyset$**
  - **M22++ $\equiv$ FS : like LP but $\sim$ 1100 col. of $\sim$ 550 pixels**

SUMMARY

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- MIMOSA-16 (SP-1) tests under way :
  - ⋇ analog part (epi-14) : tests started at DAPNIA $\longrightarrow$ CCE (epi-14) $\lesssim$ 3/2 CCE (epi-20)
    - ⋇ digital part (epi-20 & -14) : June at IPHC
      - ⋇ beam tests : $\gtrsim$ 4 Septembre at CERN (T4 - H6)
        - ⋇ 2nd wafer production finished : small doubts about quality $\longrightarrow$ negociations with AMS
- $\emptyset$ suppression micro-circuit (SP-2):
  - ⋇ design under way at IPHC (sets of 64 columns, tolerates close to 10^3 hits/cm^2/frame)
    - ⋇ submission to foundry by end of June
      - ⋇ test completed by end of year $\longrightarrow$ in time for integration in final prototype (MIMOSA-22+)
- Milestones until final chip well identified :
  - ⋇ MIMOSA-22 : pitch, surface, testability, JTAG $\longrightarrow$ subm. end Sept. '07
    - ⋇ MIMOSA-22+ (LP): surface, $\emptyset$ $\longrightarrow$ subm. Spring 2008
      - ⋇ Final Sensor (20x10 mm^2, $\lesssim$ 100 μs) : end 2008 / early 2009
- Resources :
  - ⋇ manpower : design OK – tests (mainly IPHC)
    - ⋇ chip fab. + PCB fab. + thinning $\longrightarrow$ cost $\gtrsim$ 200 keuros (neglecting CAD licences ....):
      106 keuros (EUDET) + $\gtrsim$ 100 keuros (IPHC + CBM/STAR + EUDET coll.)