LG 10/29/2006 **DRAFT**

**Initial Testing of the Infrastructure at BNL for the HFT Telescope Test Run.**

The pole tip is scheduled to be installed on the 27th of November. Before we lose access to the cables that have been placed for the telescope beam test we intend to test the functionality that is required early enough to fix any problems that may be discovered. The anticipated date for the start of our infrastructure tests is November 14th. It is expected that Howard, Xiangming and Chinh will perform the tests at BNL. The tests will include…

Tested features of Telescope:

TCD cable extension
CAT5 cables for control of motherboard via serial, parallel and USB.
Fiber optic cables from platform to DAQ room.
Latch up detection and reset functionality and hardware.
Remote desktop software in the BNL STAR network environment.
Power connection to the MWC power supplies

Hardware needed at BNL for tests:

Control PC
DAQ PC (with RORC)
Laptop PC for in DAQ room remote desktop control
Motherboard
Daughter card
Stratix Board
SIU (DDL)
Motherboard box and mount
Latch-up converter board with cables
Serial to CAT5 converters x 2
Parallel to CAT5 converters x2
USB to CAT5 converters x2
Fiber optic jumpers x2 (motherboard to platform patch panel, DAQ room patch panel to DAQ PC)
Power cable (still needed from Danny P.)

Test plan:

Test all hardware and functionality at LBL first, then ship hardware to BNL.
Install hardware at BNL in the proper places.

Testing:

Power – attach power cable check voltages.

Remote desktop software – verify that one can reach the control PC with remote desktop software. Preferably all of the testing should be done on the control PC via the remote desktop software.

TCD – check that the RHIC strobe, TPC trigger and event ID are correctly received and decoded on the motherboard / daughter card. This should be a longish term test of a large number of triggers and event IDs.

Serial – check the serial connection from the Stratix board to the control PC with Xianging's serial readout software.

Parallel – check that the Altera FPGA on the Stratix board can be configured via the parallel interface.

USB – check that the Xilinx FPGA on the daughtercard can be configured via the USB interface. Also check the USB interface to the Altera FPGA ( two possible configuration paths.)

Latch-up control – short out each of the telescope supply voltages on the motherboard one at a time and check the functionality of the latch-up detection. Reset the voltage using the VI provided by Michal.

SIU – RORC connection – attach the fiber optic jumpers and test the connectivity and data rate of the RORC – SIU connection.

It may be advisable to run several of these tests for an extended period of time. The TCD, Serial, and SIU-RORC connections should be run for at least 24 hours.