STAR HFT PXL Electronics and Sensor Review of June 23,24 2010
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We would like to thank the members of the PXL electronics group for their extremely thorough presentations and especially (together with the mechanical and physics groups) for their efforts in planning, design, and evaluation of the HFT pixel detector.

The Charges:

The scope of the review is the sensor and RDO system for the PXL detector system.

Quoting from the opening presentation:

- Does the proposed design meet the requirements as stated?
- Is the design consistent with good practice and appropriate to the task?
- Does the team possess the knowledge and skills to carry out the project?
- Is the cost and schedule realistic and appropriate?
- Is the documentation adequate to present the design?

Findings:

It is the opinion of the committee that the design of the PXL electronics and readout system meets the requirements as stated in the PXL Sensors Overview presentation.

The design choices made for the subsystems presented appear to conform to good practices and are appropriate to meeting the requirements for the PXL sensor subsystem.

The presentations given and prototypes shown to the reviewers convey the thorough understanding of the challenges presented by the PXL system, and show that the breadth and experience of the team is sufficient to complete the project.

The cost planning and schedule documents appear to be well thought out with no significant omissions. A few technological challenges may cause problems, however the contingency seems adequate. Difficulties achieving success with aluminum polymer flex circuits could impact the schedule, however the copper polymer fall-back seems to be a safe alternative with some impact on the physics capabilities.

It seems clear to the reviewers that the implementers of various PXL detector subsystems have a good grasp of the associated applications/programming interfaces, however we did not see evidence of a library of API and interface documents the designers are expected to build to. We urge the group to formalize the documentation of interfacess. Version control of these documents would also be appropriate.

Subsequent to the closeout of the review, various additional materials that were requested by the reviewers were provided. The materials gave a fuller understanding of the technical capabilities of the project's staff. They also generated additional comments from the reviewers; the favorable opinion of the reviewers is unaltered.

The committee's list of issues of interest or concern (not in any particular order):

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1. Have everyone check their current rev of firmware and software into a version control system in order to establish a baseline.

2. Include in the versioning archive the validation software/firmware/test vectors needed to demonstrate correct functionality of elements of the data acquisition subsystem under development.

3. Use an experiment wide versioning software so that collaborators at other institutions can have access to the code base. E.g. STAR CVS

4. Since the data lines between the Readout Module and the Mass Termination module are all differential, consider providing for the surrounding of all data and power pairs with ferrite chokes in order to improve common mode immunity in the installation on the STAR framework. The need for this feature may not be obvious on the bench, but could be essential in the IR. The ambient magnetic field at the readout module needs to be taken into account, of course.

5. The reviewers concur with your concern over procurement of polymer-aluminum flex circuit assemblies. We recommend that a test plan is developed in advance which will help in assessing/evaluating the robustness of prototypes. The IPC specification document(s) for flex circuit manufacture and testing may provide useful guidance. It may also be prudent to open discussions, and perhaps procure samples from more than one vendor.

6. From page 18 of the PXL System Hardware Architecture presentation, it appears that the (proposed) flex circuit solution will have exposed aluminum on both sides of a polymer substrate (no over-coating or solder mask). The reviewers have concerns about the vulnerability to physical or chemical damage of thin pure-aluminum traces without a protective coating. It is recognized that the adhesive under pixel sensors and the adhesive to the carbon stiffener protect the flex circuits locally. It is perhaps feasible to use a thin conformal coating over the finished assembly.

7. It is recommended that the flex circuits be packaged and transported in individual trays/carriers from the manufacturer and whenever possible before and after assembly of ladders. This kind of handling and packaging of flex circuits is quite common in industry. Manufactures of custom trays should be easy to find.

8. The reviewers recommend measuring the coupling of signals from real-world imbalanced LVDS signals on the data pairs running under the sensor die on the flex circuit. This may best be done by disconnecting from the chip and driving with a dual-channel waveform generator where the imbalance can be imposed in a controlled manner. The goal of this exercise is to determine whether electrostatic shielding might be needed between the pixel chips and the flex circuits in order to control chip-to-chip noise coupling.

9. Depending on the outcome of the previously mentioned coupling test, and of other tests, the floating substrate may need to be reconsidered. In particular the thick high-resistance epi process may require a different plan for the substrate than the standard epi process used to date. A preliminary design for a "via" through the adhesive, or other alternative, to make backside contact should be developed now. Lab tests (including but not limited to the data pair coupling test) and discussions with the IPHC group will settle this issue.

10. The large number of interconnections between the Virtex prototyping board and the (6 layer) carrier card they are mounted on is an area of concern. Environmental factors or aging could adversely affect the integrity of interconnections. Gold migration between contacts, for example, might cause intermittent or open circuits during the life of the project. Adequate plating thickness should be specified for gold-to-gold contacts. There is no control of the plating on the Xilinx board, of course, which may pose an issue therefore. Any other metal-to-metal compatibility issues should be evaluated.

11. Current densities for power conductors in the aluminum flex circuit must be kept well below the threshold for metal migration. Most published data is for on-chip interconnect, but indicates a threshold of order 1MA/m^2. This may be comparable to the flex circuit design values.

12. There appears to be little risk of running out of logic resources in the Virtex development board. Memory resources seem to be adequate as well.

13. The availability or end-of-life status of critical subsystems and components should be watched and appropriate steps taken to insure the success of the project. e.g. the Xilinx development board, or USB interface boards, etc.

14. The use of Windows for the controls computer to be installed in the WAH at STAR is thoroughly discouraged. Anything is ok for lab test systems but the installation should employ a relatively standard linux installation maintained by STAR computing group. It is stated that the pixel electronics and software will be entirely linux compatible so this point should be trivial to address.

15. The reviewers feel that the packaging of the readout module should be fleshed out sooner rather than later. This may have a direct and significant impact on

reliability and serviceability. Space constraints, cooling, mounting considerations, connectors, power distribution, grounding, shielding, and safety approval issues should be identified soon so that they can be dealt with in a timely fashion. The lack of external connectors to interface the readout box to all cables is potentially a concern. Appropriate connectors do exist and should be considered.

16. It may be useful to have a final version PXL DAQ emulator for testing the DAQ and off-line software subsystem especially if there are delivery delays for the final version of the pixel chip. This would probably be implemented only as software, the main point being to write PXL daq files in the exact real format. Problems like byte order and ended-ness can be identified before the real hardware is married up to the STAR DAQ. Perhaps montecarlo data could be passed through the emulator to the DAQ for analysis and verification.

17. The functionality of each Latch-Up protective power supply should be verified in-situ before connecting it to its associated ladder.

18. As is already well recognized by the team, but not fully reflected in the presentations, the signal lines between the mass termination board and the sensors should be kept to an absolute minimum. The marker signal is not needed; certain control signals are not needed (and in fact certain control signals might be absorbed internally as JTAG registers if the IPHC group is willing).

19. All four ladder ports of the prototype readout module should be verified. A test of the readout module driven by four ladder (prototypes) is advisable.

20. Will the fine twisted pairs between the mass termination board and the ladder raise any concerns in regards to safety approval? We do not feel that there is a technical safety issue here but nevertheless it is prudent to seek approval at an early stage so that any modifications imposed by safety approval requirements can be handled in a timely fashion.

21. If presented, an eye-pattern measurement is to include amplitude information, i.e., is to be measured after the cable or other transmission structure but before rebuffering. Although probing presents a challenge, we encourage that the actual eye pattern is investigated so that the amplitude margin is evident. The present measurement should be presented as a jitter histogram, In any case, BER measurements with a margin applied to clock frequency, temperature, supply voltage have demonstrated that the link performance is more than adequate. There should be no problem here; just a comment on methodology.

22. As is well understood, data dependent jitter from imperfect transmission media may be addressed though rebuffering at points along the way (as presented) or may possibly be addressed through a double termination scheme. The potential performance of a design using source termination on the ladder but no active buffers at the cable-ladder interface should be considered. This may simplify the

ladder design, improve reliability, and likely will not increase the system power dissipation. Source termination could even be included in the sensor design if IPHC is willing. (This is typical in commercial LVDS serial ADC's.)

23. Handling of all additional Trigger commands needs to be implemented.

24. A top level “essential model” context diagram needs to be part of the documentation and future presentations.

25. Inspection of the trigger interface between the STAR DAQ (described in the 2008 document) and PXL DAQ prompt the reviewers to suggest examination of compatibility issues because the PXL RDO board doesn’t appear to be compatible with the open-collector opto-isolated “busy” interface described in STAR documentation. It would be better to discover any other compatibility issues before the last turn of the PXL DAQ PC board is procured. E.g. connectors, reversed lines, incorrect levels, incorrect signaling sense, etc.
26. The SIU interface should be verified at 50MHz if it has not already been done.
27. The project seemed to be developed far enough to warrant the assignment of document numbers and title-block in schematics, yet the documentation provided after the meeting did not have them. Drawing numbers and interface document numbers in the STAR archiving system should be assigned sooner rather than later. This issue is intertwined with the document control issue mentioned above.
28. Neither the schematic design nor the kit of fabrication files (Gerbers) contained a fabrication document. The fabrication document typically includes the stack-up, board material, copper thickness, electrical tests, etc. Thorough fabrication drawings will ensure consistent quality construction and provide vendor-independence as well as personnel-independence.
29. For any boards that will be assembled by a contractor, circuit board design guidelines should be adhered to. These guidelines are typically provided by the assembly contractor. The reliability and bug rate of subassemblies could be affected. Meeting Class-2 or Class-3 standards requires efforts of both the designers and the manufacturers.
30. The VHDL module provided for our inspection appears to be of good quality; however, like other documentation provided, it lacked a document number, authorship information, project information, etc. in the file header.
31. The RDO board design seems to be a good candidate for hierarchical blocks, yet the schematics did not use them. There may be some good reason they were not used. It is our feeling that hierarchical blocks simplify the propagation of changes, reduce risk of error, and make the design easier to follow.