1 Data Acquisition and Readout

1.1 Requirements

The data acquisition system is designed to read out the large body of data from the individual sensors, to digitize the signals, to perform data compression, and to deliver the sparsified data to an event building and storage device. A summary of the requirements is provided in Table 1.

Total number of pixels	98×10^6
Number of pixels per chip	640×640
Pixel Readout rate	10 ns (100 MHz) 2 x 50MHz / chip
Readout time per frame	4 ms
Dynamic range of the ADC	10 bits
Raw data from one sensor using a 10 bit ADC	1 Gb/s
Fixed pattern noise	2000 e^-
Noise after Correlated Double Sampling	10 e^-
Maximum signal	900 e^-
Dynamic range after Correlated Double Sampling	8 bits
Total power consumption	90 W

Table 1: Requirement Summary - constraints for the APS, due to signal expectation, available design process, and mechanics

Digitizing the analog signal on each pixel into a 10 bit digital signal yields approximately 1 Gb/s per sensor chip when read out in 4 ms. Thus, the total front end data rate is ~240 Gb/s. Clearly the volume of data must be reduced before being handled DAQ event builder and written to storage.

Data compression is achieved by performing correlated double sampling (CDS), i.e. subtraction of two consecutive frames followed by zero suppression. CDS cancels out fix pattern and reset noises and reduces 1/f noise. The fixed pattern noise corresponds to the spread of the baseline voltage in all pixels. It has been measured on the MIMOSA-5 chip to be 2000 electrons. The noise remaining after CDS must be on the order of 10 e^- to guarantee an efficiency of greater than 99%. The maximum signal is estimated from dE/dx calculation and by measuring how the charge spreads over pixels. The signal can be truncated above 900 e^- without compromising either the efficiency or the position resolution, so 8 bits is a sufficient dynamic range for signal storage. Hit finding and the reduction of the data to addressed clusters then reduces the data to a manageable rate. The use of forced air-cooling on the low mass region of the ladder limits the total power dissipation to about 100 - 150 mW/cm^2.

1.2 Architecture

A sketch of the readout architecture and a description of the data flow is shown in Figure 1. Figures 30 and 31 show a schematic representation of the ladder assembly and the HFT motherboard / daughter card assemblies. The basic flow of a ladder data path starts with the APS sensors. Analog data is carried from the two 50 MHz outputs in each sensor in parallel on the low mass cable to discrete electronics at the end of the ladder and out of the low mass detector region. This electronics performs current to voltage conversion and drives the signals in parallel over a short (1 m) twisted pair cable to the motherboard. The daughter cards on the motherboard perform analog to data conversion of the data, correlated double sampling and hot pixel removal. The data is then transferred to the motherboard for hit finding and data reduction. The reduced data is then buffered and transferred to the STAR DAQ system over a high speed bidirectional fiber link. We intend to use the Source Interface Unit (SIU) and Readout Receiver Cards (RORC) developed for ALICE as our optical link hardware to transfer data to and from the STAR DAQ system. These links have been chosen as the primary readout connections for the new STAR TPC FEE. Leveraging existing hardware and expertise in STAR allows for a faster and more reliable design than developing our own custom solution. The complete system consists of a parallel set of ladder readouts consisting of 24 separate chains. The data may be combined at the optical transfer stage depending on the final rates, which will be determined by our final data reduction efficiency.

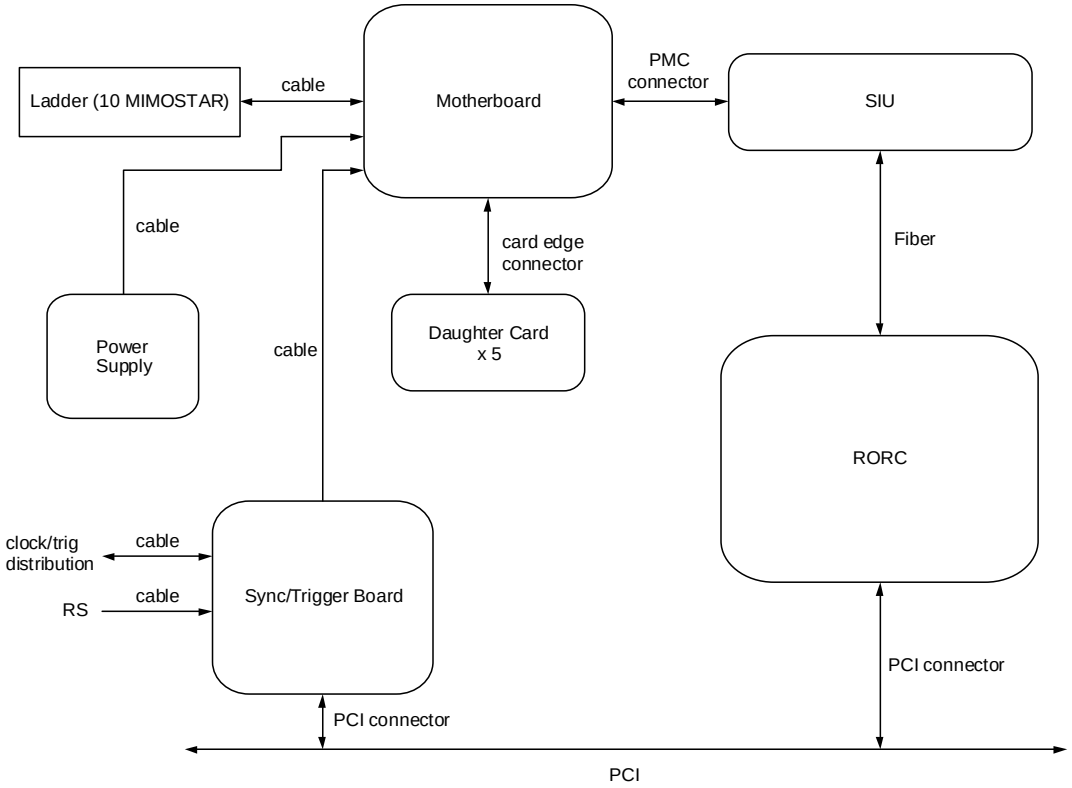

Figure 1: DAQ Layout: schematic of DAQ system for a single ladder. Analog data is carried as differential current on the low mass cable at 50 MHz. The signals are driven in parallel over short (~1m) twisted pair cables to the motherboard. Analog to digital conversion, CDS and data reduction are performed in the Motherboard / Daughter cards. The reduced hit data is transferred digitally to the SIU and carried to linux based readout PCs via an optical fiber. Control, synchronization and event ID tagging are accomplished in the Synch/Trigger board.

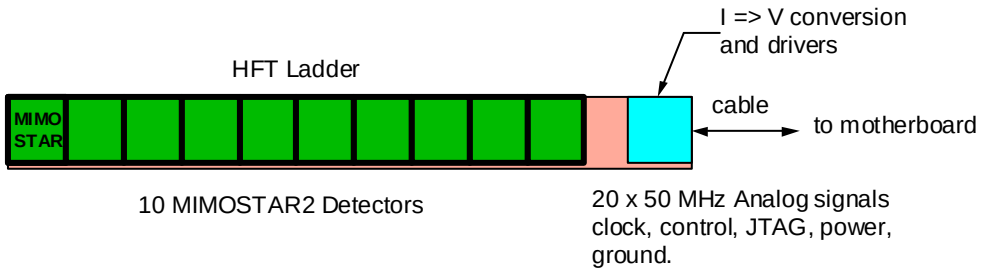

Figure 2: Ladder Layout - sketch of the readout-topology on a detector ladder. This figure shows the ten APS and the corresponding current to voltage conversion and driver electronics. The drivers will be located out of the low mass region of the detector and may require additional cooling.

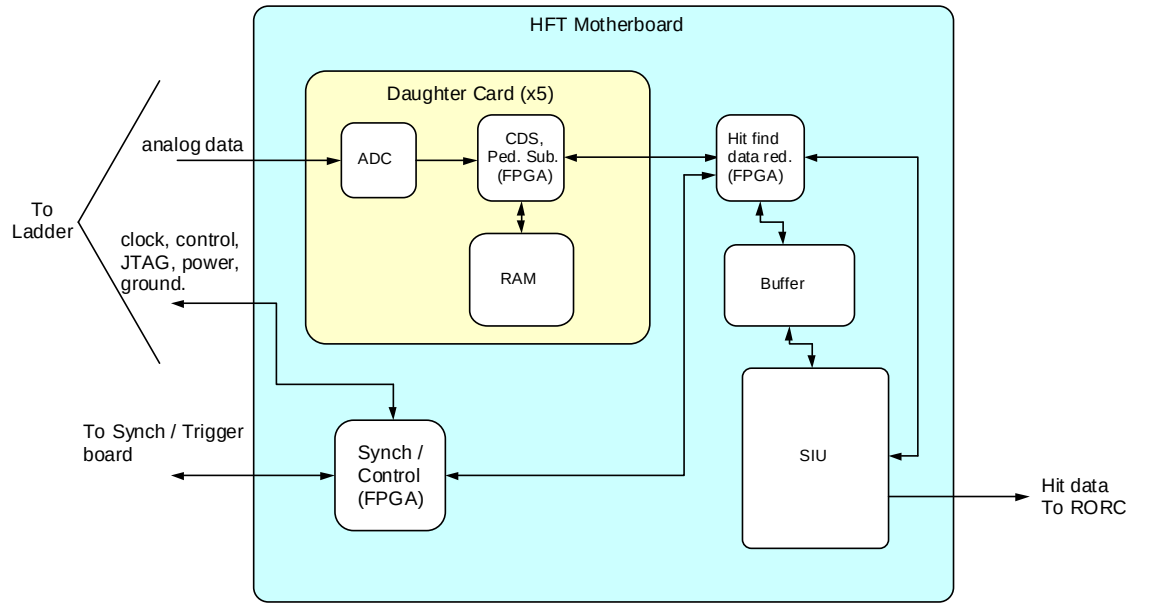

Figure 3: HFT Motherboard functional layout. This figure shows the functional layout of the HFT Motherboard and Daughter cards. There are 5 daughter cards per motherboard to process the data from one ladder. Correlated double sampling, pedestal subtraction and hot pixel removal happen at the first stage of processing on the daughter cards. Hit finding and reduction of the data to addressed clusters happens on the motherboard. Data is then transferred via optical fiber to the RORC cards where it is picked up by the STAR DAQ.

Data from the ADCs is 10 bit. Performing CDS and pedestal subtraction requires 1 data sample to be stored along with one bit hot pixel map. This drives the need for external RAM on the daughter cards. Hot pixel removal can be done in the same lookup operation used for CDS and data is then passed to the motherboard. After CDS the data can be represented by 8 bits.

We are investigating methods of hit finding and data reduction for use on the motherboard. A simple high threshold hit read out with the surrounding 8 pixels is our default approach. This can be implemented in an FPGA and run as a pipeline filling the output buffer with ADC and address values. A simple example of an FPGA logic diagram that accomplishes this can be found on the web[i]. Additional methods currently under investigation include summing algorithms around different thresholds and centroid determination by geometric pattern with high and low thresholds.

1.3 Data Synchronization, Readout and Latency

The readout of the HFT sensors is continuous. The detector as a whole will be triggered as per the standard STAR TCD module. Since 4 ms are required to read out the entire frame of interest, the data will be passed to DAQ for event building ~ 4 ms after the

trigger is received. The current model we are proposing is one where we fit most easily into the existing STAR trigger and DAQ scheme. Our detector will be triggered and go busy until the event is read and we are ready to be triggered again. While this approach is the most simple and robust, it gives a maximum event rate of 250 Hz and a full event correlation (between the TPC and HFT) of the same rate.

There are other possible readout schemes which can address this. The most obvious is to give the HFT it's own data stream. Events could then be tagged with beginning and ending bunch crossing numbers and the data correlated in the offline analysis. Due to the serial readout nature of this detector, this would often require looking in two consecutive HFT events for hits relevant to an arbitrary event occurrence. We are exploring the feasibility of this solution with the STAR DAQ and offline analysis groups.

A more complicated solution would be to provide the electronics and logic to allow multiple simultaneous event streams in the HFT detector. This would allow triggers at approximately the rate allowed by the TPC (dependant on the number of streams and buffering). We will provide the necessary buffering and logic such that events can be triggered at the same rate as the TPC (1 KHz) and separate events (defined as a complete 1 frame readout with the start of the frame occurring at the receipt of the trigger) will each be ready to transfer to DAQ ~4 ms after the trigger. This scheme also has several drawbacks. The first is the added complexity and additional electronics required to stream and buffer events. The second downside is duplication of data. Each separate event stream would include some data duplicated in the previous event (assuming that the events came less than 4 ms apart). This has the potential to nearly quadruple our data rate.

Regardless of the scheme chosen, synchronization between the ladders/boards must be maintained. We will provide functionality to allow the motherboards to be synchronized at startup and at any point thereafter.

1.4 Data Rates

We have determined that 10 bits of dynamic range is required to give us sufficient signal to noise given the expected signal sizes, noise.[ii] The data rate from each 640 x 640 MIMOSTAR2 detector is thus approximately 1 Gb / sec. The total rate of raw data entering the processing chain in the detector is thus approximately 240 Gb / sec. After CDS, the data can be represented by 8 bits. 10 bits of column address and 10 bits of row address are required for each detector and an additional 4 bits of detector-in-ladder address and 5 bits of ladder address are required to map the detector pixel space. Combining this with the occupancy per layer and the 4 ms frame read time gives a data rate from the detector of 186.3 Mb/sec. This is shown graphically in figure 30. Data is saved on a cluster basis. A cluster is composed of a seed pixel, defined as a pixel that exceeds a high threshold, and the geometrically surrounding 8 pixels. The ADC data for a 9 pixel cluster with complete addresses for the seed pixel are saved for all of the hits in a

frame and the resulting event is read into the DAQ structure. The encoding of just the seed address and a fixed pattern of surrounding ADC values significantly reduces the rate at which data is saved to RCF. Each HFT frame sent to DAQ for event building will have the data rate shown below.

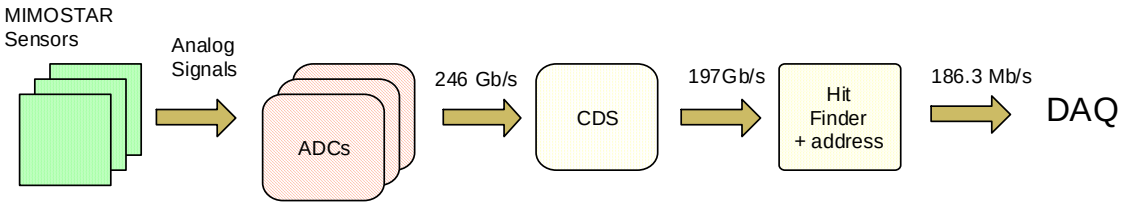

Figure 4: Data rates at the various stages of the HFT readout chain.

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[i] http://www.lbnl.leog.org/data_reduction.pdf
[ii] http://www-rnc.lbl.gov/~wieman/ADCrange.htm