Summary of the STAR meeting at IReS-Strasbourg on Januray 18-20, 2006

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Abstract

The meeting was mainly intended to help preparing the test runs of MIMOSTAR-2 chips foreseen to be mounted on ladders and installed at RHIC in 2006, to discuss the design, production and tests of the final sensors for the intermediate upgrade and to investigate possible chip architectures for the ultimate upgrade.

Issues related to MIMOSTAR-2

Tests of MIMOSTAR-2 on ladders

LBNL exposed its plans to mount 4 MIMOSTAR-2 chips on 2 ladders and to install them in STAR before the end of 2006. The test objective is in particular to operate the sensors inside the STAR DAS and to investigate the beam background. An existing STAR board will be used, on which a mezzanine board adapted to MIMOSTAR-2 will be mounted. The board will be equipped with FPGAs doing the cluster reconstruction. The corresponding algorithm should be developed using real MIMOSTAR-2 data.

MIMOSTAR-2 operation

The operation of MIMOSTAR-2 was discussed, based on the demonstration of MIMOSTAR-2 running on a test bench at IReS.

It was agreed that LBNL will get 6 naked MIMOSTAR-2 chips as well as 1 tested sensor mounted on its PCB.

MIMOSTAR-2 beam test data

LBNL intends to use MIMOSTAR-2 data collected by IReS with a $\sim$ 5 GeV electron beam at DESY in order to optimise the cluster algorithm being implemented in FPGAs equipping the DAS board of the ladders mentioned above. For its studies, LBNL intends to superimpose real signal clusters to frames taken without beam in order to check the algorithm performance (detection efficiency versus fake hit rate). Up to now, no data were collected with beam off. It may be done in June-July during the scheduled beam tests at DESY. These tests may also include runs with the sensor inclined at $\sim$ 45 and $\sim$ 30 degrees in order to adapt the FPGA algorithm to clusters produced by inclined tracks.

For the time being, IReS will provide LBNL with the beam test raw data of about 5000 hits collected with radiation tolerant pixels at 40°C, with 2 ms integration time. The information should consist in ADC counts for the 5x5 pixels building a cluster, after CDS and pedestal subtraction. The raw data of empty frames taken at IReS in the same conditions would be very welcome. IReS will investigate what can be done.

Remaining steps for the intermediate upgrade

The way to the final chip goes through an intermediate sensor, called MIMOSTAR-3, which features the final architecture but has only half the size of the final chip, named MIMOSTAR-4. MIMOSTAR-3 is planned to be sent for fabrication by the end of June 2006, and is expected to allow estimating the production yield of the technology. MIMOSTAR-4 should be sent for production early April 2007.

MIMOSTAR-3

MIMOSTAR-3 is made of 640 x 320 pixels (30 μm pitch) and has two analog outputs implemented on the same side of the chip and running at 50 MHz each. The frame read-out time is 2 ms. The fabrication will rely on an engineering run in AMS 0.35 OPTO technology. This run will host several other chips, some of them relevant for the ultimate upgrade architecture.

LBNL and IReS agreed that the sensor fabrication should, a priori, be limited to 2 wafers, and that STAR would only get the MIMOSTAR-3 chips (about 50 pieces) of one of the two wafers. STAR would therefore only pay for half of the MIMOSTAR-3 chips, i.e. $\sim$ 25 keuros. The other wafer would remain at IReS. This scenario, which increases the financial charge of IReS, needs still to be confirmed in the coming weeks, once the 2006 budget of IReS will be known.

Testing the MIMOSTAR-3 chips should go through the following steps:

- Septembre 2006: probe station tests of the two undiced wafers; estimate of the yield and spotting of the bad chips. A detailed list of the parameters to check remains to be done. Once tested, the first wafer will be sent to LBNL;
- Octobre 2006: dicing of all chips on the STAR wafer, including those not for STAR, and thinning of the MIMOSTAR-3 chips to 50 μm in the US. All chips will consecutively be returned to IReS;
- Novembre 2006: probe station tests at IReS of all individual chips not considered as bad by the wafer test. A detailed list of tests needs to be done. If asked by IReS, LBNL will help setting up the parts of these tests which involve experienced handling of the thinned chips;

- Decembre 2006: send first batch of 10-15 tested sensors to LBNL for assembly and mounting on ladder;

- 1st trimester 2007: finish testing the remaining chips at IReS and send them to LBNL.

MIMOSTAR-4

The base line architecture assumes 640 x 640 pixels with 30 μm pitch. The chip would have 2 analog outputs running at 50 MHz, all on the same side of the chip. The read-out time is therefore 4 ms.

An alternative design was also discussed, which features 2 pairs of ouputs and provides a 2 ms read-out time. It was not retained for the base line mainly because the number of electronics channels needed for the 4 outputs per chip was considered as too expensive for the factor 2 reduction in read-out time it allows. The test of MIMOSTAR-2 (and eventualy -3) inside the STAR apparatus may reactivate this discussion. The production yield derived from the tests of MIMOSTAR-3 may also trigger it: in case of low yield, on may rely on the assembly of two MIMOSTAR-3 chips head to head on the ladder.

The fabrication of MIMOSTAR-4 will presumably proceed through a production run, preceeded by pre-production allowing to check the fabrication quality. The chek will consist in testing a few wafers on probe station at IReS. The goal is to equip 4 detectors, each made of 24 ladders, each ladder being equipped with 10 sensors. 960 good sensors are therefore needed, not counting the spares. Depending on the fabrication yield, up to $\sim$ 40 wafers (50 sensors per wafer) may be fabricated (preliminary price estimate $\sim$ 300 - 400 keuros).

The wafers are expected to be back from foundry and ready for tests at IReS early July 2007. The next steps envisaged are listed below:

- July-August 2007: IReS makes the same probe tests of the undiced wafers as those applied in 2006 to MIMOSTAR-3, and sends the tested wafers to LBNL;

- September 2007: the wafers are diced and thinned in the US;

- October 2007 until early 2008: the thinned chips get tested on probe stations in laboratories of the STAR collaboration. STAR will take care of finding these places. IReS cannot take over these tests, at least not for the full set of chips, but will mount several chips on a PCB and test them with an ^{55}Fe source. Details of the testing protocole need still to be defined.

It is expected that at least one full detector (i.e. made of 240 sensors) can be assembled and installed in time for the run starting mid-July 2008. The payment of the dicing and thinning should account for the US property regulations.

The objective of the ultimate upgrade

Details such as the time line of the ultimate upgrade of RHIC are not yet well defined, but the present tentative goal consists in having the final chips fabricated by mid-Summer 2009.

A specific architecture needs to be developed for this upgrade, which makes the best possible use of the time structure of the trigger and DAS. The latter consists of a short time period (typicaly $\lesssim 10\ \mu s$) during which a trigger ($\sim 2\ \mu s$ latency) is expected to fire the data acquisition, followed by a much longer period ($\sim$ 1 ms) needed to read out the TPC. The sensor may therefore feature a signal processing step decorrelated from the charge integration, and only applied to the triggered sensor data.

Various chip architectures were discussed, with and without zero suppression. Power dissipation may be critical since a single column with integrated digitisation and sparsification is expected to dissipate in the order of 1 mW, translating into 150 – 200 mW/cm^2.

The general organisation of the chip would rely on columns processed in parallel. The chip operation includes a continuous cycling over the array, with an integration time of $\sim$ 100 – 200 μs. There would eventualy be in-pixel storage of the integrated charges, but CDS may eventualy not take place inside the pixels. It may then be performed at the column end and only activated by the trigger, for the sake of power consumption. For the same reason, the read-out would be slow (nearly the TPC read-out time).

The details of the signal processing, i.e. ADC or double threshold discrimination for zero suppression, are still open and should be simulated with real data. It seems at first sight that one could leave with a scenario were the complete triggered frames are transmitted to the DAS board after CDS and 2-bit conversion. Complete data processing would then be performed on the local DAS board, which would select seed pixels and limit the data transfer to their position.

Some exploratory structures may already be designed and fabricated in 2006.

Miscellaneous

Thinning

Opportunities seem to exist in industry to thin individual (i.e. diced) chips which are much smaller than a typical reticle size (i.e. $\sim$ 2 x 2 cm^2). Trials to thin MIMOSTAR-1 at APTEK industry have been agreed. 5 chips will be sent to LBNL, where from Leo will arrange the thinning operation with APTEK. IReS needs still to specify the details of this request.

LBNL proposed to participate to exploratory studies helping to control the residual thickness asked to factories supposed to thin sensors as much as possible without degrading the sensor detection performance. Howard M. is expecting IReS to send him a chip for this task.

Activities of IReS students at LBNL in 2006

Possible work programmes of Alexandre Shabetaï and Michał Scełezniak at LBNL within their PhD were discussed.

Alexandre Shabetaï will arrive at LBNL early in February 2006, and is expected to stay until early May. He will work on 3 topics:

- physics analysis based on real data: try using the SVT in order to improve the charm reconstruction efficiency;
- make latch-up tests of the MIMOSTAR-2 sensor;
- back-up the work done by Howard M. with test beam data of MIMOSTAR-2.

His priority will be on the physics analysis and, for about 2 weeks, the latch up tests. His tutor should therefore be Nu Xu and Howard W.

Michał Szełezniak is supposed to arrive at LBNL early May 2006 and to stay until the end of the year. His activity would turn around the operation of the ladders equipped with MIMOSTAR-2 chips, i..e participate to:

- preparation and realisation of laboratory tests of the 2 ladders equipped with MIMOSTAR-2 chips:
  - tests of individual MIMOSTAR-2 chips;
  - assembly and commissioning of the ladders at LBNL;
  - focus on JTAG operation (e.g. see how chips can be connected serially);
  - take care of the interface between chip and ADC.
- preparation and realisation of tests of the ladders at ALS;
- installation and commissioning of the ladders on RHIC beams.

His tutor would be Howard W.

Change of name of IReS

The status of IReS (Institut de Recherches Subatomiques) has chaged since January 1st, 2006. It is now officially bound to two other laboratories, one working in environnement sciences and the other in analytical chemistry. This new entity is called *Institut Pluridisciplinaire Hubert Curien*, abreviated by **IPHC**.