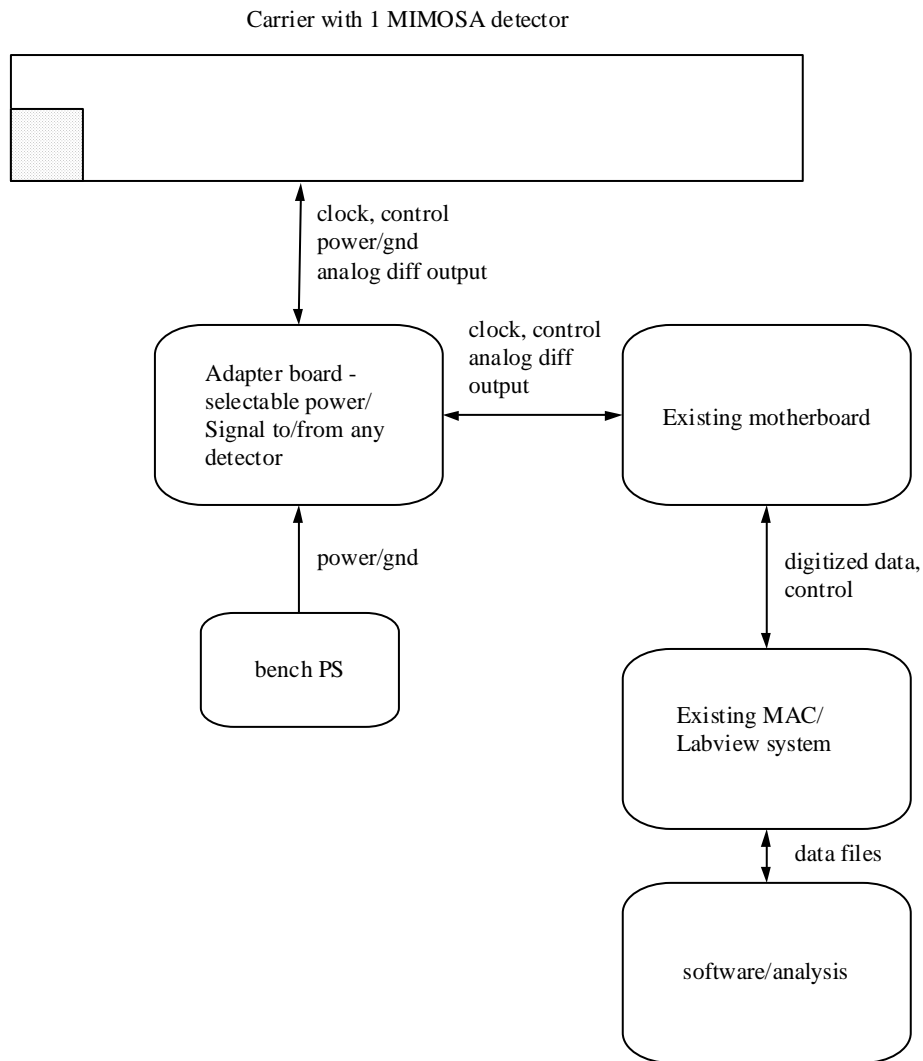LG 10/08/2004 Rev. 2

Proposed Pixel Ladder Prototype Testing for the next 6 months

We are prototyping hardware and electronics for a 10 detector ladder prototype currently under construction. The hardware and electronics construction are staged but can proceed in a complimentary but uncoupled fashion. This is discussed later. The main stages are shown schematically below.

Stage 1 – Carrier with 1 bonded MIMOSA chip using our existing hardware testing setup and existing motherboard. There are ADCs available on the existing MB so all 4 sectors of the MIMOSA can be read out.
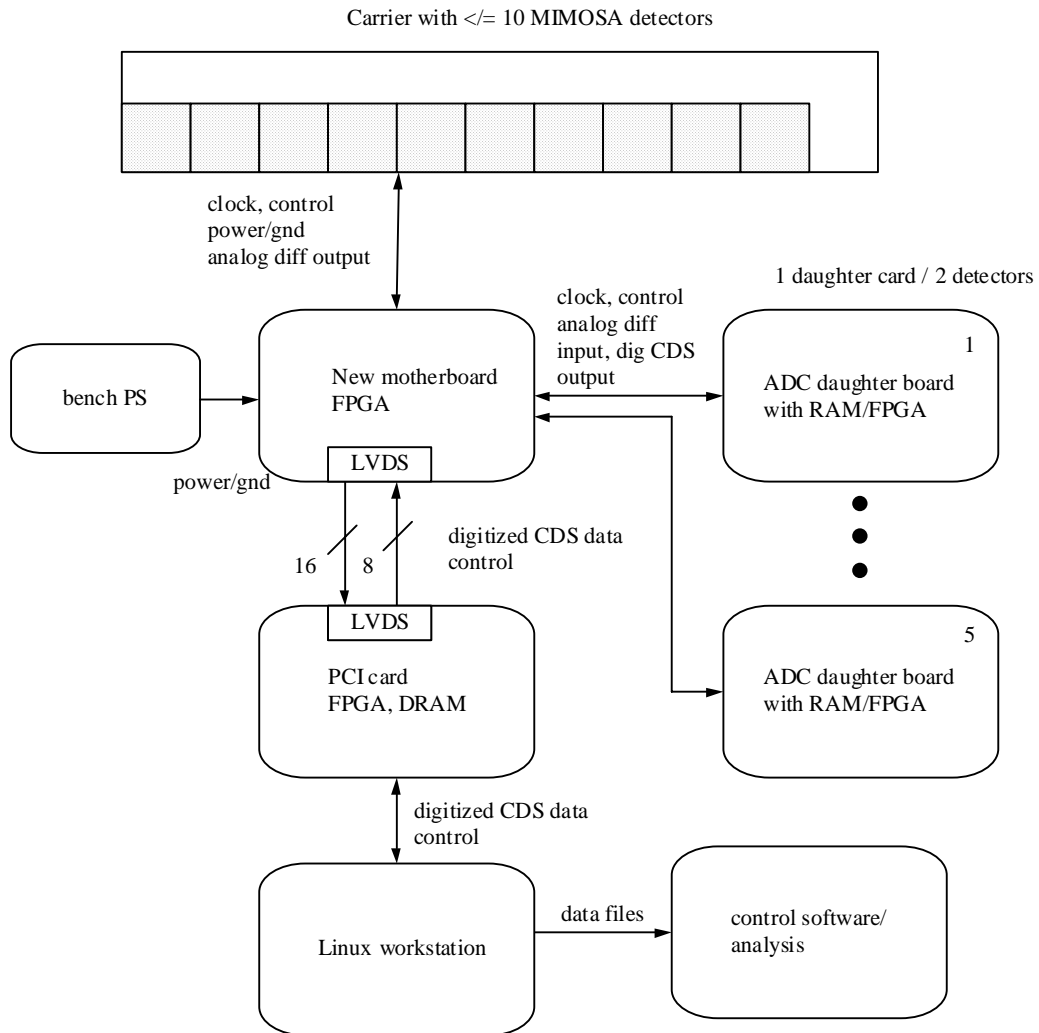
Carrier with 1 MIMOSA detector

clock, control
power/gnd
analog diff output

Adapter board - selectable power/ Signal to/from any detector

clock, control
analog diff output

Existing motherboard

power/gnd

bench PS

digitized data, control

Existing MAC/ Labview system

data files

software/analysis

Stage 1 Pieces	Persons responsible
Carrier with MIMOSA	LG
Adapter board	LG
Existing MB	FB, XX, HM
Existing MAC/Labview system	HM
Software/Analysis	XX, LP, MO, EY

Stage 1 – prototype goals
1. Cable performance with 1 detector
2. Mechanical assembly with 1 detector / bonding

Stage 2 – Carrier with multiple bonded MIMOSA detectors using the new ADC daughter cards and new motherboard read out via the pci based receiver card.

Carrier with </= 10 MIMOSA detectors

clock, control
power/gnd
analog diff output

1 daughter card / 2 detectors

clock, control
analog diff
input, dig CDS
output

bench PS

New motherboard
FPGA

ADC daughter board
with RAM/FPGA   1

LVDS

power/gnd

16   8

digitized CDS data
control

LVDS

ADC daughter board
with RAM/FPGA   5

PCI card
FPGA, DRAM

digitized CDS data
control

Linux workstation

data files

control software/
analysis

Stage 2 Pieces	Persons responsible
Carrier with MIMOSAs	LG

New MB   FB, RG
Pixel DAQ card   FB, RG
Linux workstation   RG, XX
Control software/Analysis   XX, MO, EY

Stage 2 – prototype goals
   1. Cable performance with multiple detectors.
   2. New MB performance.
   3. New daughter card performance.
   4. VHDL CDS performance.
   5. Overall system performance.
   6. Mechanical assembly with multiple detectors / bonding.
   7. Alignment techniques.
   8. Cooling system design and performance.
   9. Beam test?

Construction stages –
　　　　Due to the different requirements for the various stages of construction, the mechanical and electronic stages may not be entirely as shown. Our mechanical construction prototyping and testing may dictate that we bond multiple MIMOSA detectors to the carrier for the stage 1 testing shown. In this case, we can wire bond all of the detectors or only 1 as we see fit since the detector power is jumpered on the adapter board. Stage 2 will be the end point of the ladder prototype testing covered in this document.
　　　　The functionality of each of the schematic boxes is deliberately not detailed. The persons in charge should work out (and document) all of the detailed functionality and interfaces.

Persons – LG = Leo Greiner, FB = Fred Bieser, RG = Robin Gareus, HM = Howard Matis, MO = Markus Oldenburg, EY = Eugene Yamamoto, XX = placeholder for new person.