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# Probe Testing for the Phase-1 Sensors

We are preparing a system to allow for the probe testing of thinned Phase-1 sensors for use in the STAR Pixel detector. In order to achieve the highest possible yield of working ladders, the Pixel detector assembly sequence is arranged such that sensors are probe tested after they have been diced and thinned to 50 microns. We will describe the tests to be performed, the hardware we are developing to accomplish this task and the firmware and software that complete the testing system. A preliminary operating manual for the Phase-1 sensor may be found at http://rnc.lbl.gov/hft/hardware/docs/Phase1/PH1-UserMan-20080916.pdf.

## Tests to be performed on Phase-1 sensors:

We do not intend to characterize each production sensor individually with a source or particles during probe testing. Our goal is to carefully characterize a representative sample of the sensors to develop a good understanding of the sensor characteristics. Then to use these tests to develop a methodology for determining an operating point for the sensors that meets the experimental requirements. We will do a full characterization of a smaller sample of sensors pulled from the production stream. The production probe tests will consist of the following tests.

1. Power on testing – measure the current draw for digital and analog voltages. Reject sensors that are not within tolerance.
2. Test JTAG function to configure the sensor to return the chip ID and to set and read back the nominal operating condition parameters.
3. Measure the DAC setting versus voltage output for the IKIMO, IVDREF1 and IVDREF2 DAC structures.
4. Measure the discriminator output transfer functions of all 4 outputs as a function of IBUFF bias, IPIX, VCLPDISC.
5. Use a flashed LED to find any dead pixels and test general pixel function.

The testing and characterization to be done to the smaller sample (2 functioning sensors per wafer) of sensors will consist of the previous list of production testing as well as the following additional characterization.

6. Measure noise at the analog outputs and compare to the hit rate as a function of discriminator level.
7. Use a $^{55}Fe$ source to generate a spectrum from the analog outputs. Compare this spectrum to the reference.

## Hardware System Architecture

To perform the sensor selection required we are developing a hardware testing system. The hardware system architecture is shown schematically below.

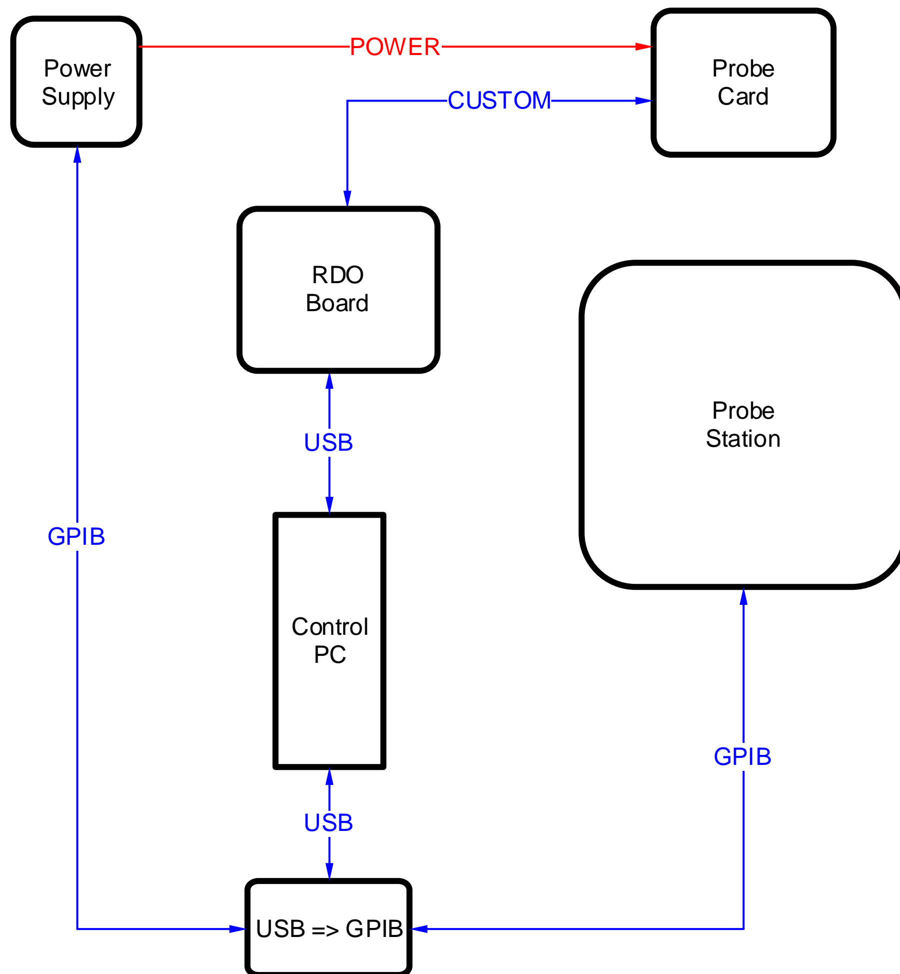


**Figure 1 Phase-1 probe testing hardware architecture shown schematically.**

The system is controlled by a PC running WinXP. The PC directs the Probe station positioning, actuation of the probe card and the power supplied to the sensor using a GPIB connection. The configuration, control and testing data are sent via CAT-5 and ribbon cable from the RDO card to the probe card. The readout and testing sequence are generated in the PC and implemented over the UBS data connection between the PC and the RDO card.

<u>Mechanical Positioning and Holding Phase-1 Sensors</u>

As was previously indicated, in order to achieve the highest possible yield of working ladders, the Pixel detector assembly sequence is arranged such that sensors are probe tested after they have been diced and thinned to 50 microns. This poses additional fixturing requirements as most probe testing is done on full thickness wafers. We will be developing specialized hardware to accommodate the thinned sensors. We will use the same vacuum chuck technology with bump edges for positioning and individually actuated sensor vacuum hold-down bays as used for Pixel ladder assembly. We expect to achieve positioning tolerances of ~25 um of the sensors onto the vacuum chuck. This

filled vacuum chuck will them be mounted to the probe test table. We will modify the probe station software to find fiducial markers on each sensor individually to do alignment for probe testing.

## Firmware and Software

The system is designed to allow for scripted automatic probe testing of Arrays of Phase-2 sensors that have been thinned to 50 um. The main interface will reside on the control PC and be a Labview or Labwindows panel. The firmware modules are located in the RDO motherboard. The software modules are located in the control PC. The basic higher level firmware and software modules are shown below.

| **Control PC** | **RDO motherboard** |
|---|---|
| Probe station control<br>JTAG control<br>RDO control (modes)<br>Power Supply control<br>Data logging<br>Data analysis (root)<br>Database interface<br>Database<br>User Interface | JTAG interface<br>Sensor RDO (analog)<br>Sensor RDO (digital)<br>Parameter RDO (supply current, IKIMO, IVDREF1, IVDREF2, Temp.)<br>LED flash |

## Tracking and Database

The thinned sensors from wafers of Phase-1 sensors (53 sensors / wafer) to be tested need a system of tracking and to have the probe testing results, wafer ID and wafer positions saved in a database. This will allow for the selection of good sensors and for the tracking and analysis of any sensor function related problems that may be observed. The sensors themselves do not contain any distinguishable individual markings and are also quite fragile so the application of external labels to the sensors themselves is not foreseen. The tracking and identity preservation of individual sensors will be accomplished by careful procedural measures with the chip carriers holding the identifying markings. The database will be maintained on a PC. The number of entries is expected to be in the 10k range.