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Phase-1 test summary

- **second batch of sensors,**
- **different voltage biases,**
- **reduced number of decoupling capacitors**

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Test of the second batch of sensors

We have tested the second set of Phase-1 prototypes to obtain a better assessment of the fabrication yield.

Phase-1 prototypes that were tested came from the following wafer positions: A3, B6, C2, D3. The test boards for these four chips were assembled for the digital readout only - no circuitry for analog test readout was loaded onto the test PCBs.

JTAG programming and power consumption

All tested chips respond to JTAG programming correctly. The JTAG parameter space has not been fully tested, but basic configuration and adjustments to BIAS DAC settings work without any problems.

The power consumption for these chips was measured in two instances:

1. when a typical JTAG configuration was loaded,
2. after the START signal had initialized sensor operation.

	JTAG loaded		Running	
	Dig (A)	Ana (A)	Dig (A)	Ana (A)
A3	0.10	0.054	0.11	0.092
B6	0.10	0.056	0.11	0.094
C2	0.10	0.056	0.11	0.095
D3	0.10	0.058	0.11	0.097

DAC linearity

DAC linearity was tested for VREF2 and IKIMO DACs. Good linearity was measured from 0 to approximately 200 counts (0.1 to 2.0 V). Above 200 counts, significant flattening of the DAC response was observed. Minor gain and offset dispersion were observed between tested prototypes for both DACs. An example of measured dispersions is shown in Figure 1 for the VREF2 DAC.
Significant dispersion between chips can be observed in the discriminator threshold value (VREF2 – VREF1) as presented in Figure 2.

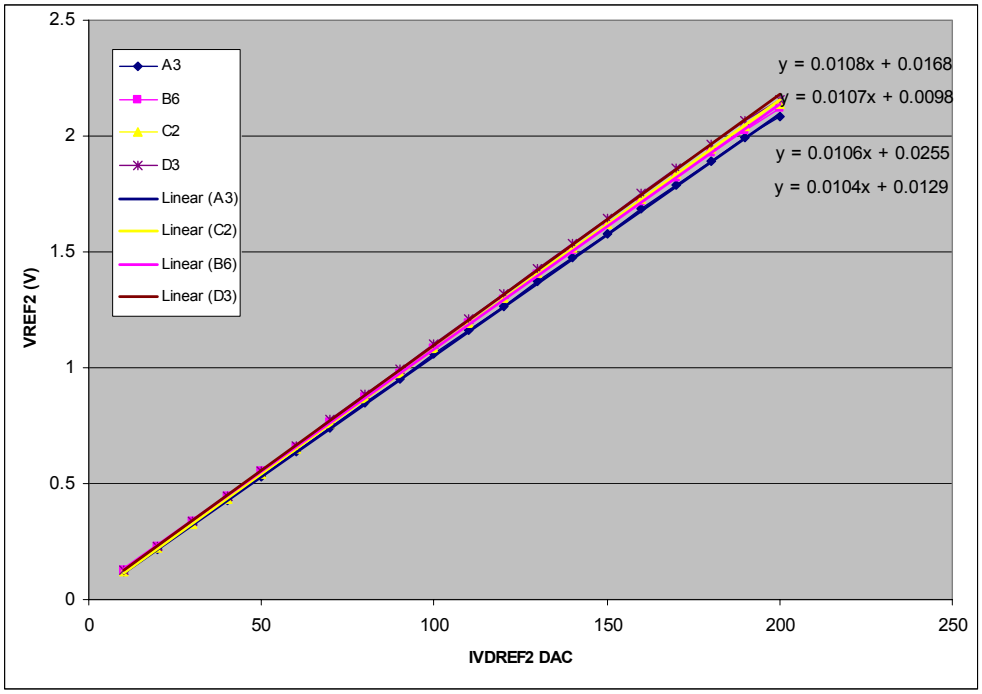


Figure 1 Linearity of VREF2 DACs for 4 tested sensors. Linear fits are added to quantify the dispersion.

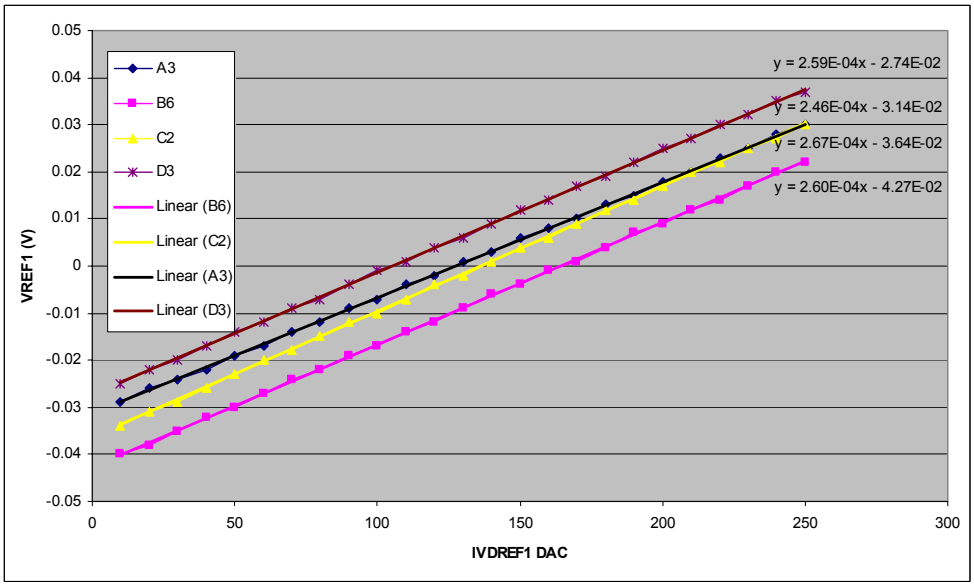


Figure 2 Range of threshold voltages (VREF1 – VREF2) for 4 tested sensors. Linear fits are added to verify the linearity and quantify offset.

The crossing points for Vth = VREF1 - VREF2 = 0 extracted from the linear fits to the measured data points are:

Chip	DAC counts
A3	127
B6	164
C2	136
D3	104

This result is consistent with measurements of the first batch of chips.

Discriminator transfer functions

We characterize the Phase-1 discriminators in the digital readout mode by performing a threshold voltage scan with the pixel signals connected to discriminators and the sensor located in a dark box. The scan starts with low threshold values that allow all pixels to cross the threshold and be registered as "1" on digital outputs. The scan ends when the threshold is high and no pixel signals pass it.

At each scan point we acquire 10 frames of data. This gives us 6400 samples for each discriminator. To extract the characteristics of each discriminator, we calculate a derivative of the transfer function and then fit it with a Gaussian distribution. The mean value and standard deviation of the Gaussian fit represent the crossing point and temporal noise of the column of pixels, respectively.

The offset dispersion or fixed patter noise, FPN, in the sensor is extracted as the RMS value of the distribution of crossing points of all 640 discriminators.

The temporal noise of the sensor is extracted as the mean value of the distribution of temporal noise values for 640 columns.

We have characterized discriminator transfer function as a function of two parameters: ICLPDISC and VREF2.

The scan with different ICLPDISC values was performed with the settings of 20, 30, 40, 50, 70 and 100 DAC counts. The range was chosen based on our previous measurements which indicated that the least dispersion between discriminators was achieved with the lowest value used in the parameter scan, i.e. 30 DAC counts. Since then, we have received a confirmation from IPHC that the operational range of ICLPDISC reaches 30 DAC counts. The lower limit of 20 was set to verify if there is any degradation of performance below the chosen optimum operating point. The upper limit of 100 is the default value specified in the Phase-1 documentation.

The goal of the scan with different VREF2 values was to measure -2, -1, +1, +2 DAC (1 DAC = 10 mV) counts from the optimal value of this parameter. The optimal setting is chosen based on the scope observations of all four digital outputs when threshold voltage for discriminators is set to zero[1] and VREF2 is varied to obtain approximately 50% of pixels showing as "1".
The optimal VREF2 settings for different chips were 82, 80, 81, 78 for A3, B6, C2, D3 chips, respectively. It was not possible in all cases to lower the setting by 2 DAC counts. At these low settings, the lowest threshold voltage available at VREF1 = 0 DAC counts was insufficient to allow all pixels to pass the threshold. .

Plots showing the measurement results are presented in Appendix A. Measured performance is compatible with our measurements with sensors from the first test batch. Again, lower ICLPDISC results in better uniformity in discriminator transfer functions.

[1] VREF1 voltage equal VREF2 voltage for the DAC setting that was extracted from the DAC linearity tests.

We can clearly observe that one end of the discriminator section is highly susceptible to the settings of the tested parameters. At the same time, discriminators in the other end of the pixel array exhibit significantly less variation in performance. This may indicate an issue with the distribution of reference voltages across the discriminator section.

LED test

To check for dead /stuck pixels in the tested sensors we monitored sensor response to a short LED pulse.

In all cases the threshold for discriminators was set at 12.5 mV. An LED pulse was configured to trigger response in all pixels. Dark frame and two frames following the LED pulse were registered. In the dark frames we did not observe any stuck pixels and in the frames after the LED pulse we did not register any dead pixels.

Example of the test result is presented in Figure 3.

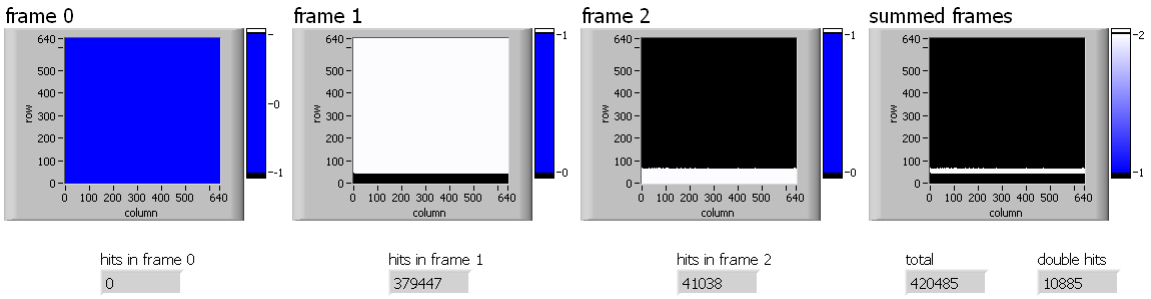


Figure 3 Chip B6 response to an LED pulse. Three consecutive frames are shown: frame 0 before the LED pulse, frame 1 encompassing the LED pulse, frame2 after the pulse. The fourth frame shows the sum of the acquired 3 frames.

Summary

We have extensively tested in total 8 sensors and observed nearly 100 % production yield. We have not observed any dead or stuck pixels in any of the sensor tested. All digital functionality was verified to be operational.

The only problem we have seen so far was a single dead analog test channel in the chip D1 from the first test batch.

The performance of all tested chips is quite similar, and the optimization of performance leads in the same direction (mostly lowering ICLPDISC).

For optimized bias settings, the RMS value of discriminator threshold offsets that we measured varies from 0.6 mV to 1 mV for different sensors. In all cases this FPN value is smaller than the temporal noise estimated at 1-1.2 mV.

Phase-1 performance as a function of bias voltage

The primary objective for this test was to quantify the safety margin available in the power supply voltage of the Phase-1 prototype. We have tested Phase-1 operation under different power supply voltages, ranging from 2.7 V to 3.6 V. The digital and analog voltages were set to the same test value for each test point. We did not measure them independently. We performed this test on the first batch of sensors that have the analog section loaded and available for measurement.

Tests encompassed ^{55}Fe calibrations and characterization of discriminator transfer functions.

Bias settings used for the test included:

- IbufBias = 10 DAC counts
- ICLPDISC = 30 DAC counts
- IPIX = 50 DAC counts (default value)
- VREF2 = 82, 83, 80, 81 DAC counts for chips D1, E3, E4, F4, respectively.

Three sets of measurements will be shown before the results are summarized.

1. Power consumption
2. discriminator performance
3. ^{55}Fe calibrations

Power consumption

The measurements of power consumption of the Phase-1 prototype with different power supply voltages are listed in Table 1 for two different chips.

Table 1 Power consumption of the Phase-1 prototype at different power supply voltages (VDDA and VDDD) tested on two different chips.

	Chip D1 (at Vref1=170)			Chip E3 (at Vref1=100)			On average
Voltage (V)	VDDD (A)	VDDA (A)	Power (W)	VDDD (A)	VDDA (A)	Power (W)	%
3.60	0.12	0.10	0.792	0.12	0.098	0.785	113
3.45	0.12	0.10	0.759	0.11	0.097	0.714	106
3.30	0.12	0.097	0.716	0.11	0.096	0.680	100
3.15	0.11	0.096	0.649	0.10	0.095	0.614	90
3.00	0.11	0.094	0.612	0.10	0.093	0.579	85
2.85	0.10	0.091	0.544	0.09	0.090	0.513	76
2.70	0.10	0.087	0.505	0.08	0.087	0.451	68

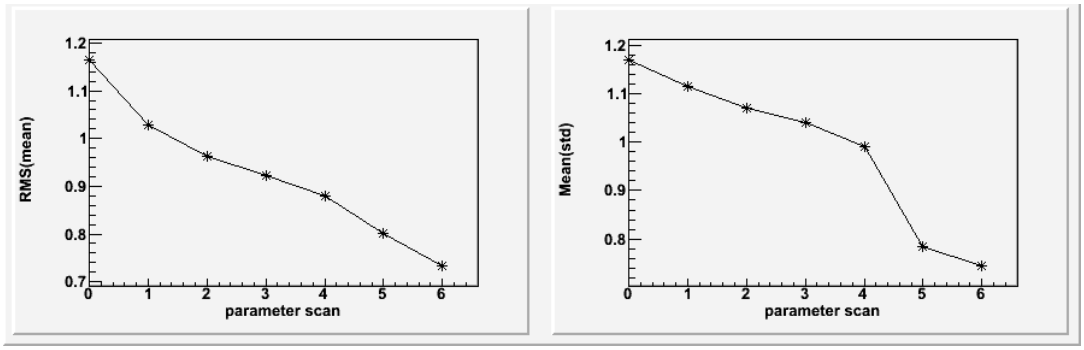
Discriminator performance

Discriminator performance was investigated in the following configurations:

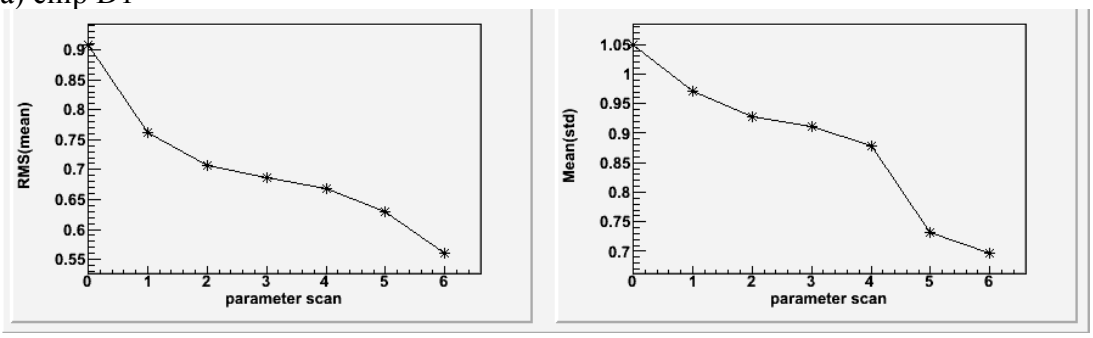
1. Chip D1, E3 scans: 3.6, 3.45, 3.3, 3.15, 3.0, 2.85 and 2.7 V
2. Chip E4, F4 scan 3.3, 3.0 V
3. Chip D1, E4 scan 3.0, 2.95 V

- The goal of the first test was to determine the sensor operation and performance over a wide range of power supply voltage values.
- The goal of the second test was to directly compare operation at 3.3 and 3.0 V on additional sensors.
- The goal of the third test was to verify the operating margin below 3.0 V.

Test results are presented in Appendix B and summarized in Figure 4 and Table 2.



a) chip D1



b) chip E3

Figure 4 Discriminator performance characteristics as a function of power supply voltage in a voltage scan range including 3.6, 3.45, 3.3, 3.15, 3.0, 2.85, 2.7 V. RMS(mean) represents offset dispersion and Mean(std) represents temporal noise.

It can be observed that the offset dispersion and temporal noise are reduced as the power supply voltage decreases. The results at the two last scan points at 2.85 and 2.7 V shown in Appendix B, Figure 20 and Figure 21, indicate that the operation of the sensor is strongly affected at these power supply voltage values. ^{55}Fe calibrations presented in the next section prove that these voltages are too low and severely deteriorate sensor performance.

The measured discriminator performance at 3.3, 3.0 and 2.95 V is summarized in Table 2. (The complete set of results is presented in Appendix B, Figure 22 - Figure 25.)

Table 2 Summary of discriminator performance at 3.3, 3.0 and 2.95 V power supply voltage.

chip	FPN			Temporal noise			Temporal noise (RMS)		
	3.3 V	**3.0 V**	**2.95 V**	**3.3 V**	**3.0 V**	**2.95 V**	**3.3 V**	**3.0 V**	**2.95 V**
D1	--	0.85	0.71	--	1.00	0.93	--	0.034	0.032
E4	0.80	0.72	0.67	1.01	0.93	0.85	0.049	0.060	0.061
F4	0.67	0.62	--	1.01	0.95	--	0.049	0.044	--

The result presented in Table 2 indicates that there is a 5-10% improvement in terms of offset dispersion and temporal noise performance as the voltage is lowered from 3.3 to 3.0 V.

^{55}Fe calibrations

The set of power supply voltage scans described above was accompanied by ^{55}Fe calibrations in a slightly different configuration to optimize storing of large amounts of data required for calibrations.

1. Chip E3 was calibrated at 3.6, 3.3, 3.0, and 2.7 V
2. Chip D1 was calibrated at 3.3, 3.0, 2.95, 2.90, 2.85V
3. Chip E4 was calibrated at 3.0, 2.95 V
4. Chip F4 was calibrated at 3.3, 3.0 V

The results of calibrations are graphically shown in Figure 5 - Figure 7 and fully summarized in Appendix B, Table 3 - Table 5.

Overall, the results show that the senor performance in terms of ENC practically doesn't change for power supply voltages ranging from 3.3 V to 2.95 V. The calibration peak is present at lower ADC count values for lower power supply voltages, but the sensor noise is reduced by the same factor.

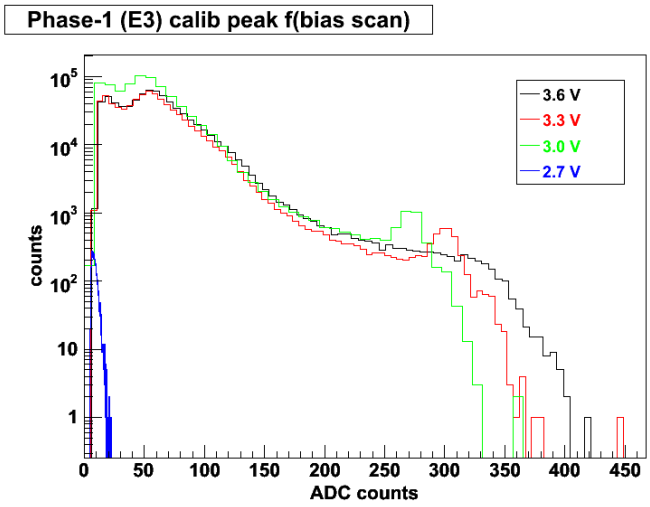


Figure 5 ^{55}Fe calibration spectrum for chip E3 at power supply voltages of 3.6, 3.3, 3.0, and 2.7 V. No calibration peak can be observed with the power supply voltages of 3.6 and 2.7 V.

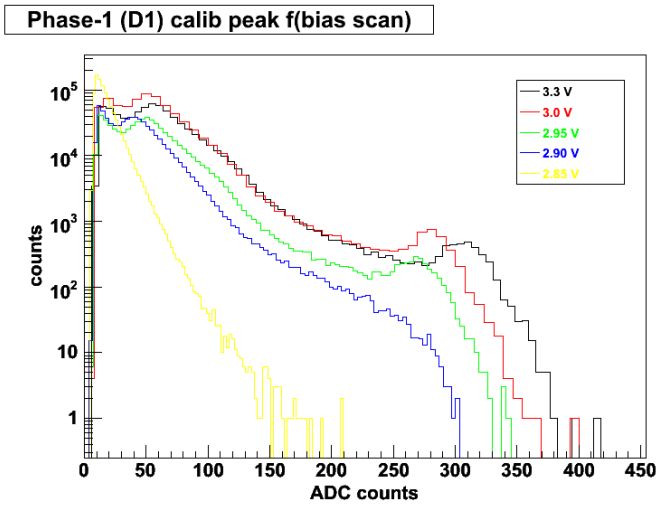


Figure 6 ^{55}Fe calibration spectrum for chip D1 at power supply voltages of 3.3, 3.0, 2.95, 2.90, and 2.85 V. No calibration peak can be observed with the power supply voltage below 2.95 V.

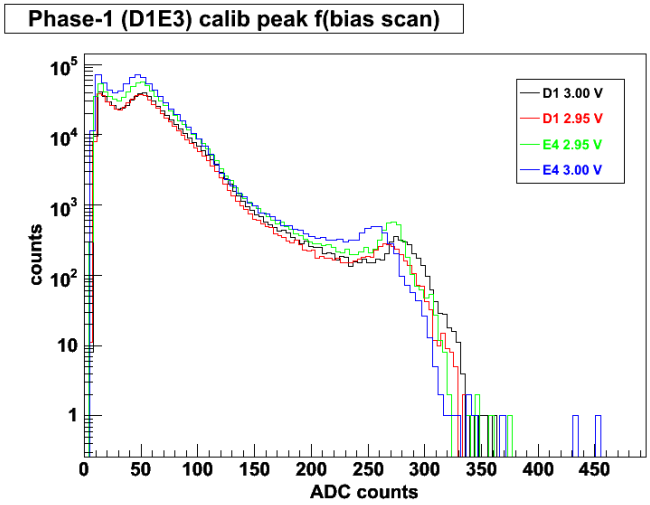


Figure 7 ^{55}Fe calibration spectrum for chips D1 and E4 at 3.0 and 2.95 V power supply voltages. The calibration peak value at 3.0 V is lower than at 3.3V but the senor ENC performance is not affected.

Summary

We have verified that the sensor can operate without loss of performance in terms of analog calibrations and discriminator transfer function when the power supply voltage value is lowered to 3.0 V.

The result presented in Table 2 indicates that there is a 5-10% improvement in terms of offset dispersion and temporal noise performance as the voltage is lowered from 3.3 to 3.0 V. Pixel noise and the calibration peak are also reduced by approximately 10 % in this power supply voltage range.

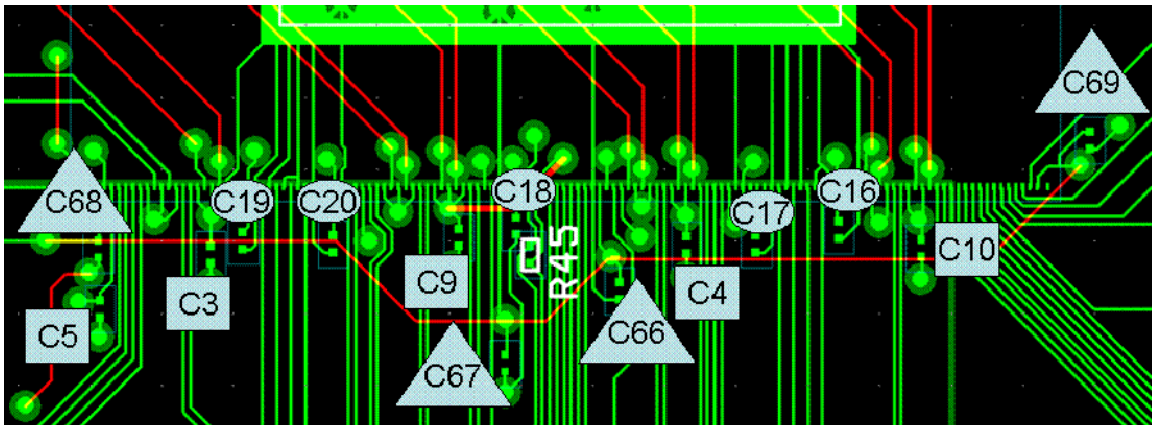
Overall, the presented results indicate that it might be advantageous to operate the Phase-1 prototype at 3.0 V instead of the default 3.3 V. The main advantage arises from a close to 15% reduction in power consumption as shown in Table 1.

Phase-1 performance as a function of decoupling capacitance

In preparations for designing a low mass cable that will provide readout for 10 Phase-1 prototypes we need to optimize the number of decoupling capacitors that are required for proper operation of these prototypes.

We decided to test the performance of Phase-1 with different number of decoupling 100 nF capacitors that were successively reduced from the starting number 14 to 0 at the end of the test. In addition, we extended the path with thin wire to the two lager 10 µF tantalum capacitors that provide the low frequency filtering on the test PCB. This testing is intended to provide a quick look into the Phase-1 performance as a function of the number of decoupling capacitors. The test will be repeated once prototype ladders with multiple sensors are available.

The layout of the decoupling capacitors in the Phase-1 test PCB is shown in Figure 8. The location of 14 100 nF capacitors is shown together with their assignment to the VDDD (squares), VDDA (ovals) power supply lines, and the VCLP reference voltage (triangles).



VCLP 4 capacitors (C66 –section 8, C67-section 5 , C68 – section 1, C69 – section 13)
VDDA 5 capacitors (C16 –section 10, C17-section 10, C18 – section 5, C19 – section 3, C20 – section 3)
VDDD 5 capacitors (C4 –section 9, C5-section 2, C8[2] – section 2, C9 – section 4, C10 – section 11)

Figure 8 Layout of the decoupling capacitors on the Pahse-1 test PCB.

The measurements were performed in the following order

1. reference run

[2] incorrectly labeled C3 in Figure 8.

2. The distance between 10 µF capacitors and the sensor was increased the by approximately 10 cm (half of the planned ladder length) by soldering the capacitors on thin wires.
3. VCLP capacitors C67, C68 were removed
4. VDDD capacitors C5, C9, C10 were removed
5. VDDA capacitors C16, C18, C19 were removed
6. Remaining VCLP capacitors C66, C69 were removed
7. Remaining VDDD capacitors C4, C8 were removed
8. Remaining VDDA capacitors C17, C20 were removed

The chip under test was calibrated with ^{55}Fe at each step and a discriminator transfer function was measured (at ICLPDISC = 40).

The results of the transfer function characterization are presented in Figure 9. The first page of Appendix A explains in details the layout and color scheme used in the figure.

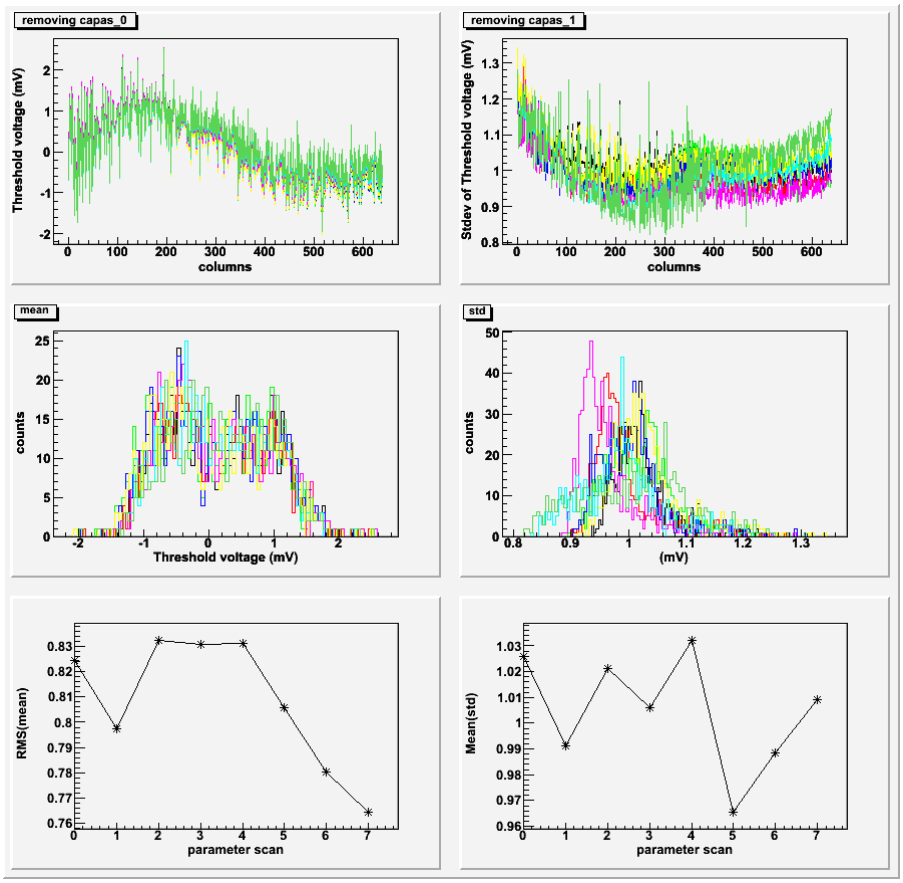


Figure 9 Discriminator transfer function measured for different number of 100 nF decoupling capacitors. Parameter scan points correspond to 14, 12, 9, 6, 4, 2, decoupling capacitors.

The study of RMS of the offset distribution and mean value of noise distribution reveals that there is no quantifiable difference in operation as the capacitors are successively removed. The sensor performance seems not to degrade, even when all 100 nF decoupling capacitors are removed from the test PCB.

The calibration results are presented in detail in Appendix C. The noise and the amplitude of the calibration peak did not change in this test, indicating that the analog performance of the sensor was not affected by removal of decoupling capacitors.

After removing all 14 100 nF capacitors, we also tested the senor performance in different configuration of 10 μF decoupling capacitors on VDDD and VDDA power supply lines.
Performance was compared in four cases:

1. Decoupling capacitors on VDDA and VDDD approximately 10 cm away from the chip.
2. single decoupling capacitor on the VDDA power supply line
3. no 10 μF decoupling capacitors
4. single decoupling capacitor on the VDDD power supply line

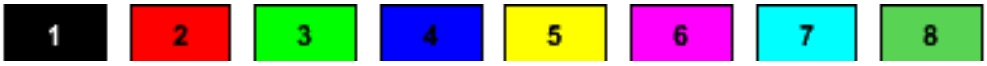
The measurement result and ^{55}Fe calibrations are shown in Figure 27, Figure 28, and Table 7. The result indicates that there is no degradation in performance of the Phase-1 prototype when these low frequency filtering capacitors are removed.

Appendix A
Discriminator transfer functions

The layout of the figures in this section is following:

Mean value of Gaussian fit to discriminator transfer functions plotted as column number	**Standard deviation** of Gaussian fit to discriminator transfer functions plotted as column number
Histogram of mean values	Histogram of standard deviation values
RMS values of mean values distribution as a function of the scan parameter number	**Mean** values of standard deviation distribution as a function of the scan parameter number

The color scheme used in plots:



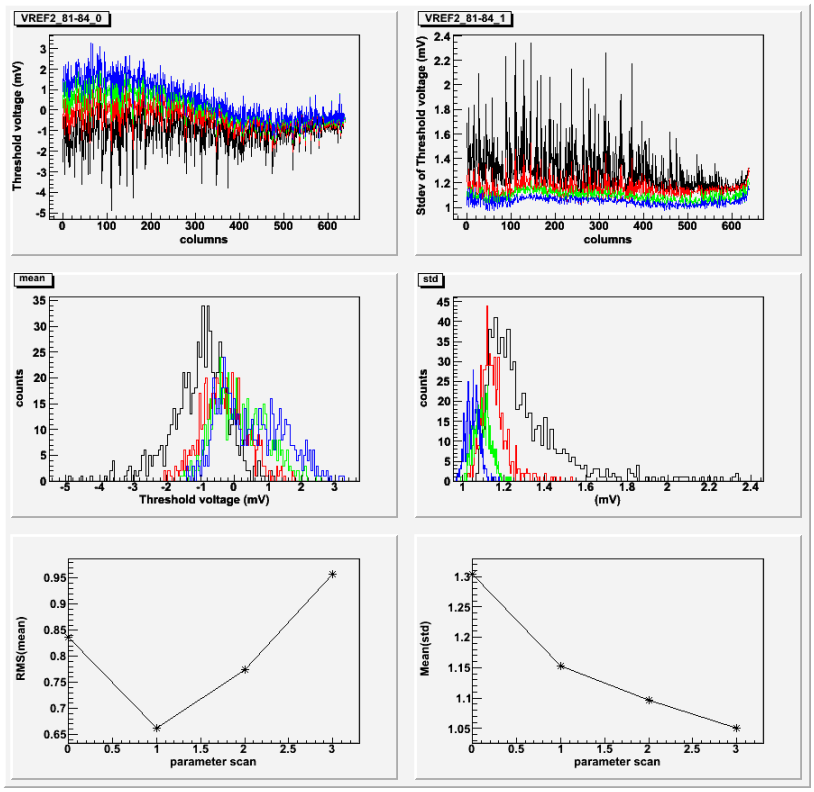


Figure 10 Chip A3; VREF2 scan from 81 to 84 DAC counts. The initial estimation of the optimal setting gives 82 counts.

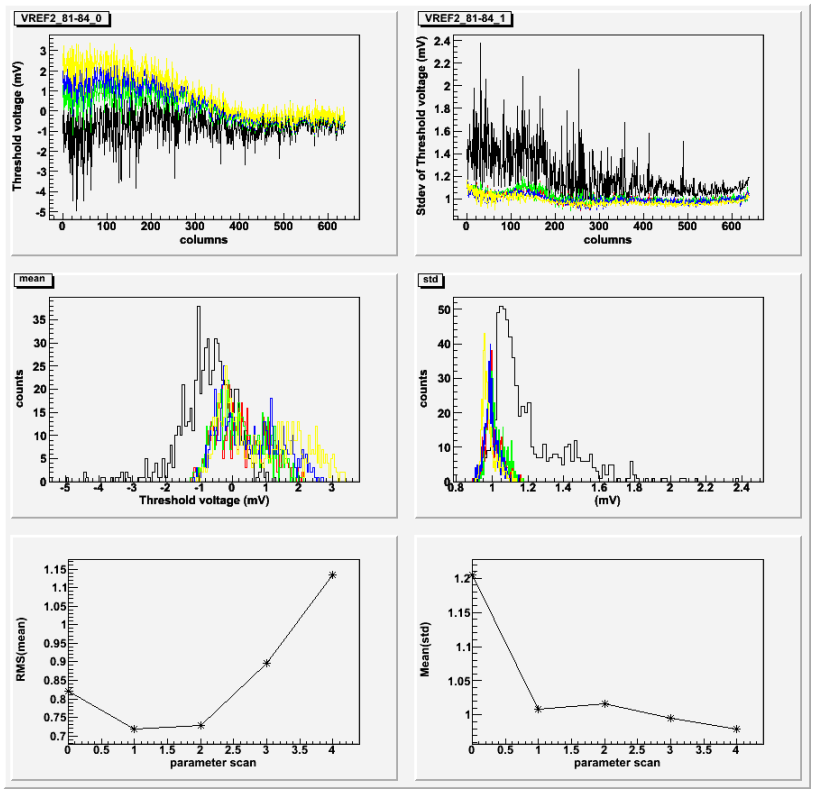


Figure 11 Chip B6; VREF2 scan from 79 to 83 DAC counts. The initial estimation of the optimal setting gives 80 counts.

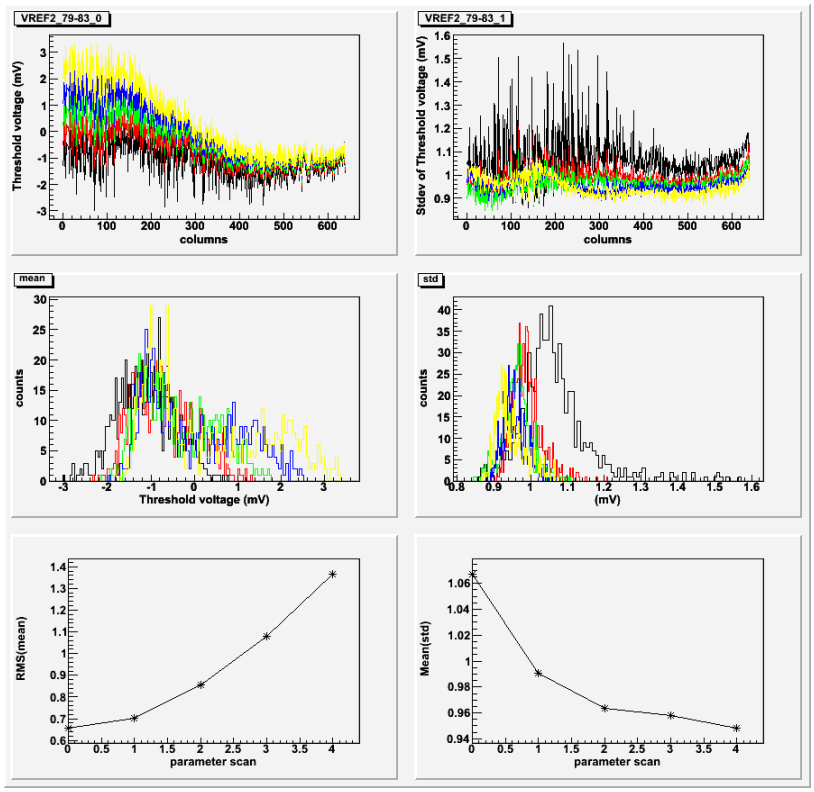


Figure 12 Chip C2; VREF2 scan from 79 to 83 DAC counts. The initial estimation of the optimal setting gives 81 counts.

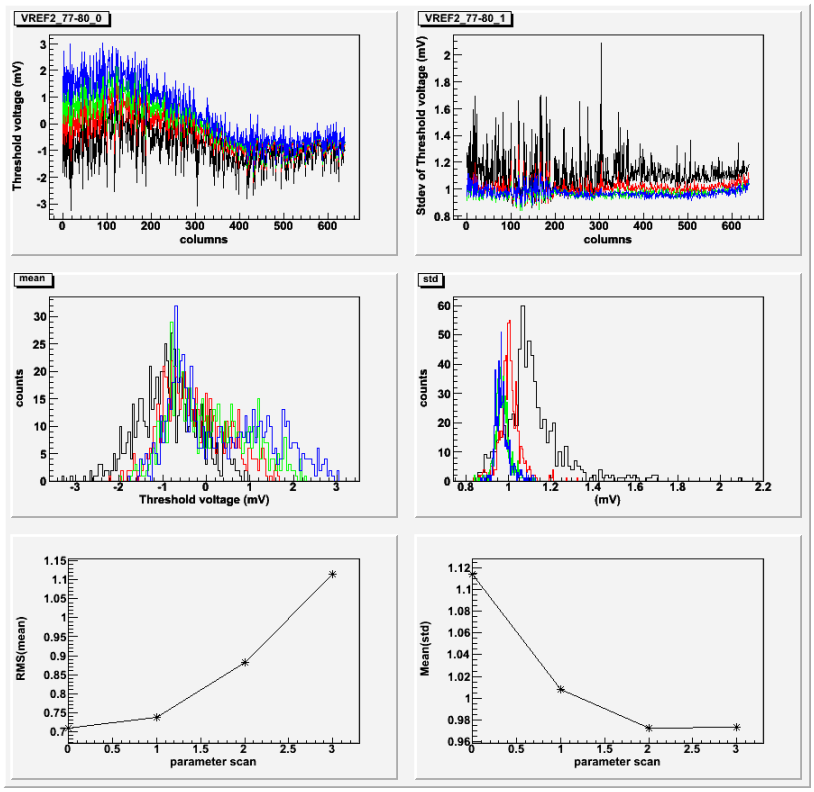


Figure 13 Chip D3; VREF2 scan from 77 to 80 DAC counts. The initial estimation of the optimal setting gives 78 counts;

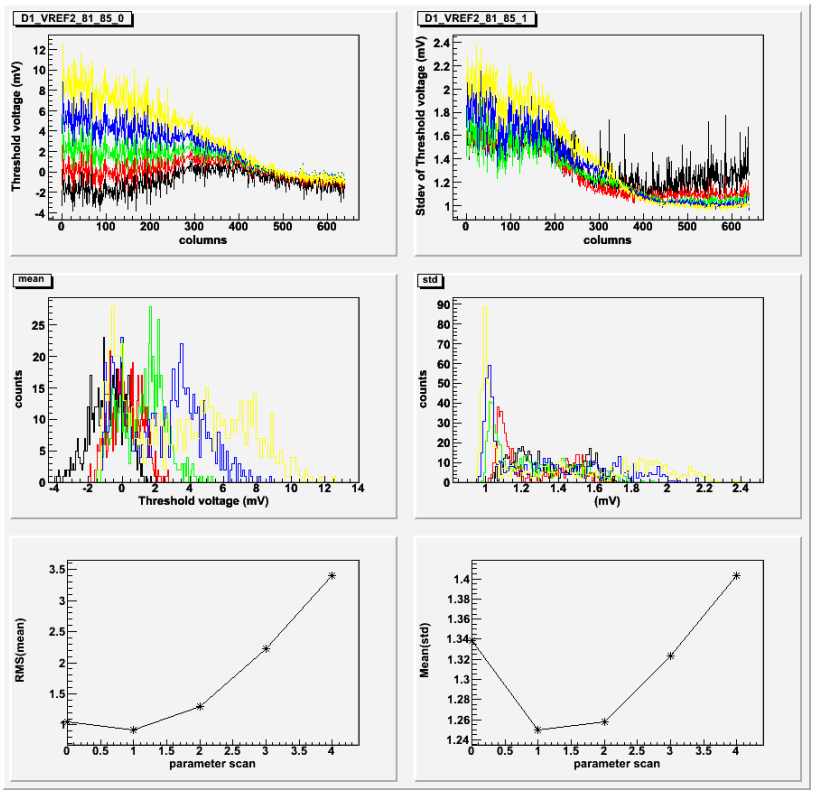


Figure 14 Chip D1 (first batch); VREF2 scan from 81 to 85 DAC counts. The initial estimation of the optimal setting gives 82 counts;

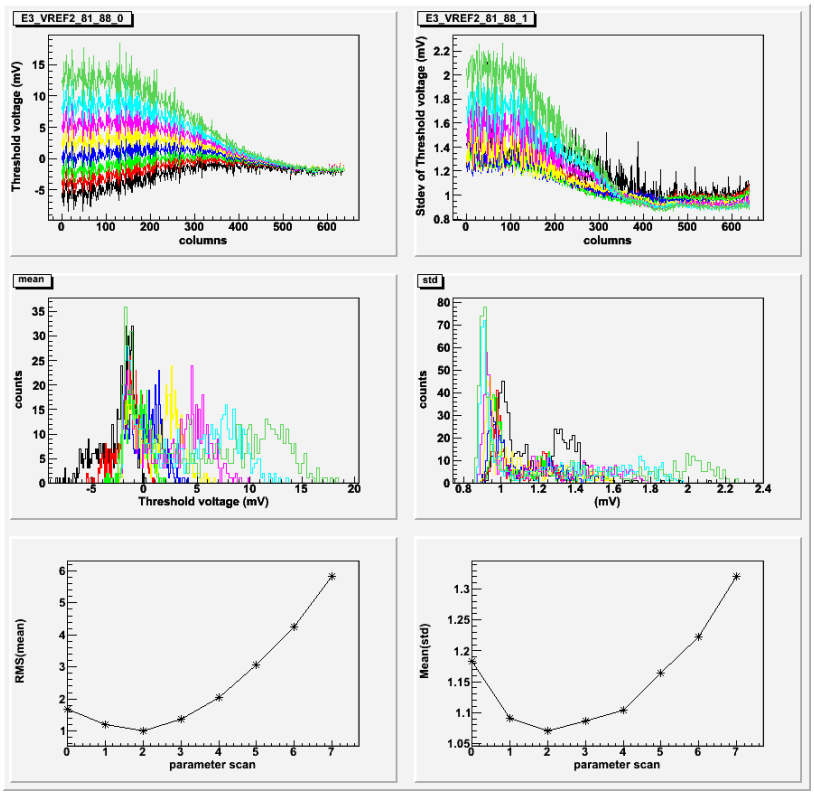


Figure 15 Chip E3 (first batch); VREF2 scan from 81 to 88 DAC counts. The initial estimation of the optimal setting gives 84 counts;

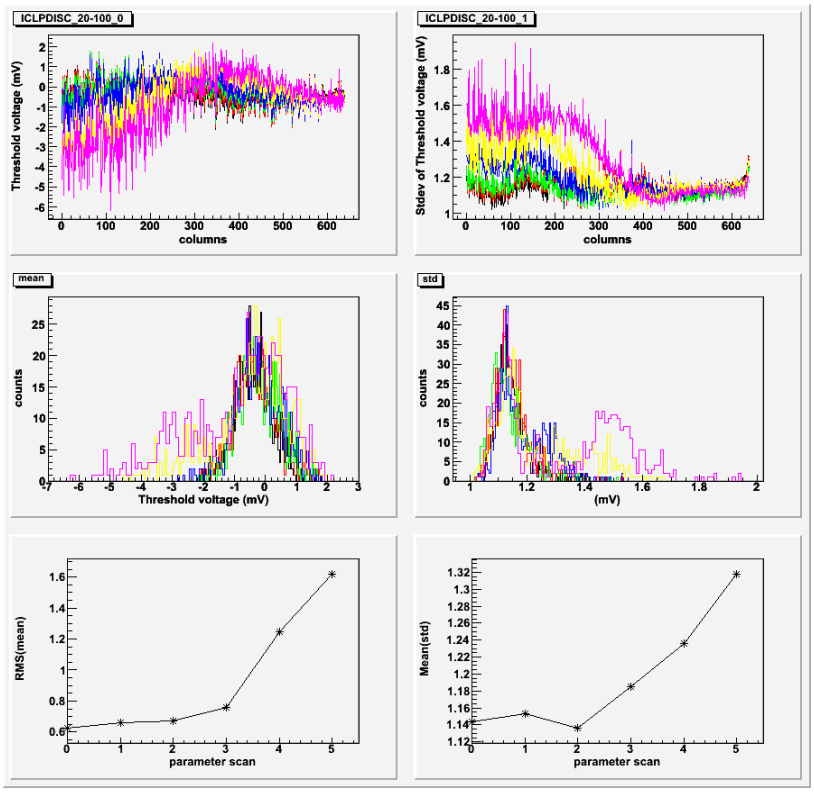


Figure 16 Chip A3; ICLPDISC scan at 20, 30, 40, 50, 70, 100 DAC counts.

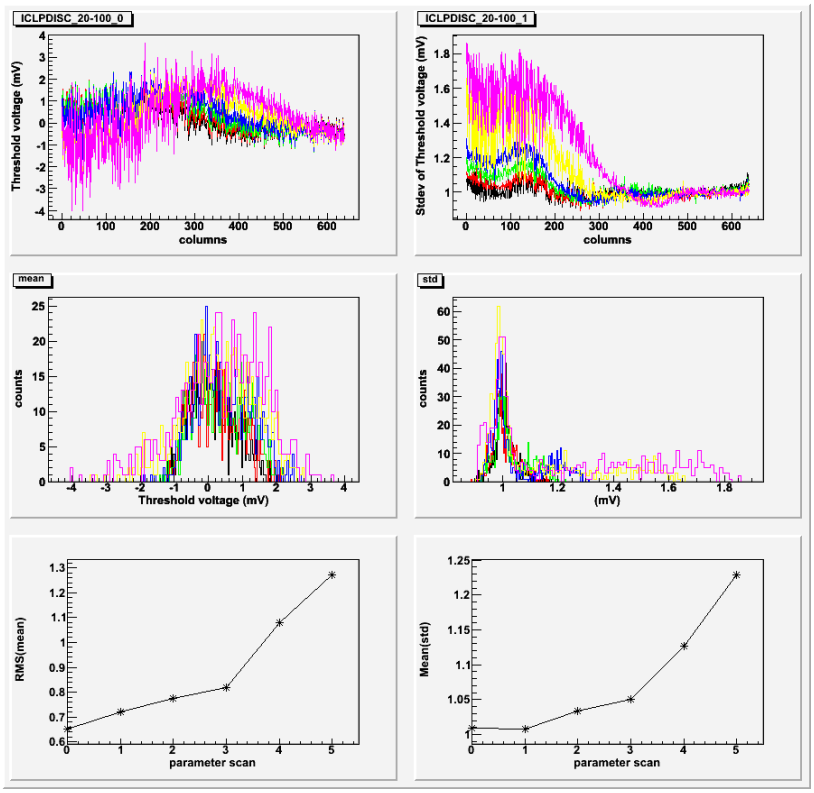


Figure 17 Chip B6; ICLPDISC scan at 20, 30, 40, 50, 70, 100 DAC counts.

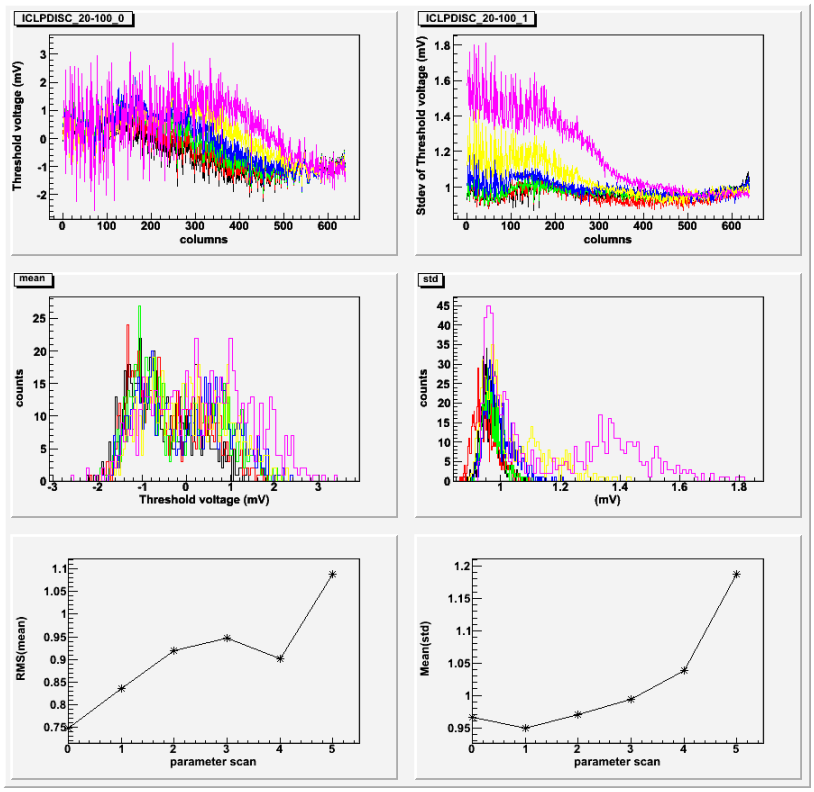


Figure 18 Chip C2; ICLPDISC scan at 20, 30, 40, 50, 70, 100 DAC counts.

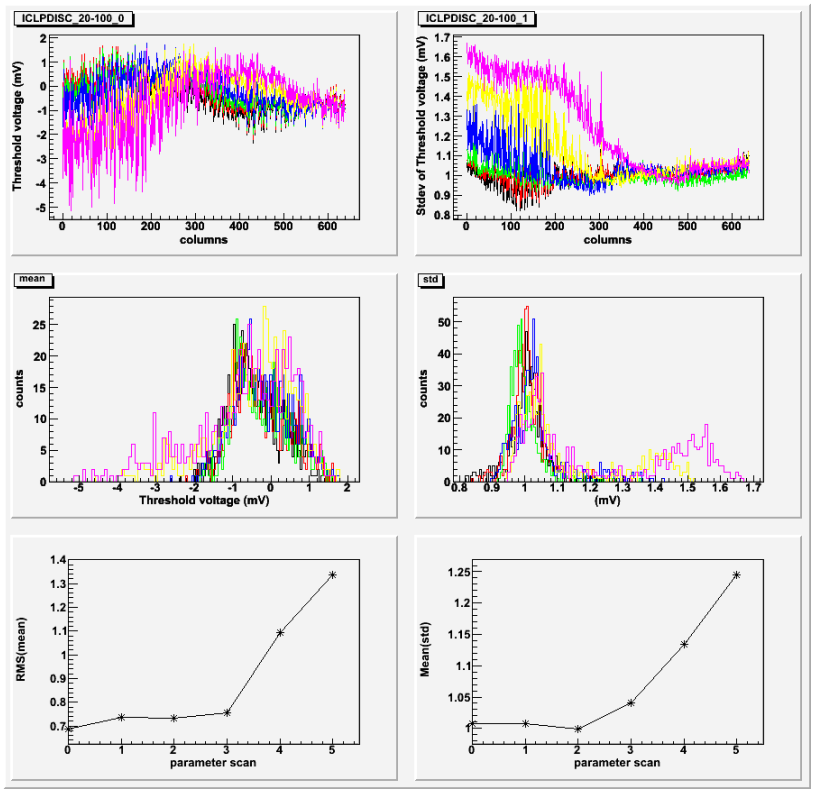


Figure 19 Chip D3; ICLPDISC scan at 20, 30, 40, 50, 70, 100 DAC counts.

Appendix B
Reduced power supply voltage

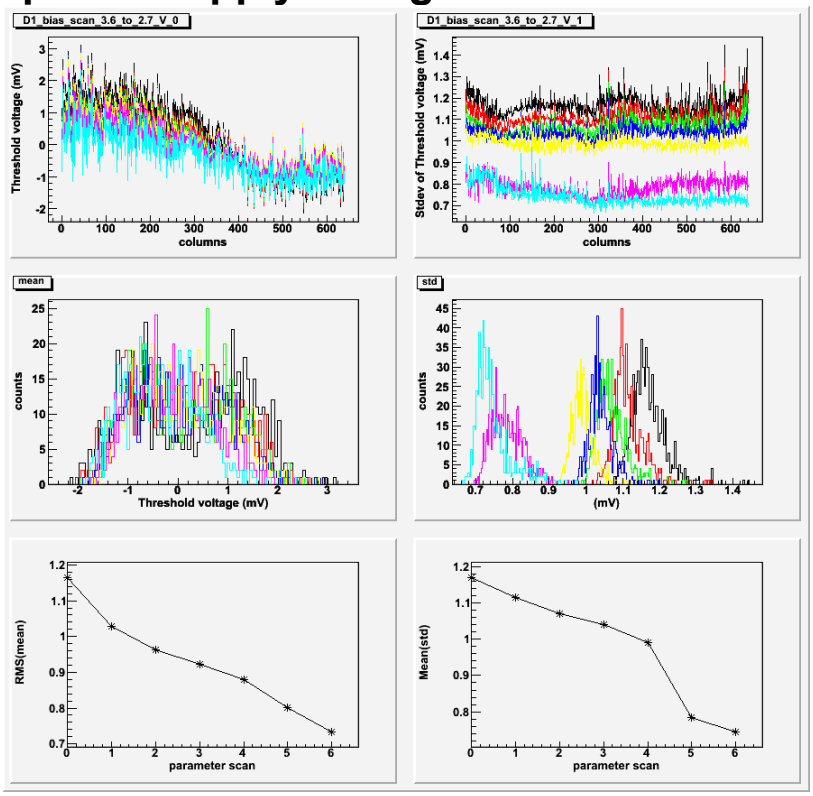


Figure 20 Chip D1 discriminator transfer functions; power supply voltage scan at 3.6, 3.45, 3.30, 3.15, 3.0, 2.85. 2.7 V.

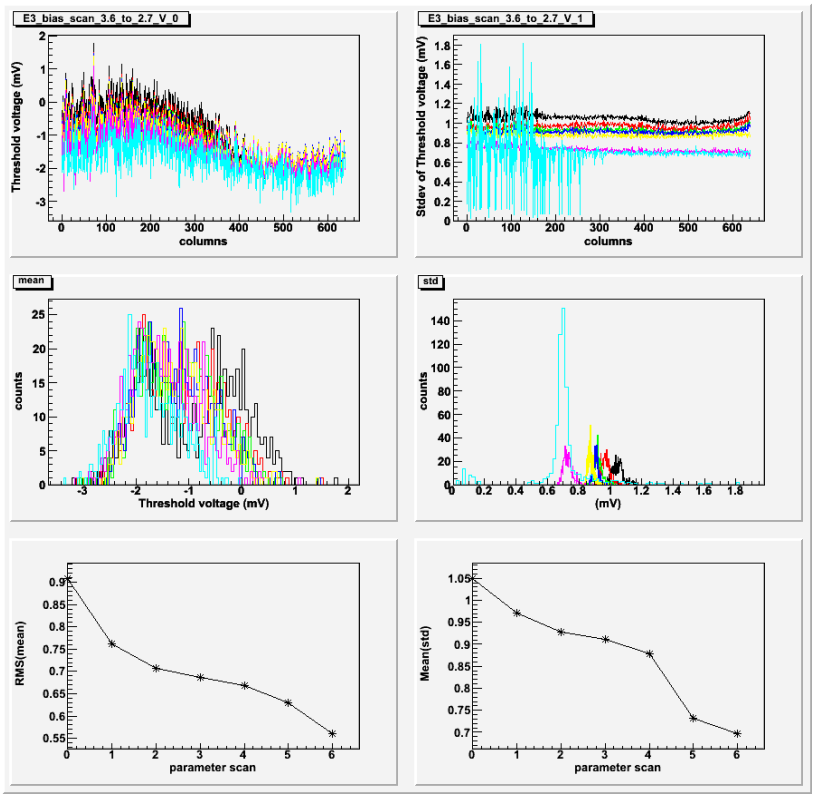


Figure 21 Chip E3 discriminator transfer functions; power supply voltage scan at 3.6, 3.45, 3.30, 3.15, 3.0, 2.85. 2.7 V.

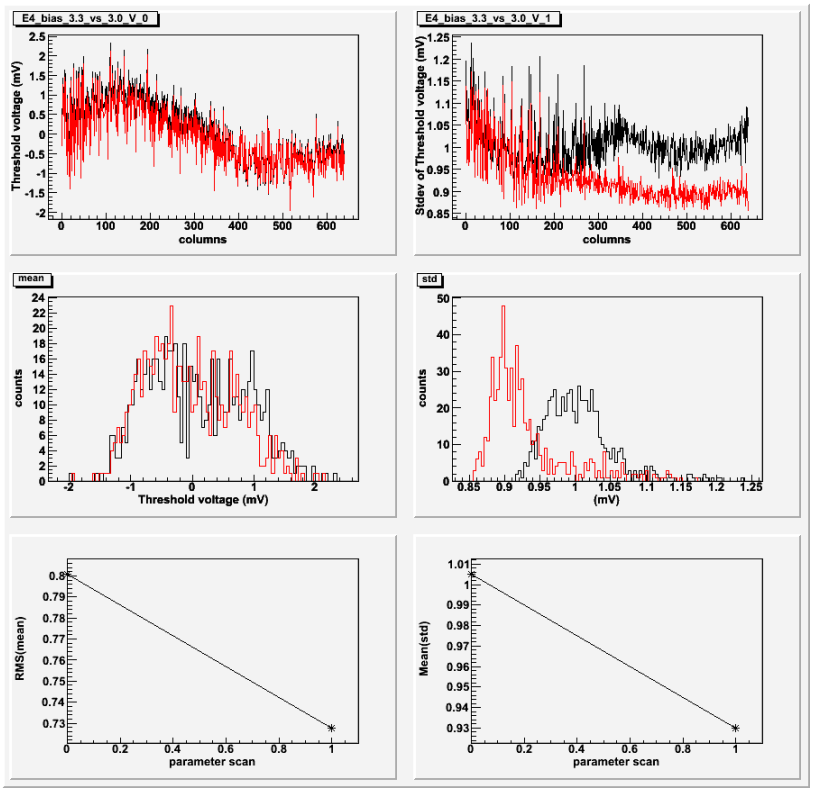


Figure 22 Chip E4 discriminator transfer functions. Comparison of performance at power supply voltage of 3.30 and 3.0 V. (Black – 3.3 V, Red – 3.0 V)

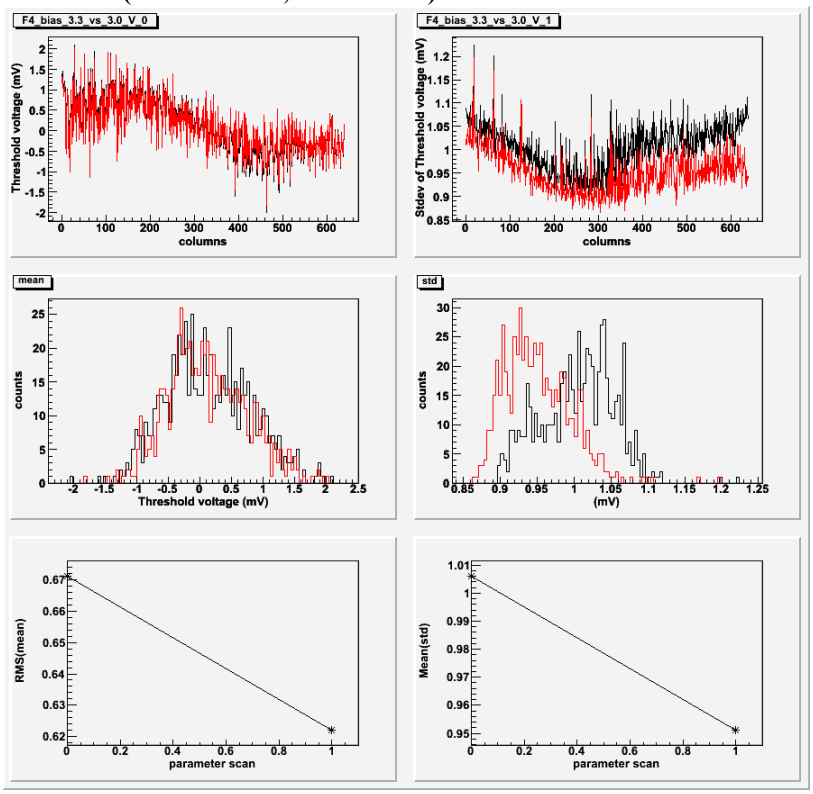


Figure 23 Chip F4 discriminator transfer functions. Comparison of performance at power supply voltage of 3.3 and 3.0 V. (Black – 3.3 V, Red – 3.0 V)

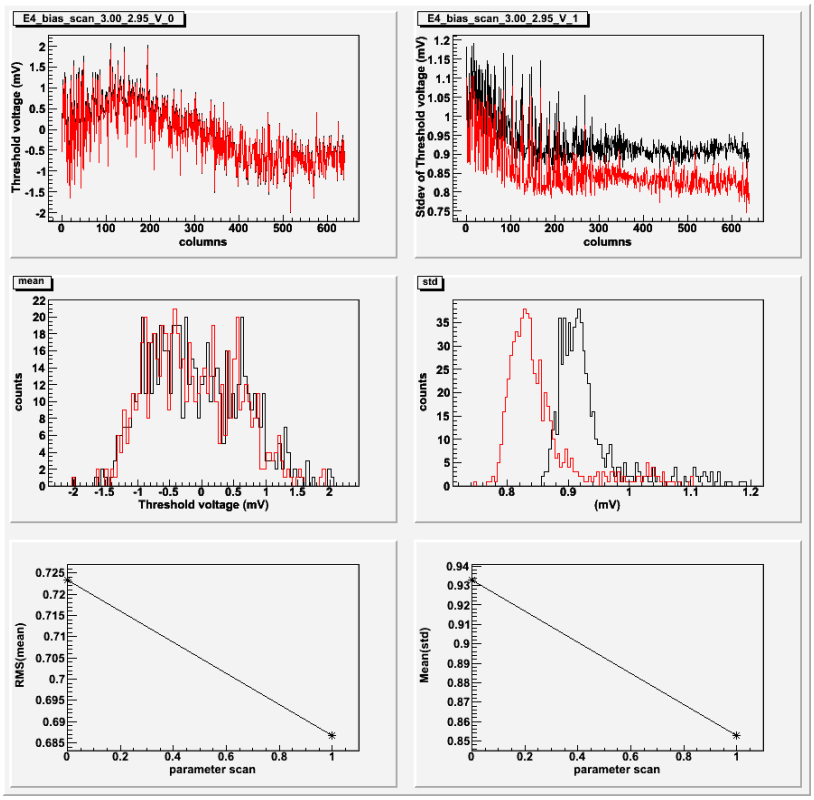


Figure 24 Chip E4 discriminator transfer functions. Comparison of performance at power supply voltage of 3.0 and 2.95 V. (Black – 3.0 V, Red – 2.95 V)

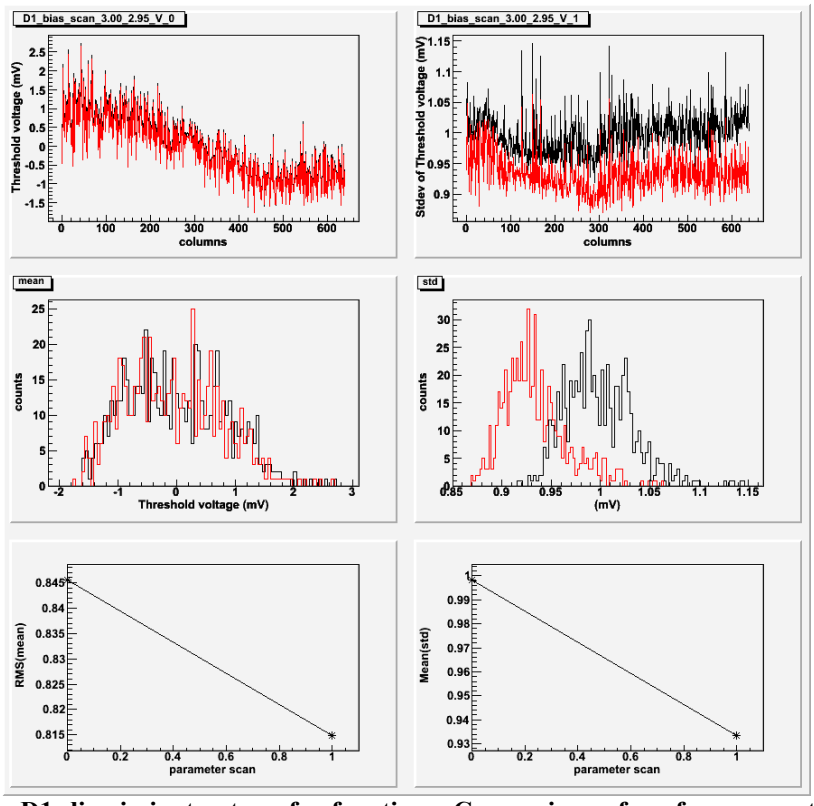


Figure 25 Chip D1 discriminator transfer functions. Comparison of performance at power supply voltage of 3.0 and 2.95 V. (Black – 3.0 V, Red – 2.95 V)

Table 3 ^{55}Fe calibration results for chip E3 at 3.6, 3.3, 3.0 and 2.7 V and chips E4, F4, D1 at 3.3 and 3.0 V

Chip/ bias	Run	Pedestal	Noise	Peak	Peak sigma	ENC
E3 3.3 V	38	2.86 (0.79 RMS)	2.57	299.5	9.7	**14.1**
E3 3.0V	39	3.09 (0.75 RMS)	2.33	270.2	9.9	**14.1**
E3 3.6V	40	3.7 (0.95 RMS)	2.88	NA (signal)	NA	**NA**
E3 2.7	41	1.89 (0.67 RMS)	1.42	(no signal)	NA	**NA**
E4 3.3 V	42	3.0 (0.80 RMS)	2.52	296.9	11.1	**13.9**
E4 3.0V	43	2.9 (0.9 RMS)	2.26	268.4	10.3	**13.8**
F4 3.3 V	44	3.2 (0.80 RMS)	2.61	303	9.5	**14.1**
F4 3.0 V	45	3.17 (0.84 RMS)	2.37	270	10.0	**14.4**
D1 3.3 V	46	2.14 (0.90 RMS)	2. 73	305.6	15.9	**14.6**
D1 3.0 V	47	1.17 (0.78 RMS)	2.48	278.9	14.7	**14.6**

Table 4 ^{55}Fe calibration results for chip D1. Characterization of the space between operational 3.0 V bias and non-operational 2.7 V bias.

Chip/ bias	Run	Pedestal	Noise	Peak	Peak sigma	ENC
D1 2.9 V	48	1.42 (0.81 RMS)	2.15	NA	NA	**--**
D1 2.85 V	49	1.76 (0.76 RMS)	1. 72	NA	NA	**--**
D1 2.95 V	50	1.53 (0.73 RMS)	2.37	266	16.6	**14.6**

Table 5 ^{55}Fe calibration results for chips D1 and E4. Verification of the operating safety margin at the proposed optimal power supply voltage of 3.0 V.

Chip/ bias	Run	Pedestal	Noise	Peak	Peak sigma	ENC
D1 3.00 V	51	1.80 (0.79 RMS)	2.51	278	14.4	**14.8**
D1 2.95 V	52	1.48 (0.70 RMS)	2.40	265	17.5	**14.8**
E4 2.95 V	53	3.04 (0.87 RMS)	2.20	270	10.3	**13.3**
E4 3.00 V	54	**-0.31 (2.26 RMS)**	2.08	251	17.4	**13.6**

Appendix C

Reduced number of decoupling capacitors

Table 6 ^{55}Fe calibration results for Phase-1 prototype with different number of decoupling capacitors.

Set	Pedestal	Noise	Peak	Peak sigma	ENC
reference	2.84 (0.81 RMS)	2.49 (0.55 RMS)	296.6	9.86	**13.7**
10 uF capas 10 cm away	2.90 (0.80 RMS)	2.46 (0,55 RMS)	299.6	9.42	**13.4**
C67, C68 removed	2.96 (0.81 RMS)	2.45 (0.55 RMS)	299.3	9.32	**13.4**
C5, C9, C10 removed	3.59 (0.85 RMS)	2.46 (0.55 RMS)	299.2	9.47	**13.5**
C16, C18, C19 removed	3.36 (0.82 RMS)	2.46 (0.55 RMS)	299.3	9.05	**13.5**
C66, C69 removed	3.47 (0.81 RMS)	2.48 (0.55 RMS)	298.5	10.12	**13.6**
C4, C8 removed	2.95 (0.81 RMS)	2.48 (0.55 RMS)	298.3	9.78	**13.6**
C17, C20 removed	2.80 (0.79 RMS)	2.47 (0.55 RMS)	297.8	10.11	**13.6**

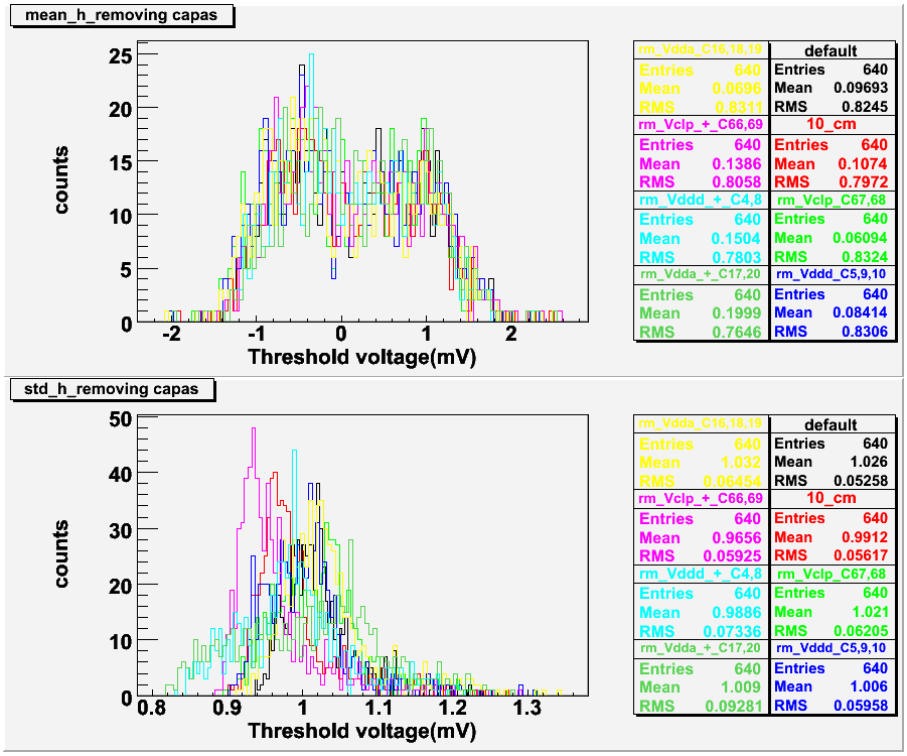


Figure 26 Detailed results of the study of the discriminator transfer function with different number of 100 nF decoupling capacitors surrounding the Pahse-1 prototype. The upper and lower plots represent offset and noise distribution, respectively.

Table 7 ^{55}Fe calibration results for Phase-1 prototype with removed 10 uF decoupling capacitors.

Set	Pedestal	Noise	Peak	Peak sigma	**ENC**
10 uF capas 10 cm away	2.90 (0.80 RMS)	2.46 (0,55 RMS)	299.6	9.42	**13.4**
C51 (VDDD) removed	2.73 (0.83 RMS)	2.44 (0.55 RMS)	299.7	9.53	**13.3**
C51 (VDDD), C50 (VDDA) removed	3.18 (0.87 RMS)	2.46 (0.55 RMS)	298.6	9.48	**13.5**
C50 (VDDA) removed	3.15 (0.85 RMS)	2.46 (0.55 RMS)	298.8	9.49	**13.5**

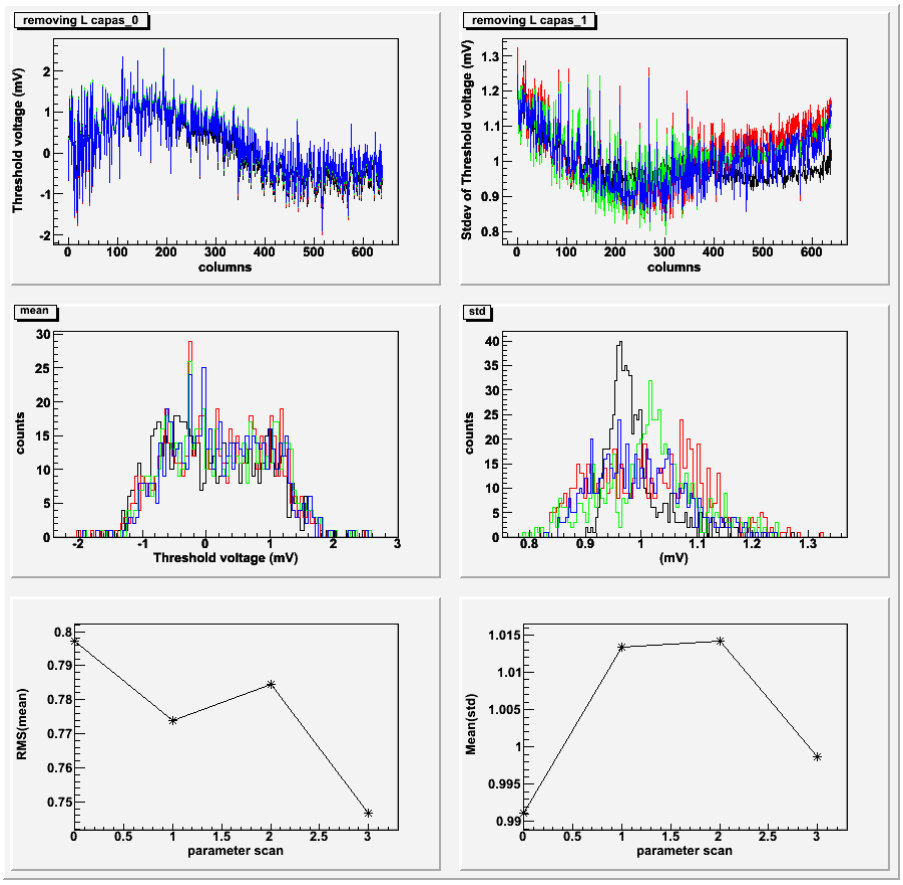


Figure 27 Discriminator transfer function measured in different configurations of 10 µF decoupling capacitors on the VDDD and VDDA lines. Parameter scan points correspond to the configuration with both decoupling capacitors present, VDDD decupling capacitor removed, both VDDA and VDDD decoupling capacitors removed, and only VDDA capacitor removed.

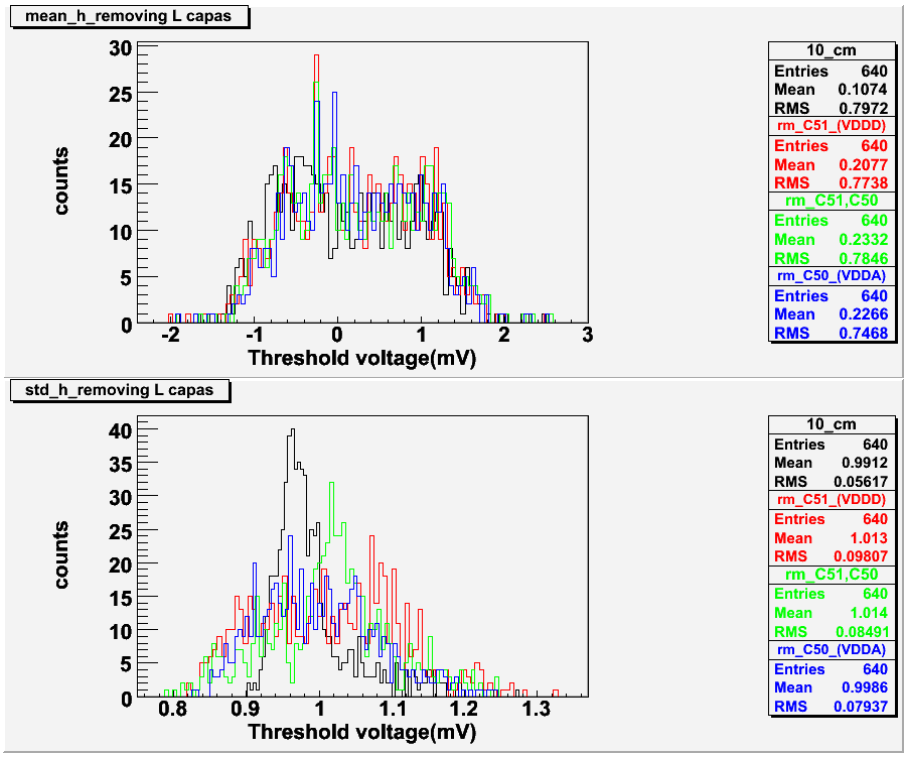


Figure 28 Detailed results of the study of the discriminator transfer function with 10 µF decoupling capacitors removed from the vicinity of the Pahse-1 prototype. The upper and lower plots represent offset and noise distribution, respectively.