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February 5, 2010

Phase-1 and Phase-2 Sensor Testing at IPHC, Nov. 2009

- **Setup and initial testing**
- **Discriminator transfer functions in test mode**
- **Phase-2 performance**
- **Phase-2 vs. Phase-1**
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Setup and initial testing

The goal for the tests at IPHC was to confirm and further investigate dispersion observed in threshold values of discriminators in Phase-1 prototypes tested at LBL. This dispersion manifested itself in a spatial distribution with a distinct pattern across the sensor width.

Available testing equipment allowed us to utilize test cards fabricated and assembled at LBL and to interface them to the IPHC readout system. The IPHC readout system that was used in these tests reads the 16 parallel CMOS outputs of Phase-1 but does not provide capability for reading 160 MHz LVDS signals. In a parallel testing setup, we run a full LBL test bench comprising readout system and test cards operated at 160 MHz. The LBL readout system is optimized for sensor operation in a multi-chip detector setup and supports the fast LVDS data path, without having the interface arrangement to allow for reading out the CMOS outputs.

To cross-connect LBL test cards with IPHC readout system we used available generic IPHC-designed LVDS<->CMOS translator cards that provided logic conversion for up to 16 channels each. We used two of these cards to provide full conversion for all JTAG, control and monitoring signals, and 16 CMOS Phase-1 outputs.

Following the IPHC testing procedures, we started tests with a detailed study of on-chip discriminators in their test mode readout. In this readout, pixels are not connected to discriminators. Instead, pixel signals are emulated by internally generated and configurable reference voltages.

In the LBL test bench, we focused on testing Phase-2 prototypes using the same procedures as for Phase-1 prototypes previously tested at LBL. Phase-2 was fabricated based on the Phase-1 design with minor mask changes to address the discriminator threshold dispersion issues.

A set of measurements gave us confidence that the IPHC parallel CMOS readout was fully functionally equivalent to the LBL LVDS readout.

This write-up addresses two aspects of the tests performed:

1. a brief description of test results obtained in the discriminator test mode readout
2. Phase-2 tests and performance comparison between the Phase-1 and Phase-2 prototypes.

Selecting DAC step for discriminator threshold scans

When we first started testing sensors, we realized that our groups had differently optimized the speed of data acquisition by using different step sizes and ranges for scanned thresholds.

We have performed sets of measurements with different DAC steps used in threshold scans to measure the influence of the step size on test results. A comparison between DAC steps of 1 and 2 is presented in Figure 1. The results are the same within precision better than 3%. We have also verified that with the DAC step of 5 the results are within 10% from results obtained with the step of 1 DAC unit.

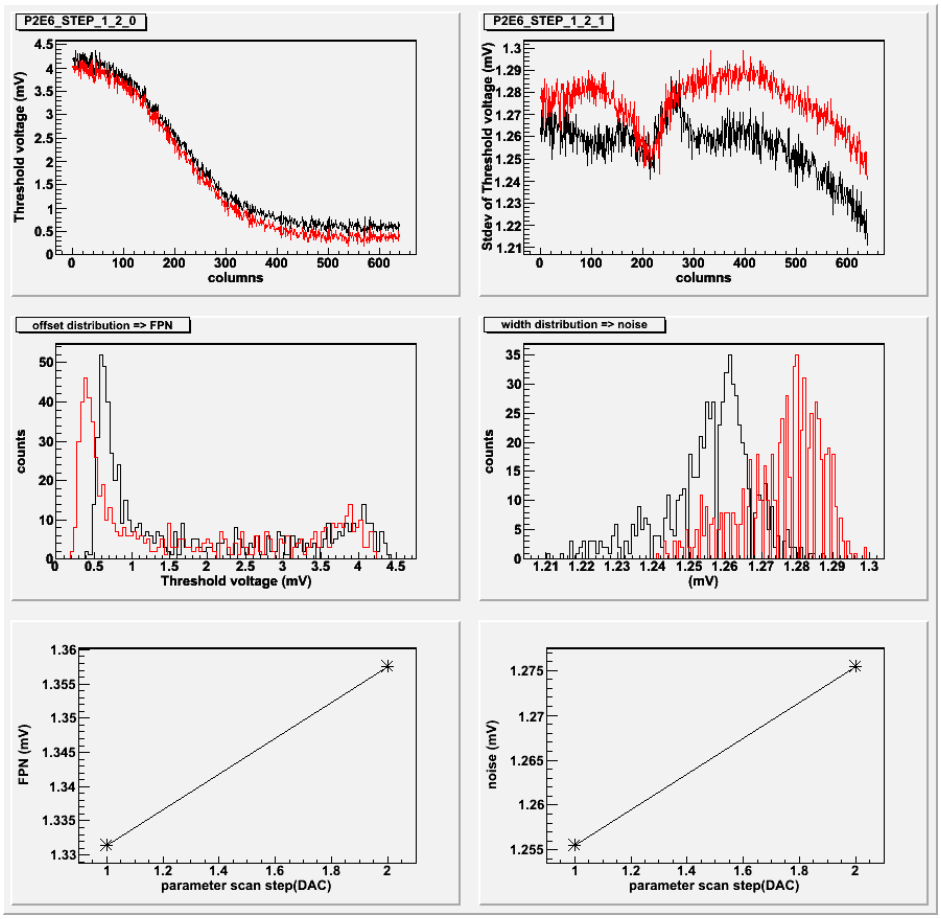


Figure 1 Discriminator transfer function measured for DAC step of 1 and 2. The values of extracted FPN and temporal noise agree with precision better than 3%.

In addition to the scan step size, we have verified that the typically used data sample of 10 frames per scan point is sufficient and increasing the amount of data to 100 frames has no influence on the measured FPN and temporal noise. Two sets of scans acquired with 10 and 100 frames are presented in Appendix B Figure 18 and Figure 19, respectively. The measured FPN and temporal noise values are the same with a better than 4% accuracy.

Most of the results presented further in this write-up are based on threshold scans performed with the DAC step of 2 and 10 frames per scan point.

Discriminator transfer function in test mode readout

Initial set of tests performed at IPHC focused on discriminators in the test mode. In this testing mode the variation of discriminator threshold voltages is significantly increased compared to when pixels are readout. This is summarized in
Table 1 on an example of Phase-1 (D1) and Phase-2 (P2E6) prototypes with data analyzed for all rows of pixels. The magnitude of the dispersion is presented in Figure 19 and Figure 20 in Appendix B and can be easily compared with other plots that represent standard readout mode.

Initial test results in the discriminator test mode indicated a factor of two differences in FPN and temporal noise values measured by IPHC and LBL readout systems. We tried to determine if it was related to different numbers of frames processed or different DAC steps used in our scans or the fact that different types of outputs were used (LVDS vs. CMOS). After proving that none of the above differences could affect our results, we studied our analysis algorithms and found differences that explain the observed dependencies. These differences are explained next.

Even and odd rows

The default IPHC analysis of discriminator threshold voltages processed tens of frames but looked only at a single row of pixels. This is in contrast to the LBL analysis procedure where we sum pixels above threshold in each pixel column for ten frames, which gives us 6400 samples for our discriminator threshold analysis.

We have decided to look at even and odd rows separately, and the results of this analysis are summarized in
Table 1. There is a significant difference in measured noise when the chip is tested in the discriminator test mode. However, it needs to be noted that when the chip is in full operation mode – reading out pixels – we do not observe any row-dependent dispersions. At the present state of our knowledge, we do not have an explanation for the observed effect in the discriminator test mode.

Table 1 FPN and temporal noise measured on Phase-1 chip D1 and Phase-2 chip E6 in the discriminator test mode and with full pixel array readout. In addition to the "full-array" analysis, results are presented for odd and even rows separately.

	FPN			**Temporal noise**		
rows	all	even	odd	all	even	odd
D1 discri test	4.90	4.88	4.94	0.84	0.44	0.46
P2E6 discri test	1.09	1.07	1.08	1.10	0.39	0.41
D1 pixels (LBL)	1.50	1.51	1.64	1.71	1.71	1.63
opt	1.25	1.24	1.25	1.47	1.45	1.47
P2E6 pixels	0.85	0.79	0.78	0.82	0.82	0.82

IPHC test using discriminator test mode

Additional comparison of performance of Phase-1 (D1) and Phase-2 (E6) prototypes read out in the discriminator test mode is summarized in Table 2. FPN in Phase-2 chip E6 is only 25% of that in Phase-1 D1.

As we know from Phase-1 tests performed at LBL, the magnitude of the FPN dispersion can be minimized by adjusting ICLPDISC setting in Phase-1.

It needs to be highlighted here that FPN was reduced by 40% when the ICLPDISC value was decreased from 95 to 20 for D1 and from 86 to 11 for E6.

Table 2 FPN and temporal noise measured on Phase-1 chip D1 and Phase-2 chip E6 in the discriminator test mode and with full pixel array readout.

	FPN	**Temporal noise**
D1 test	5.40	0.50
P2E6 test	1.36	0.47
D1 opt	3.38	0.48
P2E6 opt	0.84	0.38

Table 2 shows the estimated values of FPN and temporal noise. The graphical representation of this dispersion is shown in Appendix C. The values of VRef2 and VClpdisc for D1 and E6 were selected to provide the same voltage measured on the corresponding test pads. The results are shown for close to default settings (as per the Phase-1 user manual) and with settings optimized to some extent (low value of ICLPDISC).

Phase-2 performance

"0"-threshold measurements

The threshold range for different Phase-2 prototypes was tested using the IPHC automated testing procedure for testing VREF1 and VREF2. The results limited to the DAC value that corresponds to discriminator threshold equal to zero are summarized in Table 3. These results indicate a quite significant chip-to-chip dispersion of this parameter. This is in agreement with Phase-1 measurements (full range from 100 to 170 DAC).

Table 3 JTAG settings for obtaining discriminator threshold values of zero in Phase2 chips A2, C2, G2, E6.

Phase-2 chip	VREF2-VREF1=0 (DAC)
A2	190
C2	170
G2	105
E6	98

Threshold voltage parameter scans

The following sets of plots summarize the Phase-2 performance in terms of FPN and temporal noise. The tests were performed in the standard readout mode – with pixel signals readout through discriminators.

The dependency of the threshold voltage dispersion is presented as a function of one of the following parameters:

- ICLPDISC
- VREF2
- IBUFBIAS

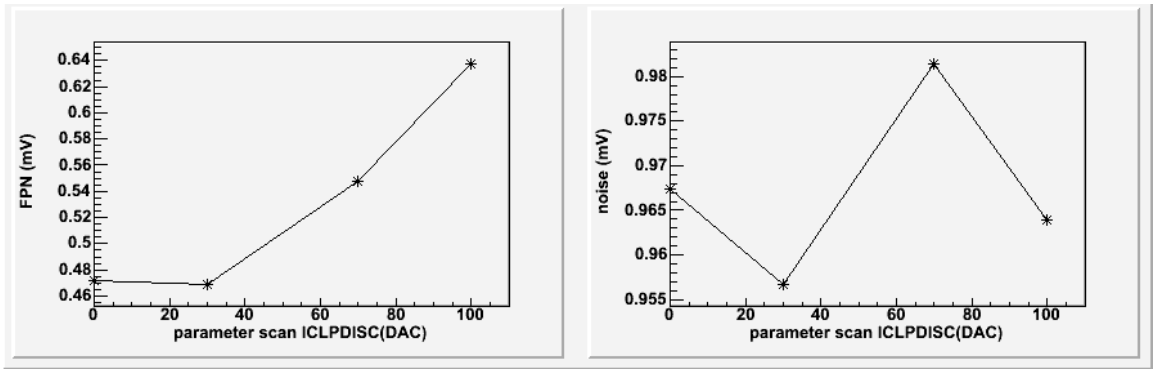
The JTAG settings used in these tests are listed in Appendix D and in Table 4. The default settings in Table 4 define the starting point for each scan.

Table 4 The default JTAG settings for measuring discriminator threshold voltages in Phase2 sensors A2, C2, G2, E6.

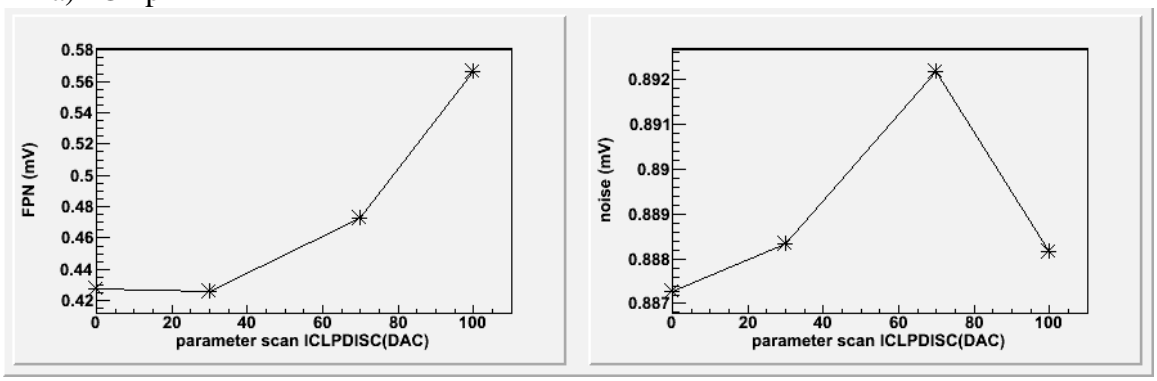
Phase-2	VREF2	IBUFBIAS	ICLPDISC
A2	85	10	30
C2	80	10	30
E6	80	10	30
G2	83	10	90

The plots in this section summarize measurements. Full sets of plots, including shape of transfer curves and distribution of FPN and temporal noise are presented in Appendix A.

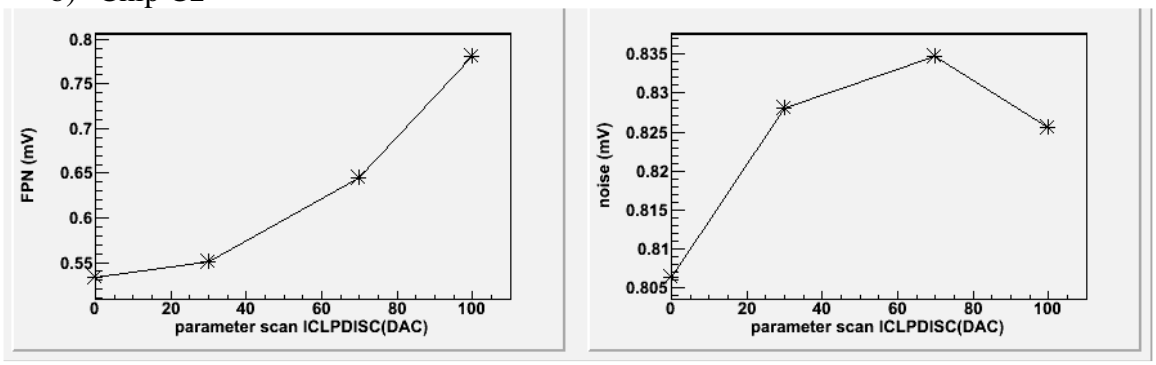
ICLPDISC scan



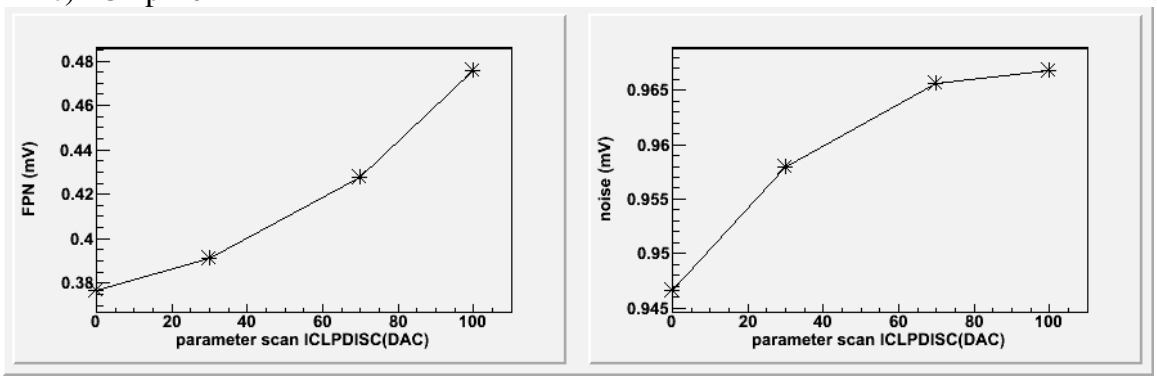
a) Chip A2



b) Chip C2



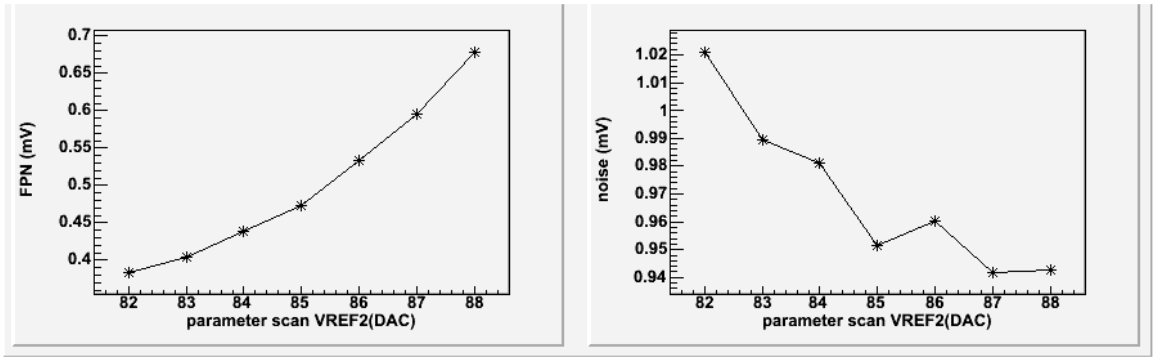
c) Chip E6



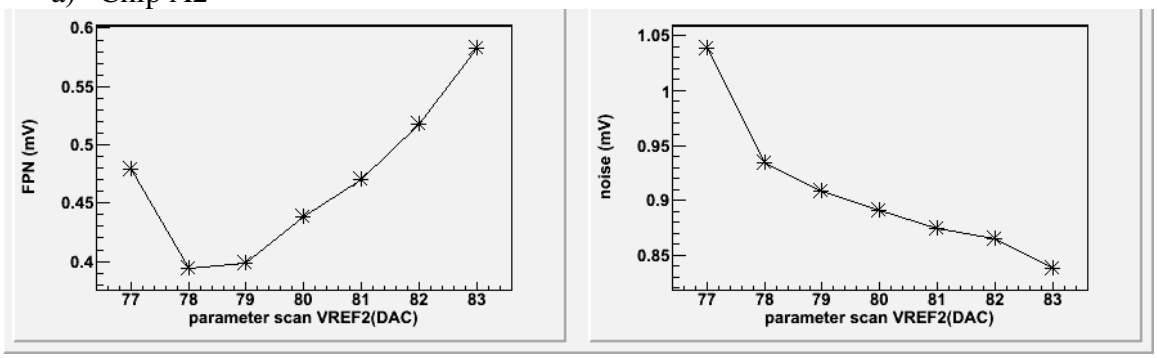
d) Chip G2

Figure 2 FPN and temporal noise extracted from discriminator transfer function scans. The scans were performed at ICLPDISC values of 0, 30, 70, 100 DAC units. The other JTAG settings are listed in Appendix D and in Table 4.

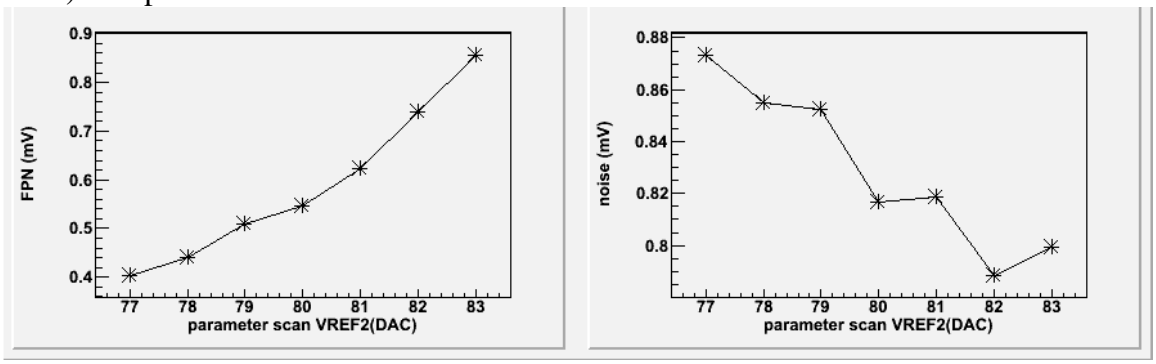
VREEF2 scan



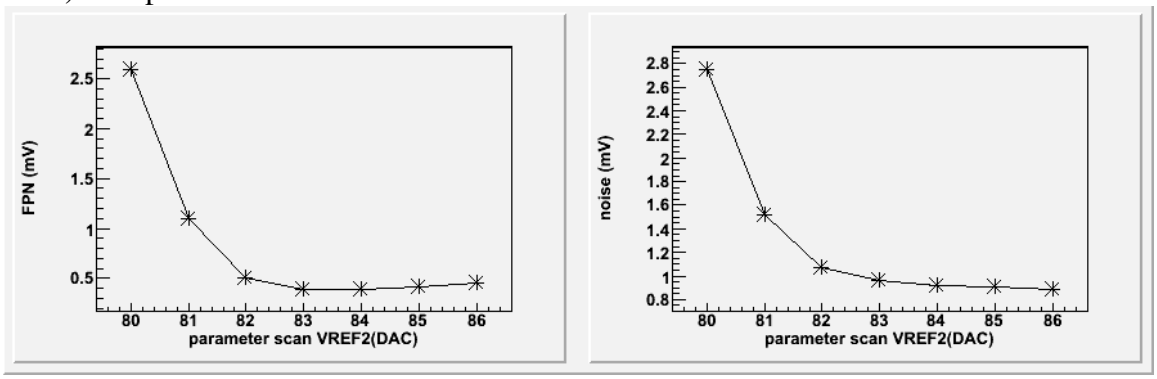
a) Chip A2



b) Chip C2



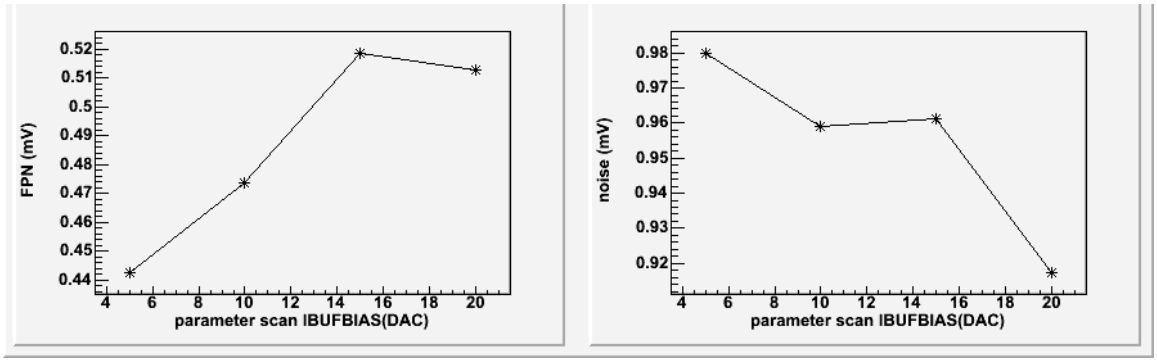
c) Chip E6



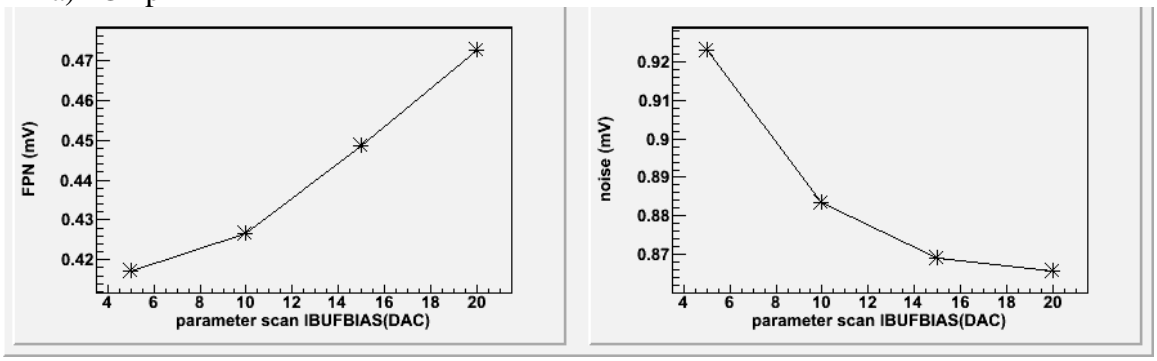
d) Chip G2

Figure 3 FPN and temporal noise extracted from discriminator transfer function scans. The scans were performed at various VREF2 ranges selected independently for each of the sensors. The other JTAG settings are listed in Appendix D and in Table 4.

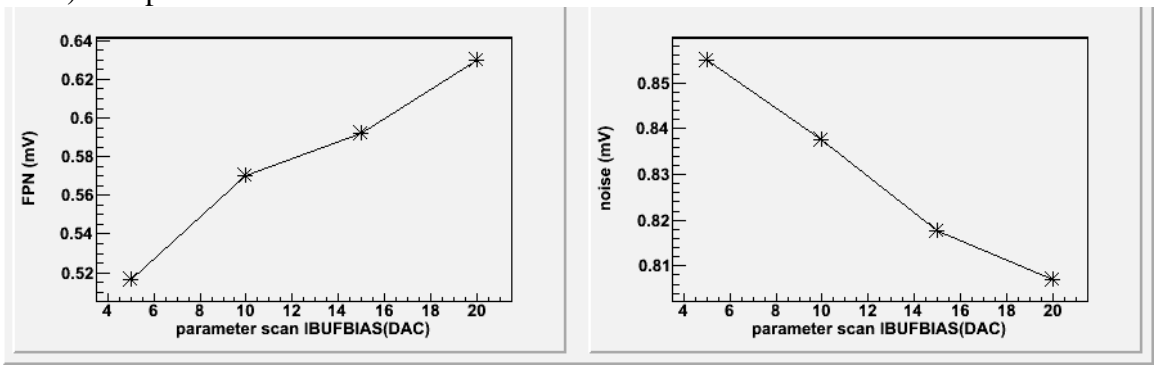
IBUFBIAS scan



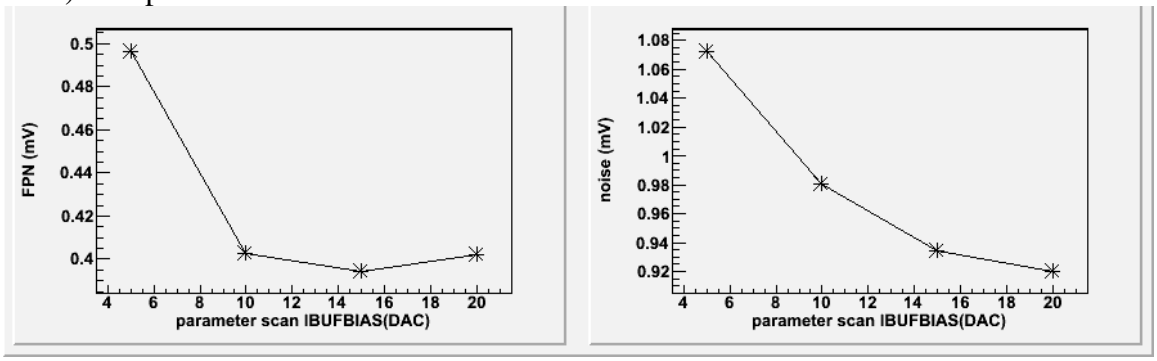
a) Chip A2



b) Chip C2



c) Chip E6



d) Chip G2

Figure 4 FPN and temporal noise extracted from discriminator transfer function scans. The scans were performed at IBUFBIAS values of 5, 10, 15 and 20 DAC units. The other JTAG settings are listed in Appendix D and in Table 4.

Bias check

Voltages that correspond to particular JTAG settings are summarized in Table 5 for ICLPDISC and in Table 6 for VREF2. The dispersion between sensors can be as large as 100 mV.

Bold numbers in Table 6 indicate settings that can be considered optimal based on the scan results presented above. In case of chips A2 and E6, additional data points at lower VREF2 settings would be needed to correctly asses optimum settings for each of these sensors.

Table 5 Bias voltages for different ICLPDISC settings in the tested Phase-2 prototypes.

IbufBias=10	G2	A2	C2	E6
ICLPDISC(0)	1.175	1.183	1.177	1.179
ICLPDISC(30)	1.446	1.463	1.449	1.483
ICLPDISC(70)	1.802	1.827	1.811	1.880
ICLPDISC(100)	2.065	2.098	2.079	2.174

Table 6 Bias voltages for different VREF2 settings in the tested Phase-2 prototypes.

IbufBias=10	G2	A2	C2	E6
VREF2(77)			0.841	**0.850**
VREF2(78)			**0.852**	0.861
VREF2(79)			0.863	0.872
VREF2(80)	0.821		0.873	0.883
VREF2(81)	0.832		0.884	0.894
VREF2(82)	0.842	**0.851**	0.894	0.905
VREF2(83)	0.852	0.861	0.905	0.916
VREF2(84)	**0.862**	0.871		
VREF2(85)	0.872	0.881		
VREF2(86)	0.882	0.892		
VREF2(87)		0.902		
VREF2(88)		0.912		

^{55}Fe calibrations

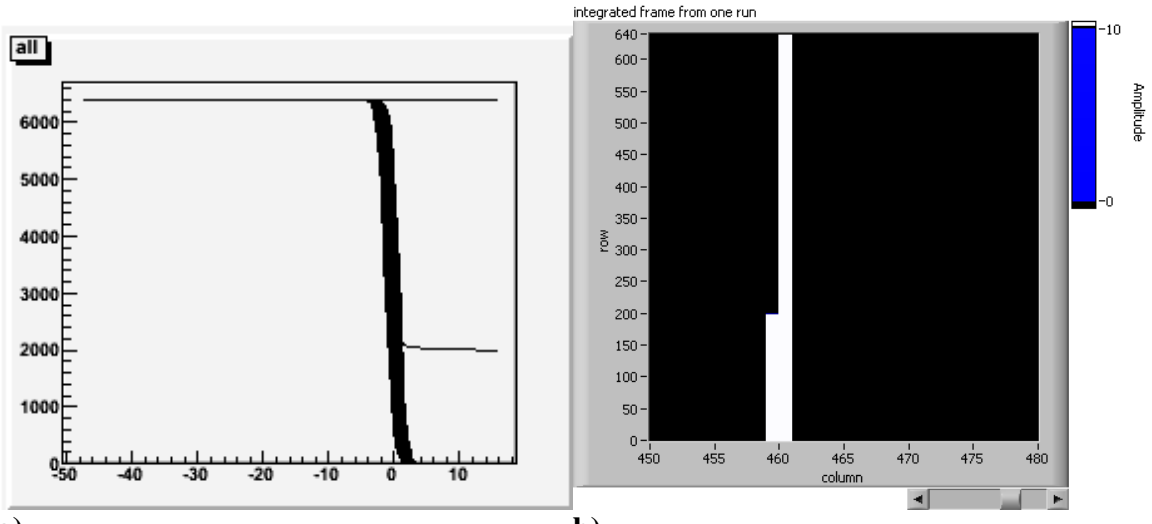
A set of ^{55}Fe calibrations was performed on the four available Phase-2 prototypes. The results are summarized in Table 7. The equivalent noise charge (ENC) measured for Phase-2 is at **14.0± 0.2** electrons. It is, as expected, in very close agreement to Phase-1 measurements.

Table 7 ^{55}Fe calibration results for Phase2 chips A2, C2, G2, and E6.

Chip	Pedestal (ADC)	Noise (ADC)	Peak (ADC)	Peak sigma (ADC)	**ENC (electrons)**
A2	3.23 (0.84 RMS)	2.5	295	9.7	**13.9**
C2	3.1 (0.72 RMS)	2.4	294	9.0	**13.4**
G2	1.36 (0.67 RMS)	2.6	300	8.4	**14.2**
E6	2.7 (0.73 RMS)	2.4	285	8.5	**13.8**

A2- faulty pixels

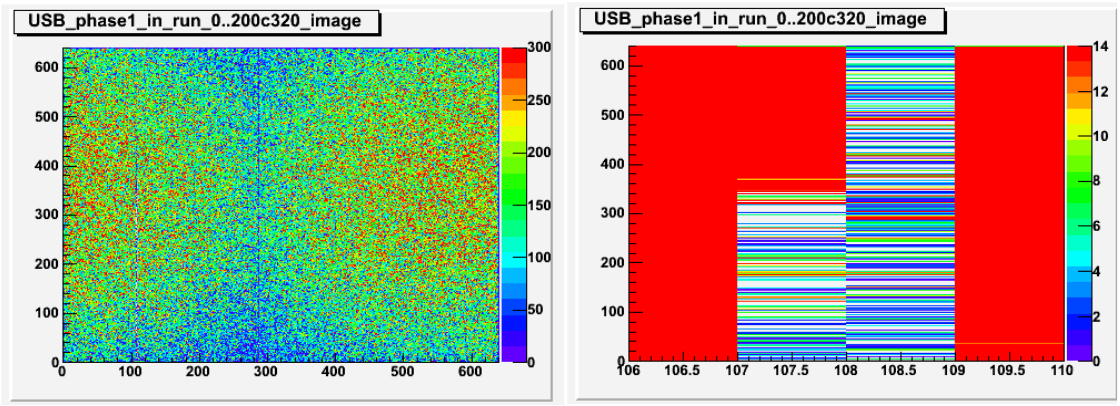
In the chip A2 some faulty pixels have been observed. This is the first and so far the only sensor in the tested batch of 9 Phase-1 prototypes and 4 Phase-2 prototypes that exhibited such flaws. The first indication of chip defects was observed in the plot of all 640 measured transfer functions. Two columns of pixels do not switch to "0" even for the highest threshold values applied. In one column, signals from all pixels stay above threshold. In the second column, only part of the pixels shows this behavior. This is presented as transfer functions in Figure 5 (a) and a 2D image of the faulty section in Figure 5 (b).



a) **b)**

Figure 5 (a) All 640 discriminator transfer functions measured with Chip A2. Two of the transfer curves show anomalous behavior i.e. even at high discriminator thresholds some pixels signals still pass the discriminator threshold. (b) Corresponding 2-D view zoomed to the faulty pixel columns.

It is difficult to distinguish between faulty pixels and discriminators from the above result. However, analog output tests – ^{55}Fe calibrations – can provide additional information. Similar special behavior is observed in analog readout. An integrated image of the signals from a ^{55}Fe source is presented in Figure 6 (a). The image of the source is split into two sections indicating that there is a misalignment of the frame boundaries in the acquisition system. This is caused by the fact that in our readout system we use the chip's digital readout marker to synchronize the analog readout. The implementation of this approach is apparently flawed and doesn't guarantee the correct synchronization to the first 8-column section in the readout data stream. This however is not a problem in this calibration analysis, which is based on signals from single pixels.

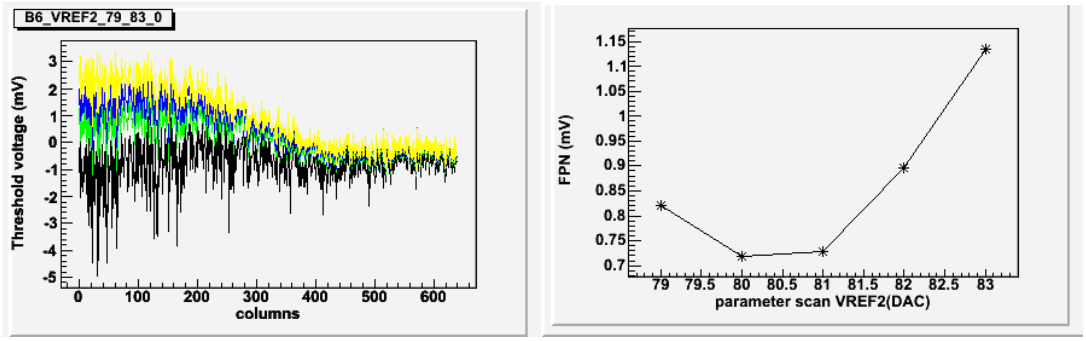


a) **b)**

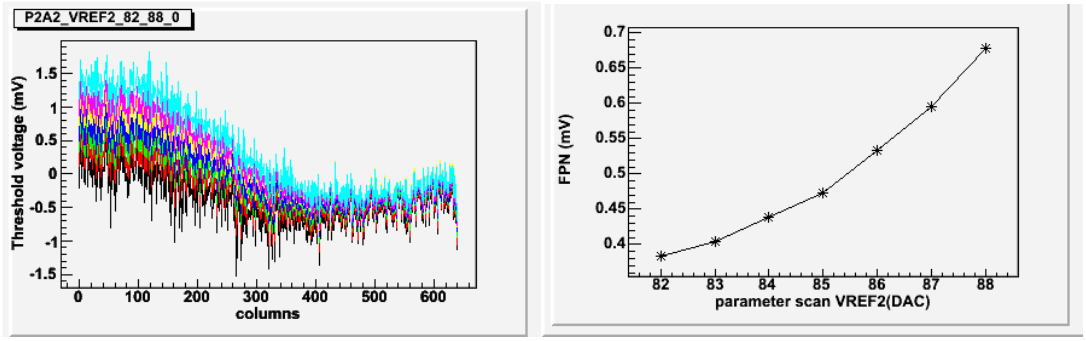
Figure 6 (a) integrated image from the ^{55}Fe calibration of chip A2. The image of the source is split into two sections indicating that there is a misalignment of the frame boundaries in the acquisition system. (b) Closer look at the affected columns.

The frame boundary in analog readout is at column 287 and the inefficient column is 108. When corrected for the frame misalignment, the faulty columns are 459 and 460.
The location of faulty columns is consistent between the digital readout (discriminator threshold scan) and analog readout (^{55}Fe calibrations).

Phase-2 vs. Phase-1

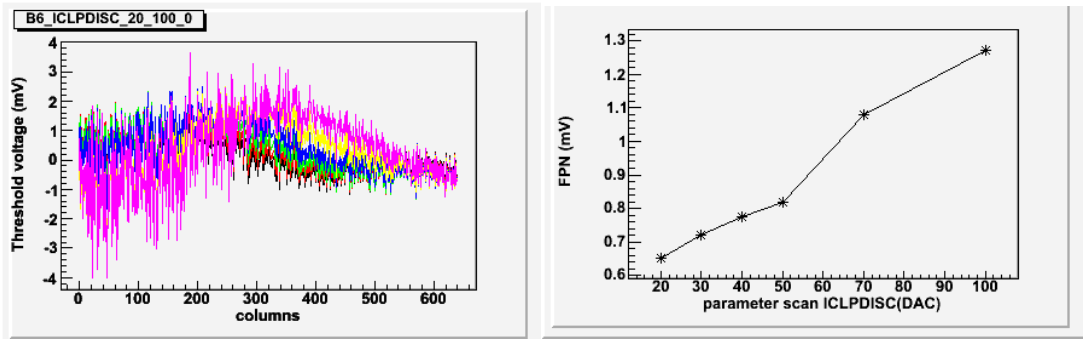


a)

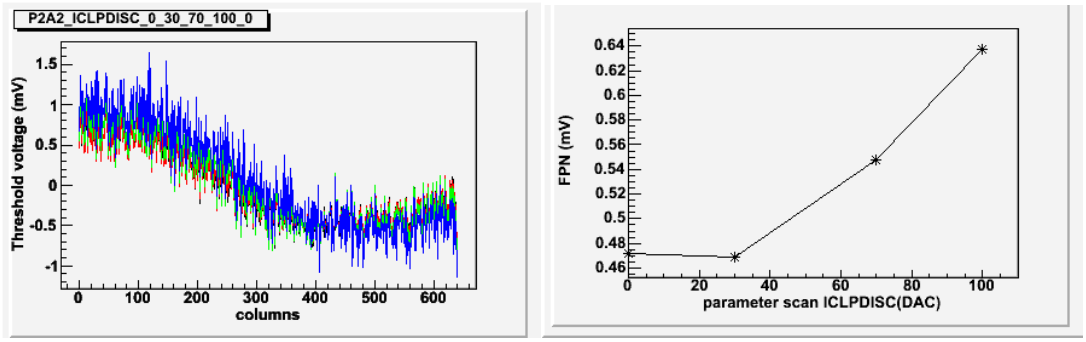


b)

Figure 7 Comparison of FPN measured at different VREF2 values for Phase-1 chip B6 (a) and Phase-2 chip A2 (b). Note different ranges of VREF2 used in these tests. In Phase-2, the magnitude of discriminator threshold variations is smaller than in Phase-1.



a)



b)

Figure 8 Comparison of FPN measured at different ICLPDISC values for Phase-1 chip B6 (a) and Phase-2 chip A2 (b). The impact of the ICLPDISC settings on the discriminator threshold distribution is less pronounced in Phase-2.

Figure 7 and Figure 8 show a side-by-side comparison of discriminator threshold scans in selected Phase-1 and Phase-2 prototypes.
Threshold voltage scan as a function of VREF2, presented in Figure 7, clearly indicates that in Phase-2 the magnitude of discriminator threshold variation is smaller than in Phase-1.
Similarly, the impact of the ICLPDISC settings on the discriminator threshold distribution is less pronounced in the case of Phase-2 (Figure 8).

Summary and conclusions

It appears that optimization of the Phase-2 performance requires careful adjustment of VREF2 settings to a value as low as possible without degrading the chip performance. Phase-2 sensors tested with optimized settings show FPN and temporal noise values summarized in
Table 8.

Table 8 FPN and temporal noise measured on Phase-2 sensors.

Chip	FPN	Temporal noise
A2	0.47	0.96
C2	0.43	0.88
G2	0.38	0.95
E6	0.55	0.82

*Chip G2 was tested at ICLPDISC = 90 DAC units and additional tests are required to confirm that it is beneficial to run at lower ICLPDISC settings.

These parameter values are extracted from measurements presented in section *Threshold voltage parameter scans.* The FPN value is approximately half of the value of temporal noise. This is a clear improvement over the Phase-1 performance.

The Phase-1 performance tested on several chips[1] demonstrated FPN ranging from 0.6 mV to 1 mV and temporal noise estimated at 1-1.2 mV.

In parallel to the tests of Phase-1 and Phase-2, the chip designers made progress in device simulations. It has been shown that the threshold dispersion effect can be reproduced in circuit simulations. Understanding of the origin of this effect should allow for further reduction of FPN in new prototypes. Description of the source of the measured threshold dispersion is beyond the scope of this write up and will be addressed elsewhere.

[1] http://rnc.lbl.gov/hft/hardware/docs/Phase1/Phase1_test_summary(bias,capas).pdf

Appendix A

Explanation of the plot layout and color scheme used in plots

The layout of the figures in this section is following:

Mean value of Gaussian fit to discriminator transfer functions plotted as column number	**Standard deviation** of Gaussian fit to discriminator transfer functions plotted as column number
Histogram of mean values	Histogram of standard deviation values
RMS values of mean values distribution as a function of the scan parameter number	**Mean** values of standard deviation distribution as a function of the scan parameter number

The color scheme used in plots:

Discriminator transfer functions

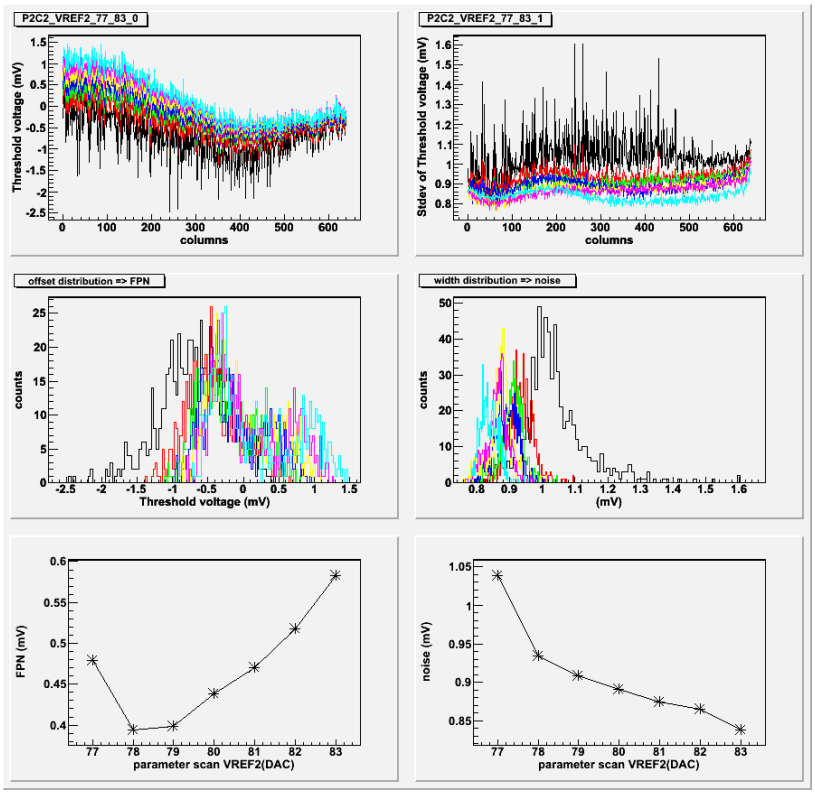


Figure 9 Chip C2; VREF2 scan from 77 to 83 DAC counts.

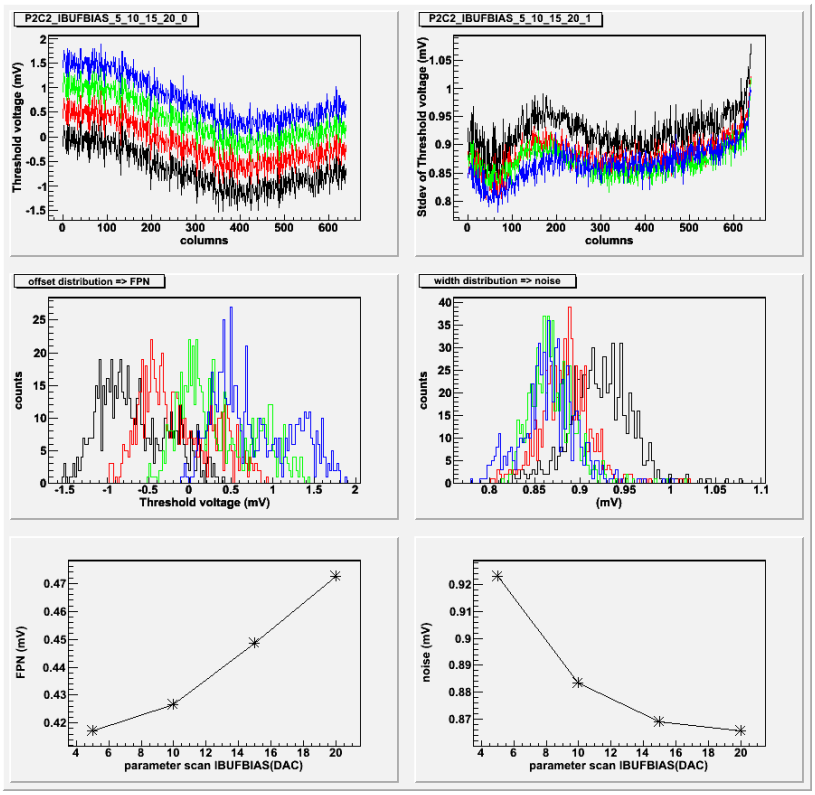


Figure 10 Chip C2; IBUFBIAS scan at 5, 10, 15, 20 DAC counts.

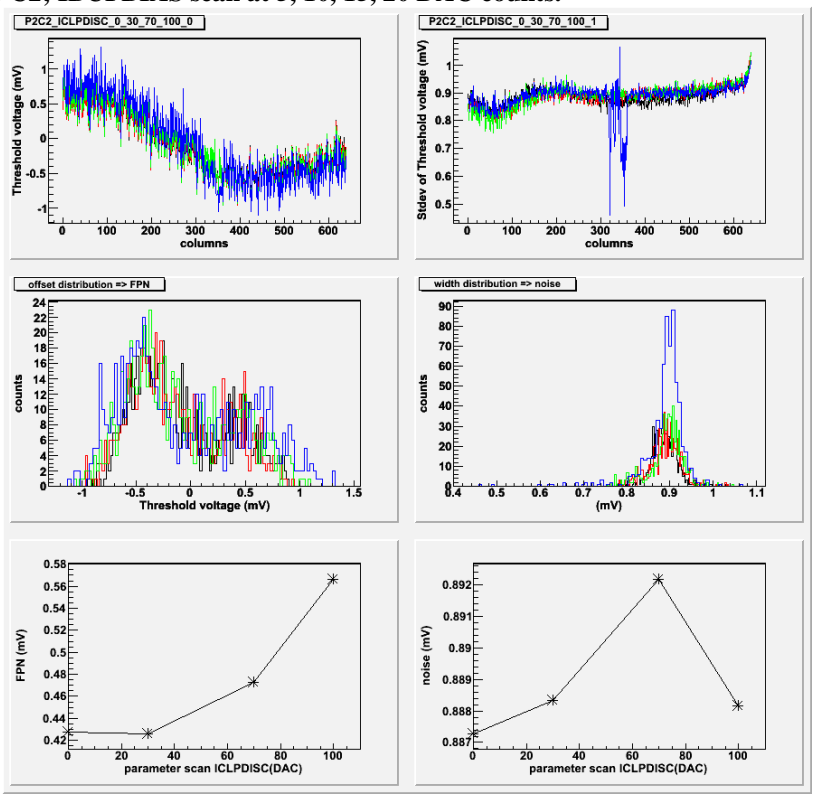


Figure 11 Chip C2; ICLPDISC scan at 0, 30, 70, 100 DAC counts.

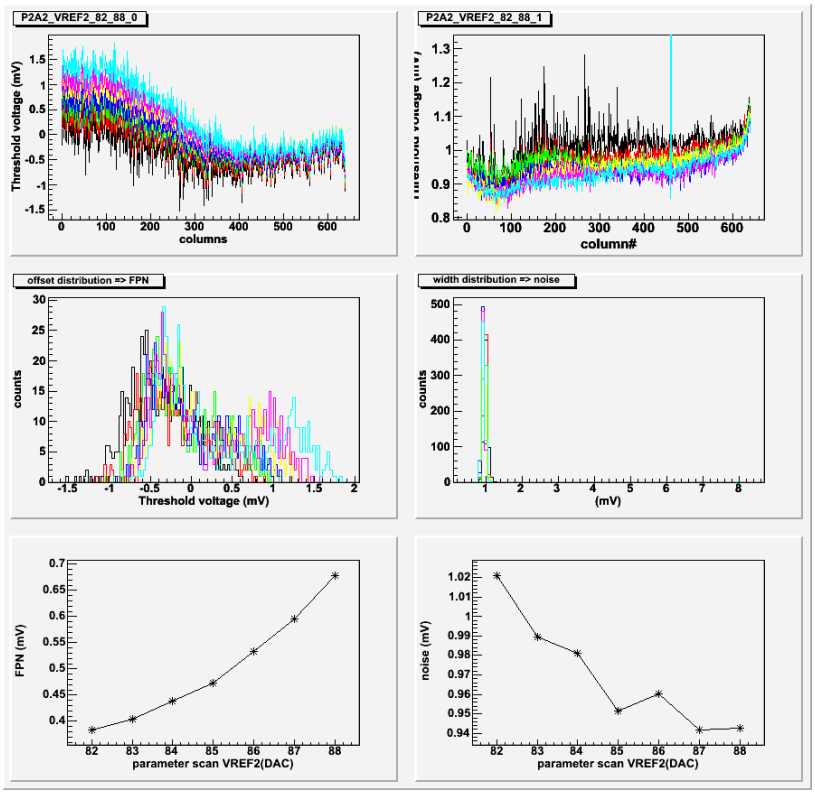


Figure 12 Chip A2; VREF2 scan from 82 to 88 DAC counts.

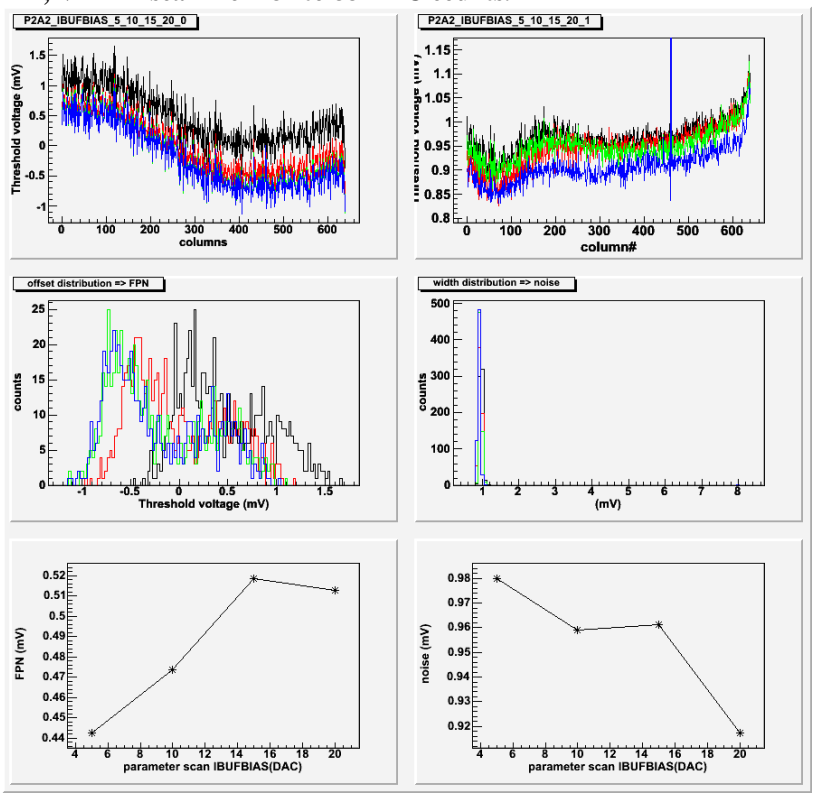


Figure 13 Chip A2; IBUFBIAS scan at 5, 10, 15, 20 DAC counts.

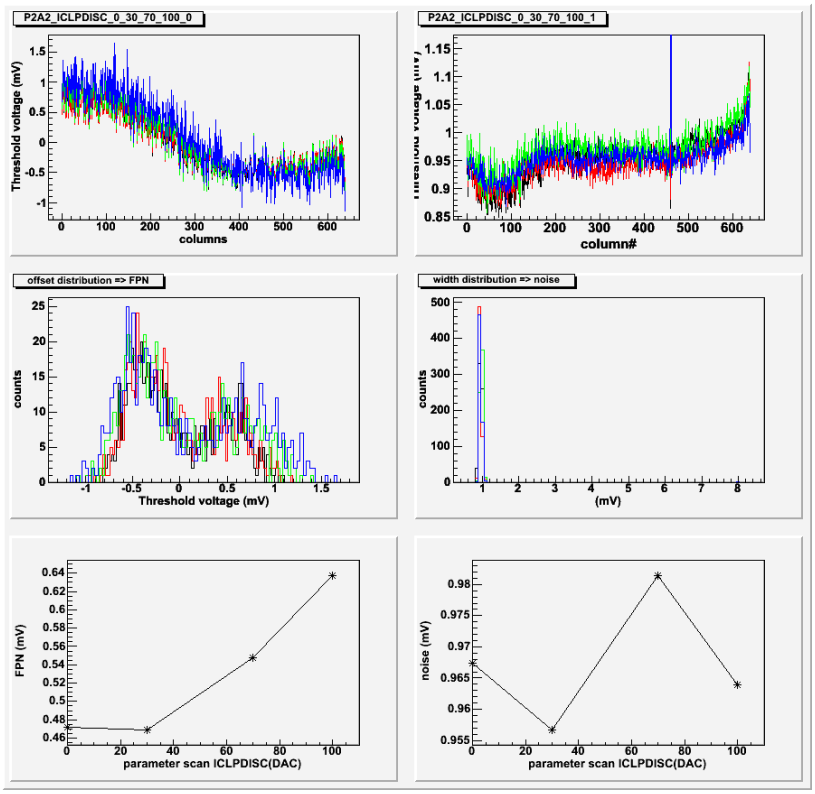


Figure 14 Chip A2; ICLPDISC scan at 0, 30, 70, 100 DAC counts.

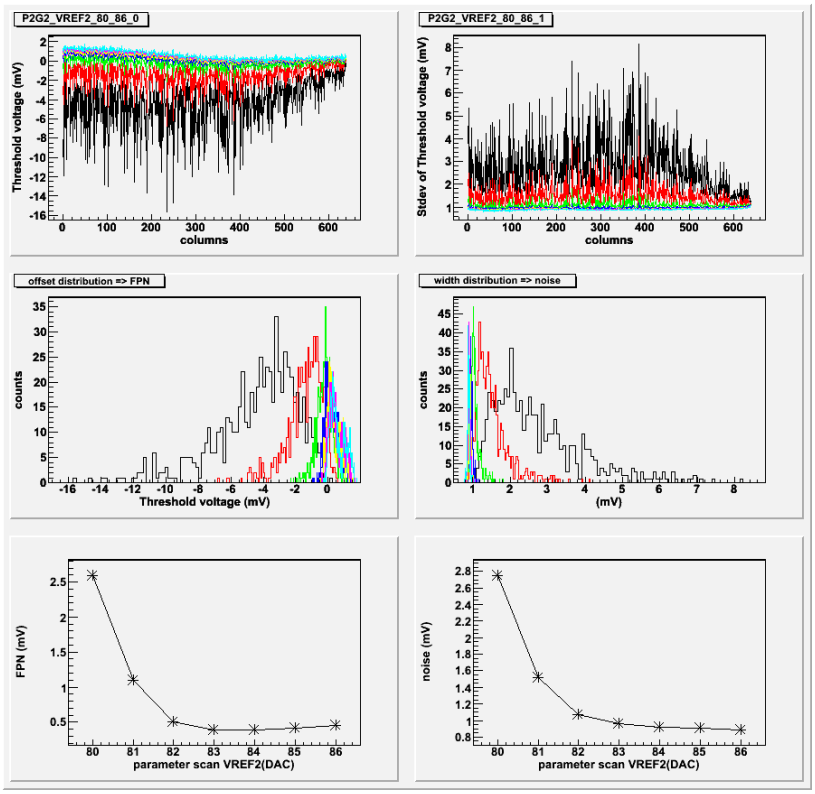


Figure 15 Chip G2; VREF2 scan from 80 to 86 DAC counts.

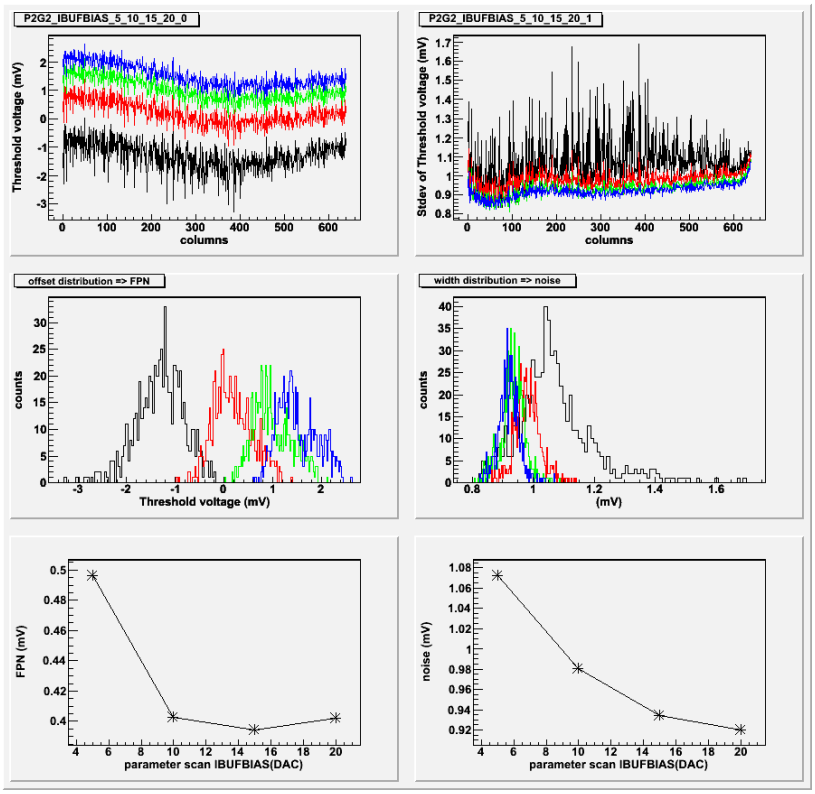


Figure 16 Chip G2; IBUFBIAS scan at 5, 10, 15, 20 DAC counts.

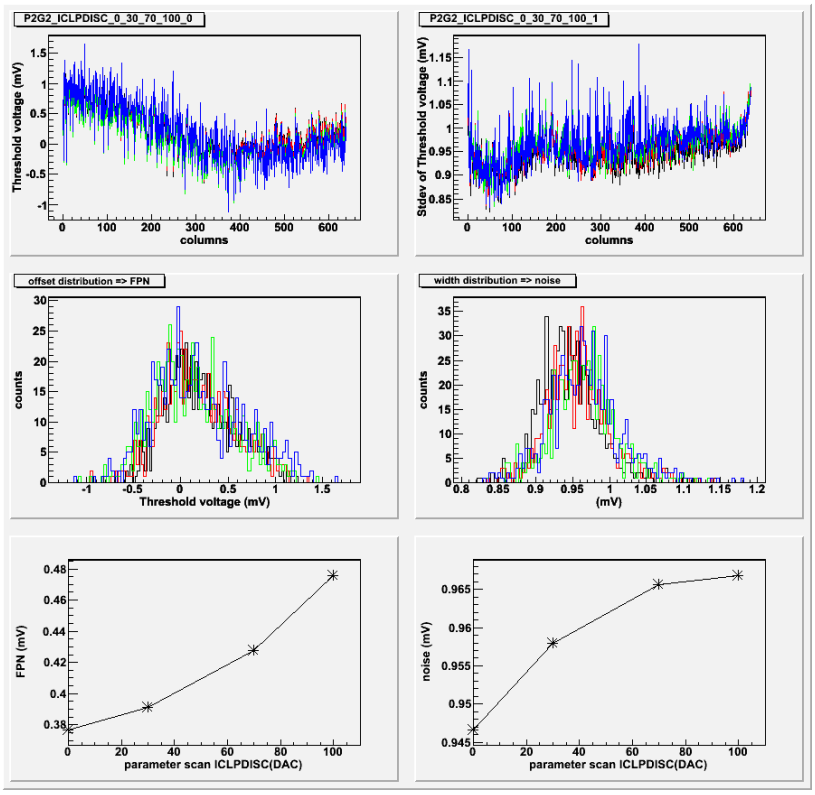


Figure 17 Chip G2; ICLPDISC scan at 0, 30, 70, 100 DAC counts.

Appendix B

Phase-2 performance as a function of different sample size

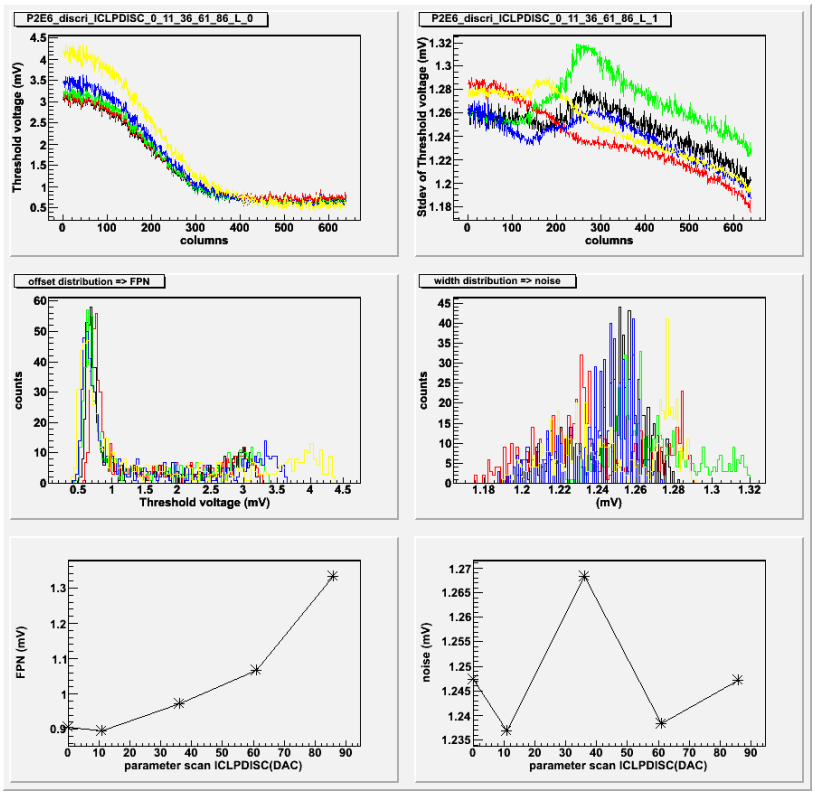


Figure 18 A set of discriminator threshold scans in the discriminator test mode. ICLPDISC was set to 0, 11, 36, 61, 86 and 100 frames were acquired for each scan point.

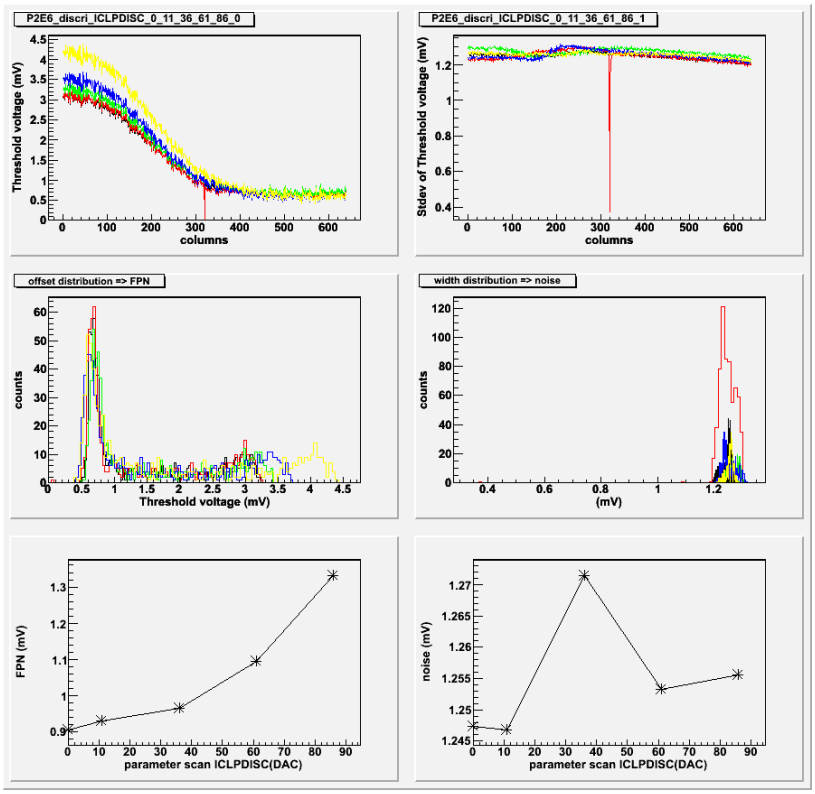


Figure 19 A set of discriminator threshold scans in the discriminator test mode. ICLPDISC was set to 0, 11, 36, 61, 86 and 10 frames were acquired for each scan point.

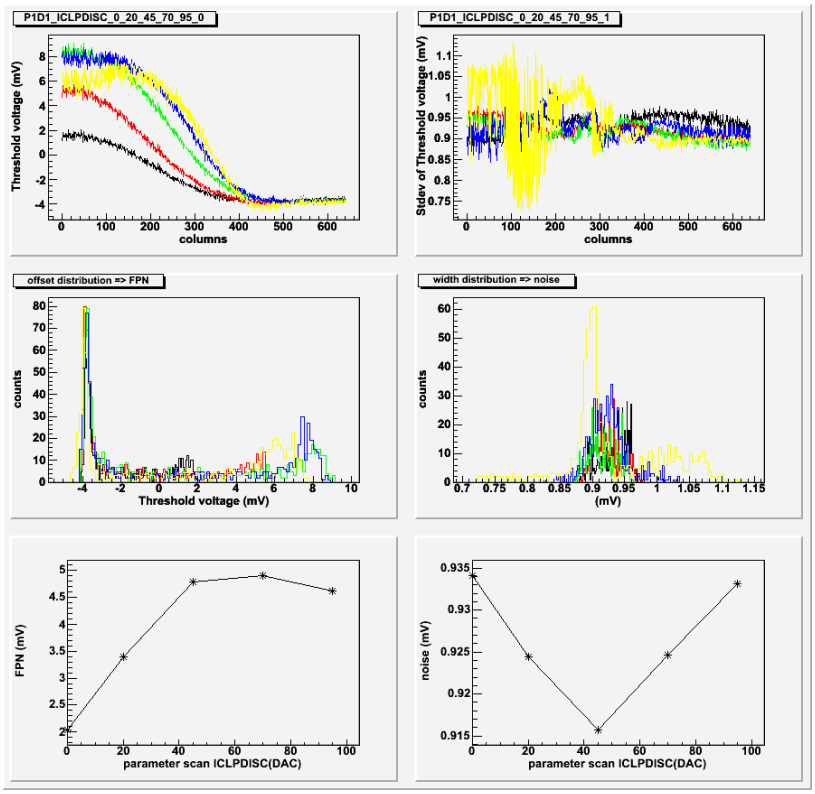
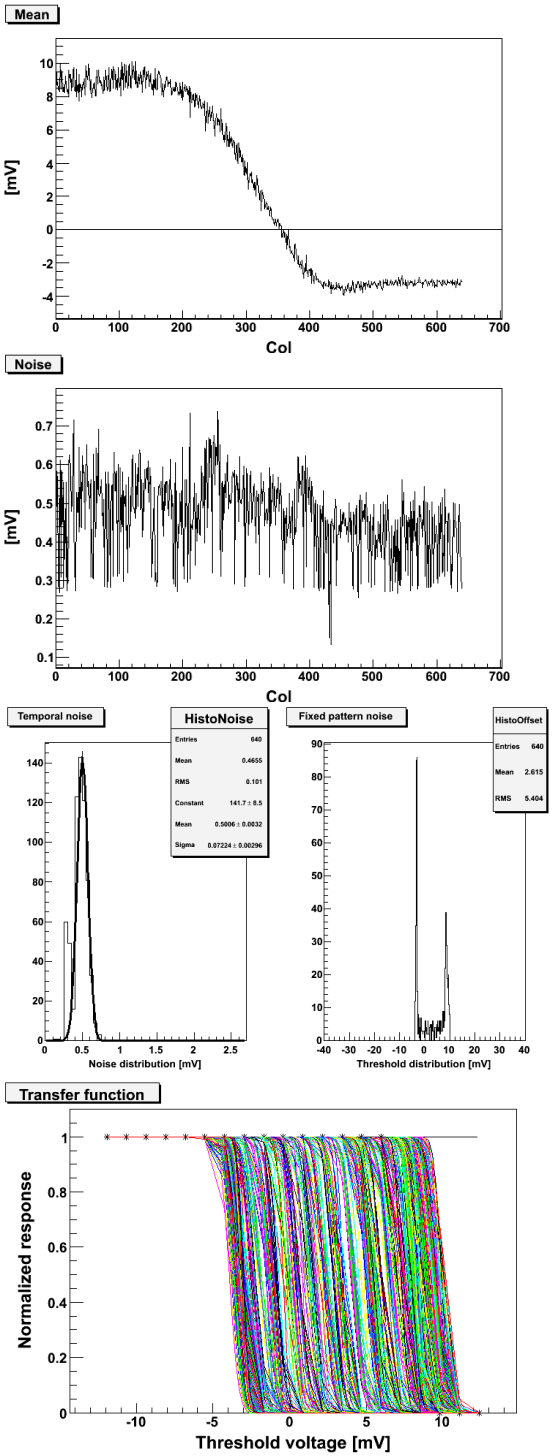


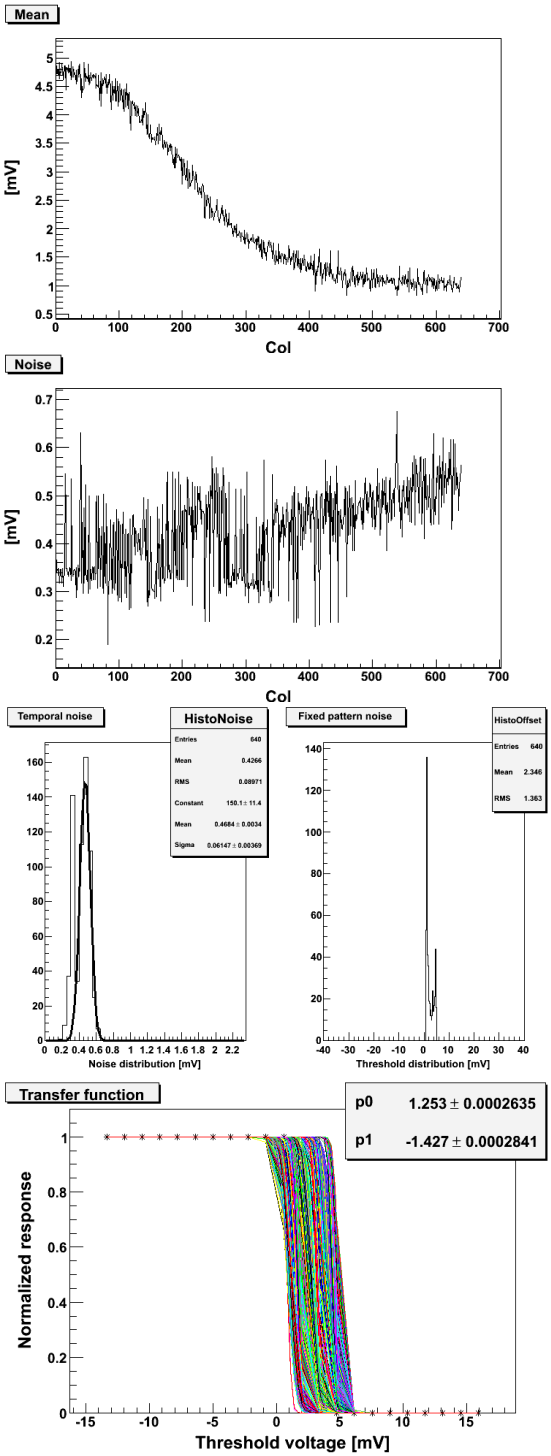
Figure 20 A set of discriminator threshold scans in the discriminator test mode on Phase1 chip D1. ICLPDISC was set to 0, 20, 45, 75, 95. These values were chosen so that the corresponding VCLPDICS voltage measured at test pads had the same value as settings used for the Phase2 E6 chip (Figure 19)

Appendix C

Discriminator test mode results

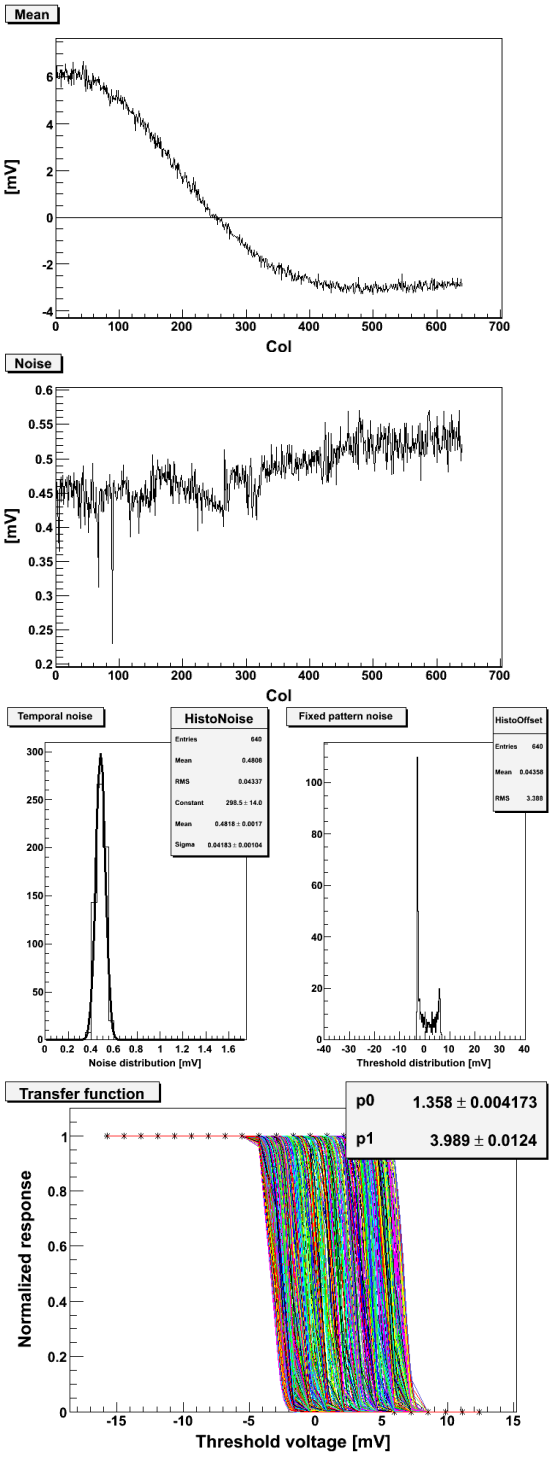


Phase 1 Chip D1
Default setting :
VClpdisc : 95
VRef2 : 117*

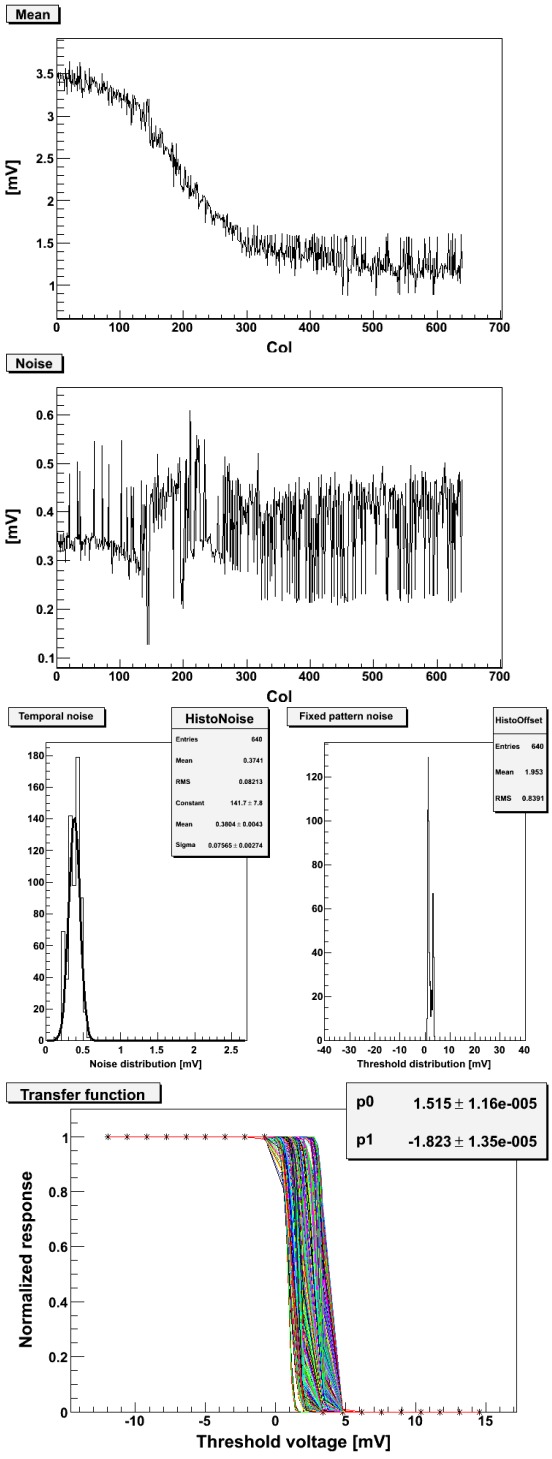


Phase2 Chip E6
Default settings :
VClpdisc : 86
VRef2 : 115

* **The values of VRef2 and VClpdisc for D1 and E6 were selected to provide the same voltage as measured on the corresponding test pads.**



Phase 1 Chip D1
VClpdisc : 20
VRef2 : 117



Phase 2 Chip E6
VClpdisc : 11
VRef2 : 115

***The values of VRef2 and VClpdisc for D1 and E6 were selected to provide the same voltage as measured on the corresponding test pads.**

Appendix D

Typical JTAG settings

Readout mode, DAC bias, and control register settings:

:RO_MODE_0[0]	0	:BIAS_DAC[0]	100	:CTRL[0]	639
:RO_MODE_0[1]	1	:BIAS_DAC[1]	10	:CTRL[1]	639
:RO_MODE_0[2]	0	:BIAS_DAC[2]	10	:CTRL[2]	639
:RO_MODE_0[3]	0	:BIAS_DAC[3]	10	:CTRL[3]	0
:RO_MODE_0[4]	0	:BIAS_DAC[4]	10	:CTRL[4]	0
:RO_MODE_0[5]	0	:BIAS_DAC[5]	40	:CTRL[5]	0
:RO_MODE_0[6]	0	:BIAS_DAC[6]	32		
:RO_MODE_0[7]	1	:BIAS_DAC[7]	50		
:RO_MODE_1[0]	0	:BIAS_DAC[8]	127		
:RO_MODE_1[1]	0	:BIAS_DAC[9]	80		
:RO_MODE_1[2]	0	:BIAS_DAC[10]	32		
:RO_MODE_1[3]	1	:BIAS_DAC[11]	32		
:RO_MODE_1[4]	0	:BIAS_DAC[12]	118		
:RO_MODE_1[5]	0	:BIAS_DAC[13]	118		
:RO_MODE_1[6]	0	:BIAS_DAC[14]	50		
:RO_MODE_1[7]	0	:BIAS_DAC[15]	5		

Sequencer settings:

:SEQ[0]	1	:SEQ[32]	0	:SEQ[64]	0	:SEQ[96]	0
:SEQ[1]	1	:SEQ[33]	0	:SEQ[65]	0	:SEQ[97]	0
:SEQ[2]	1	:SEQ[34]	0	:SEQ[66]	0	:SEQ[98]	0
:SEQ[3]	1	:SEQ[35]	0	:SEQ[67]	0	:SEQ[99]	0
:SEQ[4]	1	:SEQ[36]	0	:SEQ[68]	0	:SEQ[100]	0
:SEQ[5]	1	:SEQ[37]	0	:SEQ[69]	0	:SEQ[101]	0
:SEQ[6]	1	:SEQ[38]	0	:SEQ[70]	0	:SEQ[102]	0
:SEQ[7]	1	:SEQ[39]	0	:SEQ[71]	0	:SEQ[103]	0
:SEQ[8]	1	:SEQ[40]	0	:SEQ[72]	0	:SEQ[104]	0
:SEQ[9]	1	:SEQ[41]	0	:SEQ[73]	0	:SEQ[105]	0
:SEQ[10]	1	:SEQ[42]	0	:SEQ[74]	1	:SEQ[106]	0
:SEQ[11]	1	:SEQ[43]	0	:SEQ[75]	1	:SEQ[107]	0
:SEQ[12]	1	:SEQ[44]	0	:SEQ[76]	1	:SEQ[108]	0
:SEQ[13]	1	:SEQ[45]	1	:SEQ[77]	1	:SEQ[109]	0
:SEQ[14]	1	:SEQ[46]	1	:SEQ[78]	0	:SEQ[110]	0
:SEQ[15]	1	:SEQ[47]	0	:SEQ[79]	0	:SEQ[111]	0
:SEQ[16]	1	:SEQ[48]	0	:SEQ[80]	0	:SEQ[112]	1
:SEQ[17]	1	:SEQ[49]	0	:SEQ[81]	0	:SEQ[113]	1
:SEQ[18]	1	:SEQ[50]	1	:SEQ[82]	0	:SEQ[114]	1
:SEQ[19]	1	:SEQ[51]	1	:SEQ[83]	0	:SEQ[115]	1
:SEQ[20]	1	:SEQ[52]	1	:SEQ[84]	0	:SEQ[116]	1
:SEQ[21]	1	:SEQ[53]	0	:SEQ[85]	0	:SEQ[117]	1
:SEQ[22]	1	:SEQ[54]	0	:SEQ[86]	1	:SEQ[118]	1
:SEQ[23]	1	:SEQ[55]	0	:SEQ[87]	1	:SEQ[119]	1
:SEQ[24]	1	:SEQ[56]	0	:SEQ[88]	1	:SEQ[120]	1
:SEQ[25]	1	:SEQ[57]	0	:SEQ[89]	0	:SEQ[121]	1
:SEQ[26]	1	:SEQ[58]	0	:SEQ[90]	0	:SEQ[122]	1
:SEQ[27]	1	:SEQ[59]	0	:SEQ[91]	0	:SEQ[123]	1
:SEQ[28]	1	:SEQ[60]	0	:SEQ[92]	0	:SEQ[124]	1
:SEQ[29]	1	:SEQ[61]	0	:SEQ[93]	0	:SEQ[125]	1
:SEQ[30]	1	:SEQ[62]	0	:SEQ[94]	0	:SEQ[126]	1
:SEQ[31]	1	:SEQ[63]	0	:SEQ[95]	0	:SEQ[127]	1

Appendix E

Additional observations and remarks

In the initial tests that were performed to confirm operation of the LBL RDO and test boards, the noise performance of Phase-1 sensors was elevated compared to test results from LBL. We measured 3.6 ADC counts and more instead of the expected <3 ADC. After the chip was placed in a completely dark environment, the measured value agreed with LBL results.

While testing chip F4, external power source voltages were set to +5, -5 and +3.3V, but when the power supply was powered on, the +3.3 V module showed +5 V. This did not lead to permanent chip damage but in subsequent tests of this chip one of the analog channels was dead.

Reference voltage VREF1 in chip E3 cannot be measured on the test pad but the chip is fully operational. This problem was first observed during initial tests at LBL.

Initial test results in the discriminator test mode indicated a factor of two differences in FPN and temporal noise values measured by IPHC and LBL readout systems. A set of data was taken using the LBL readout and 16 parallel CMOS outputs. For this purpose we performed 4 acquisitions with 4 channels read out at a time. We used simple CMOS to LVDS adapter boards that had been assembled at LBL. Since the LBL readout system is designed to read 160 MHz digital outputs, the slower CMOS outputs running at 40 MHz had to be oversampled.
The set of four data acquisitions covering the complete pixel array were combined together and compared to our standard acquisition using LVDS outputs. The quality of data was the same and independent of the output type used.
The difference in FPN and temporal noise values was finally attributed to differences in analysis procedures – processing one row of pixels vs. summing all pixels in each column.