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LG
DRAFT

Proposal for Fabrication of a Phase-1 based Telescope.

The HFT Pixel sensor and RDO group has been testing and characterizing the Phase-1 sensors received from AMS early this year. The bench and source tests are mostly complete (a presentation of the progress as of June 2009 may be found here:
http://rnc.lbl.gov/hft/hardware/docs/iphc_2009_06/Phase-1_testing_LG.ppt)
A key sensor parameter is efficiency, and while the efficiency of sensors very similar to Phase-1 has been measured by IPHC, Phase-1 efficiency as a function of threshold, bias settings, voltage, etc. have not yet been measured. We propose to build a sensor telescope using 4 thinned Phase-1 sensors mounted to our existing Phase-1 individual test board design and use this telescope to measurePhase-1 efficiency with MIPS at a beam test. We will describe the construction of the telescope based on the adaptation of existing hardware and the testing plan that we hope to follow.

Hardware Design

The basic hardware design is shown below in schematic form.

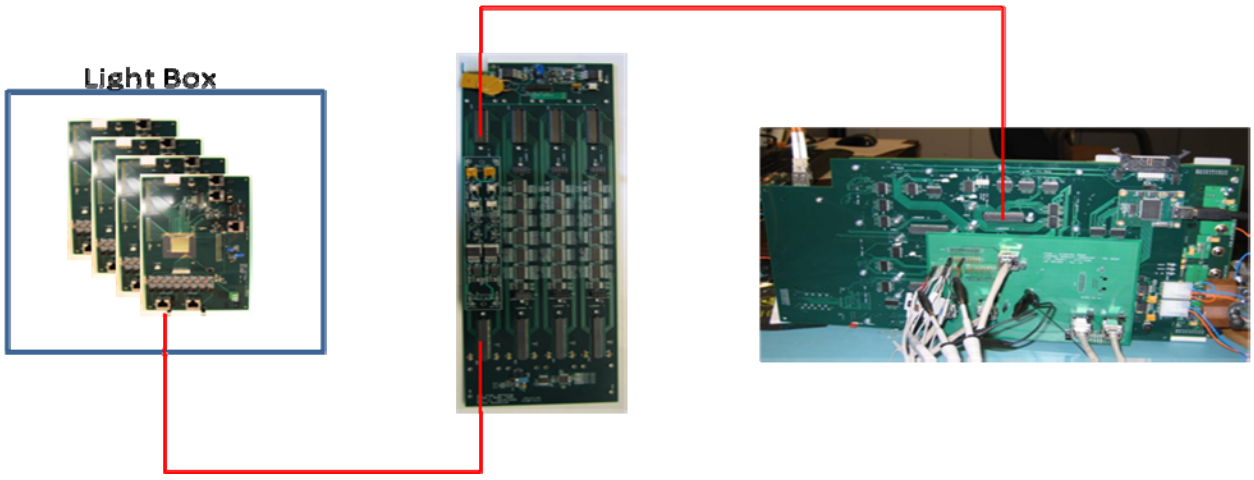

Figure 1 Basic telescope system consisting of 4 thinned Phase-1 sensors mounted to individual testing PCBs and contained in a light tight box. The PCBs are sensors are aligned treated as a ladder of 4 sensors by the rest of the RDO system. The LU protected power and signal buffering are provided by the mass termination boards and the power daughter-cards. The LVDS output signals are read into the motherboard/Xilinx Virtex-5 board combo in the same way as designed for a standard 10 sensor ladder.

In order to minimize multiple scattering, we will be removing the PCB FR-4 material under most of the active area of the sensors. We will also be using thinned sensors. We currently have a set of 5 sensors

which have been back-thinned and polished to a thickness of 120 um and were used for mechanical testing. We expect to use these sensors for the telescope.
The existing individual test board will need some small modification to allow for their use in a mass minimized telescope. The modification includes the milling of a square hole under the sensor area to remove the 0.032" of FR-4 PCB material per PCB from the MIP trajectories. The needed modification is shown in Figure 2.

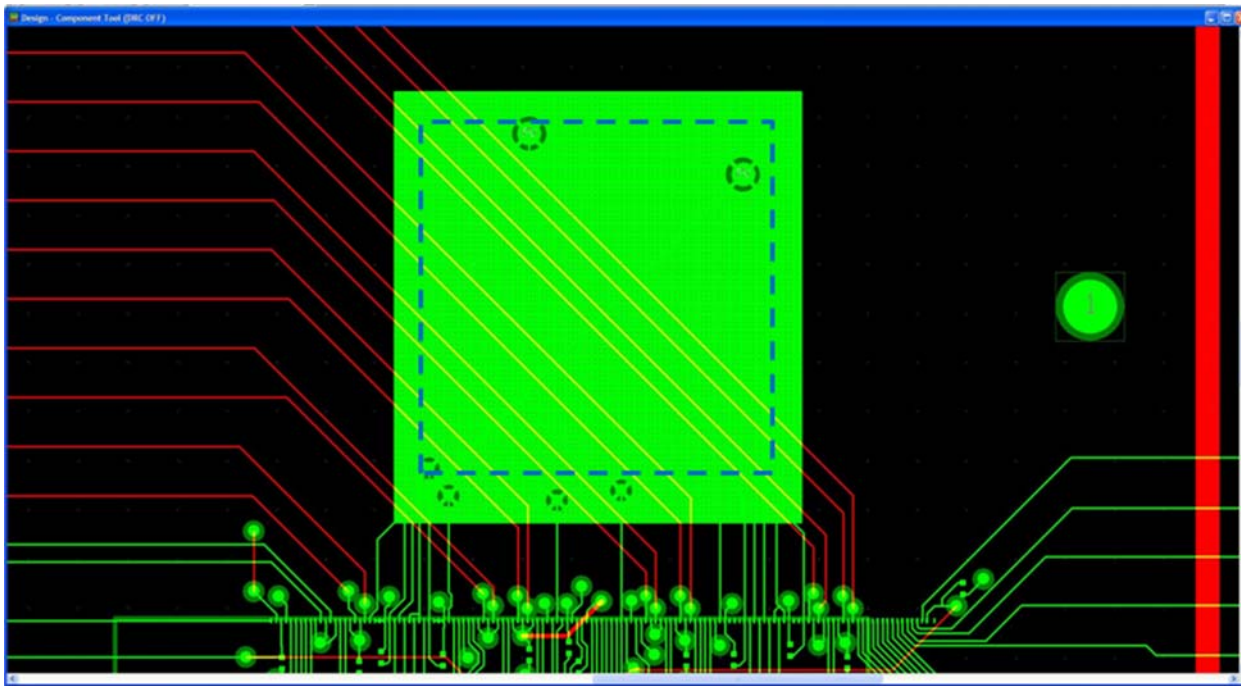

Figure 2 The modification of the existing Phase-1 testing PCB required for a low mass telescope is shown above. The layout of the ground pad under the sensor is shown. The top layer is green, the bottom layer is red. The square indicated by the dashed blue line must be removed by machining. This will cut the red bottom layer traces that are running through this area. Fortunately, these traces are the parallel sensor outputs which are unused in our application. The pads that lead to these traces will not be bonded out.

In addition to the PCB modification, we will need to fabricate a light tight box with beam windows and mechanical holding and locating fixtures for holding the PCBs in a known aligned position. The minimum distance between adjacent Phase-1 PCBs, based on component heights, is ~0.400".

Electrical Design

The electrical schematic for the Phase-1 testing board may be found here http://rnc.lbl.gov/hft/hardware/docs/Phase1/Phase-1_individual_test_board_patched_1.pdf. The manual for the Phase-1 sensor may be found here http://rnc.lbl.gov/hft/hardware/docs/Phase1/Phase-1_individual_test_board_patched_1.pdf. The JTAG chip configuration interface will be daisy chained between the individual test boards with patch wires. The Clock will be multi-dropped with termination on the last board in the chain. The START and SPEAK signals will be also multi-dropped. All signals onto

and off of each PBC are buffered on that PCB including the LVDS hit data signals. We anticipate using custom CAT-5 cabling that terminated onto our standard Samtec connector to bring all ladder control and data signals to and from the mass termination board (MTB). Power will be provided via multi-drop power cables into the existing Molex connectors on the Phase-1 PCBs. Power for the analog RDO section will be applied as required via a separate power supply. The control and data signals will be carried from the MTB to the RDO motherboard via the 6 meter 50-twisted pair cable used in the LVDS data path test. The use of the Phase-1 sensors in the telescope allows us to significantly simplify the bonding scheme. A new bonding diagram for the telescope PCB / Phase-1 sensor may be found here: http://rnc.lbl.gov/hft/hardware/docs/Phase1/PH1_bonding_diagram_individual_test_telescope.pdf. The hardware design involves board stacking and thus, the analog outputs will be available for only one of the end sensor boards. This is due to the necessity of using an analog amplifier/buffer plug in board that mounts perpendicularly to the plane of the testing board. In this design, we will be able to measure the analog pixel response on one sensor.

Firmware and Software

We are using the construction of this telescope as a preliminary test-bed for the firmware and software needed for the full ladder readout system. The firmware configuration will consist of the full functionality that is required for the ladder RDO implemented for 4 sensors instead of 10. At this point we will also be developing and implementing the full event data format. This event data format is expected to be the same for Phase-1 and Ultimate readout allowing for a single data decoding routine. This will provide a more friendly software development environment. A document describing the firmware requirements may be found here http://rnc.lbl.gov/hft/hardware/docs/Phase1/Phase-1_RDO_firmware_requirements.pdf. This development effort is still ongoing and we expect to provide more information in the next 2 weeks.

Triggering

Triggering is necessary for this detector telescope. There are several options that we can use for triggering with each option depending on where and the conditions in which we get test beam. In general, however, we will plan on making our own trigger detectors. We will design scintillator based counters to be placed before and after the active area of the telescope. The coincidence of these detectors will constitute our trigger to readout the sensor telescope. We will perform the coincidence in the FPGA on our motherboard. Inputs will be via one of our test board interface boards. We will add functionality to also allow for an accelerator “flattop” type spill indicator input into our coincidence scheme.

Test Plan

We are currently investigating places to obtain test beam. The accelerators that we are investigating are at CERN< Fermilab, ALS and possibly SLAC. We will follow up with the test beam schedules and

suitability of each possible facility. We plan to follow the following outline of a test plan in order to test our sensor telescope. After we choose a test beam facility, we will update and expand this test plan.

Starting point –

- Sensors that make up the telescope are fully characterized and the bias settings are optimized.
- Mechanical hardware is complete.
- Sensors are aligned in the box and with the scintillator counters.
- Mechanical assembly is complete and the box is light tight.
- Firmware and online analysis software has been tested and is working.
- System has been successfully tested and run on cosmic ray muons.

After system is set up in beam line:

1. Run system with all sensors at optimized (obtained from sensor characterization and based on minimizing discriminator transfer function dispersion)settings.
2. Set discriminator thresholds to 3X noise value. Update as needed such that we have a small number of noise counts ~10/sensor.
3. Take ~10k events.
4. Evaluate windowed coincidence rate between first and last sensors in the detector telescope.
5. If the rate is > 90% leave the settings the same for the first and last sensors.
6. Vary the threshold settings in 0.25 mV increments on sensor # 2 taking 1k events / run.
7. Resetting the threshold value of sensor #2 to the optimized setting, vary the threshold settings in 0.5 mV increments on sensor # 3 taking 1k events / run.
8. For sensors #2 and #3 take a set of 1k event runs at 5 discriminator settings that trace the efficiency curve for each ICLPDISC setting of 20, 50, 70, 100.
9. For sensors #2 and #3 take a set of 1k event runs at 5 discriminator settings that trace the efficiency curve for each VREF2 setting of +/- 1.
10. For sensors #2 and #3 take a set of 1k event runs at 5 discriminator settings that trace the efficiency curve for each IPIX setting of +/- 10.
11. Attach the analog output buffer section to the first sensor test board.
12. Take analog data for 5k events.