LG 04/17/2008

Pixel Phase-1 RDO Firmware Requirements

Normal Data Taking

We anticipate 2 modes for normal beam data taking and testing/calibration at STAR:

Mode 1: System is under local control and Pixel group can control the system, readout can be via SIU or USB. If readout is by SIU, data can be stored on the receiver PC HD.

Mode 2: System is under DAQ control. System will be put into a running condition in which it responds to triggers and other DAQ controls appropriately but user control is locked out.

Under both modes, the system shall operate according to the design architecture described at http://rnc.lbl.gov/hft/hardware/docs/Addendum_rdo_2007_12_26.pdf A proposed event data format will be added later.

Testing Modes

The RDO system is designed to function as a full RDO system for data taking as well as the platform for all individual sensor testing, probe testing and ladder testing. The additional capabilities dictated by these additional tasks will add further functional requirements.

Anticipated Testing Tasks

Testing individual Mimosa-22 and Phase-1 sensors. –
Mimosa-22e has analog outputs 8 columns that can be read simultaneously with the discriminator outputs in the normal data path. In order to test these sensors we need the capability to;

1. Use JTAG for sensor initialization and settings.
2. Provision of clocks and internal logic allowing for synchronization and marker checking.
3. Simultaneously take correlated ADC and digital information. Digital clock ≤ 200 MHz, Analog clock ≤ 60 MHz.
4. USB and SIU interface and control shell.
5. Internal (FPGA) scripting via soft CPU.
6. Memory buffer storage for multiple events with asynchronous RDO via SIU or USB.
7. Provision for additional general purpose i/o to be used for testing purposes, e.g. flashing LEDs, oscilloscope triggers, etc.

Probe Testing individual thinned sensors –
In this task, the basic functionality of the individual sensor testing as described above is needed, but additional capabilities may be required. Some of these functions may be added on the probe card or as an additional daughter-card PCB. Additional functionality would include;

1. Significant additional scripting capabilities probably through the soft CPU
2. Additional control i/o and internal control logic for tasks such as turning on and off power supplies, interface to ADCs to measure currents, voltages, etc.
3. Expanded interface with external software on control PCs for analysis, storage of parameters into a database, etc.

Ladder testing –
This is very similar to the normal data taking path. Additional capabilities would probably be limited to the items listed under the individual sensor testing requirements.